# Current Limits – Part II
# Base Line Text

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# Motivation

- Current monitoring limits were established as shown in

http://www.ieee802.org/3/bt/public/sep14/Balasubramanian_01_0914.pdf

- Next Steps
  - Suggest changes to relevant text sections defining “Control behavior” during inrush, $I_{cut}$ and $I_{lim}$

# Relevant Text sections

| Parameter | Text Section |
|---|---|
| Inrush | 33.2.7.5 (PSE), 33.3.7.3 (PD) |
| Overload current ($I_{cut}$) | 33.2.7.6 (33.2.7.4) |
| Output Current at Short Circuit Condition ($I_{lim}$) | 33.2.7.7 |

# Inrush – Original Section 33.2.7.5

POWER_UP mode occurs between the PSE's transition to the POWER_UP state and either the expiration of TInrush or the conclusion of PD inrush currents (see 33.3.7.3). However, for practical implementations, it is recommended that the POWER_UP mode persist for the complete duration of TInrush, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.

The PSE shall limit the maximum current sourced at the PI during POWER_UP. The maximum inrush current sourced by the PSE shall not exceed the PSE inrush template in Figure 33–13.

a) During POWER_UP, for PI voltages between 0 V and 10 V, the minimum IInrush requirement is 5 mA.

b) During POWER_UP, for PI voltages between 10 V and 30 V, the minimum IInrush requirement is 60 mA.

c) During POWER_UP, for PI voltages above 30 V, the minimum IInrush requirement is as specified in Table 33–11.

d) For Type 1 PSE, measurement of minimum IInrush requirement to be taken after 1 ms to allow startup transients. A Type 2 PSE that uses 1-Event physical layer classification, and requires the 1 ms settling time, shall power up a class 4 PD as if it used 2-Event physical layer classification.

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$$I_{PSEIT}(t) = \begin{cases} 50.0 & for\ \ 0 < t < 10.0X10^{-6} \\ 50.0 - \dfrac{(t - 10.0X10^{-6})X49.6}{0.990X10^{-6}} & for\ \ 10.0X10^{-6} \le t < 0.001 \\ 0.450 & for\ \ 0.001 \le t < 0.075 \end{cases}_A \qquad (33\text{-}5)$$

# Inrush – Section 33.2.7.5 Changes

POWER_UP mode occurs on each pair-set between the PSE's transition to the POWER_UP state on that pair-set and either the expiration of Tinrush-2P or the conclusion of PD inrush currents on that pair-set (see 33.3.7.3). However, for practical implementations, it is recommended that the POWER_UP mode on a pair-set persist for the complete duration of Tinrush-2P, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.

The PSE shall limit the maximum current sourced ~~at the PI~~ per pair-set during POWER_UP. The maximum inrush current sourced by the PSE per pair-set shall not exceed the per pair-set inrush template in Figure 33–13.

a) During POWER_UP, for ~~PI~~ pair-set voltages between 0 V and 10 V, the minimum per pair-set $I_{inrush\text{-}2p}$ requirement is 5 mA.

b) During POWER_UP, for ~~PI~~ pair-set voltages between 10 V and 30 V, the minimum per pair-set $I_{inrush\text{-}2p}$ requirement is 60 mA.

c) During POWER_UP, for ~~PI~~ pair-set voltages above 30 V, the minimum per pair-set $I_{Inrush\text{-}2p}$ requirement is as specified in Table 33–11.

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$$I_{PSEIT-2P}(t) = \begin{cases} 50.0 & for\ \ 0 < t < 10.0X10^{-6} \\ 50.0 - \dfrac{(t - 10.0X10^{-6})X49.6}{0.990X10^{-6}} & for\ \ 10.0X10^{-6} \le t < 0.001 \\ 0.450 & for\ \ 0.001 \le t < 0.075 \end{cases}_A \qquad (33\text{-}5)$$

# Inrush – Original Section 33.3.7.3

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with VPort_PD requirements as defined in Table 33–18, and ending when CPort is charged to 99% of its final value. This period should be less than TInrush min per Table 33–11.

Type 2 PDs with pse_power_type state variable set to 2 prior to power-on shall behave like a Type 1 PD for at least Tdelay min. Tdelay starts when VPD crosses the PD power supply turn on voltage, VOn. This delay is required so that the Type 2 PD does not enter a high power state before the PSE has had time to switch current limits from IInrush to ILIM.

Problem with existing text:

Inrush doesn't necessarily end with Cport 99% charged – if Cport>180uf, PD does inrush control to meet the 400mA and at the end of Tinrush min Cport might not be 99% charged.

# Inrush – Section 33.3.7.3 Changes

Inrush current per pair-set is drawn beginning with the application of input voltage at the pair-set compliant with Vport_PD-2P requirements as defined in Table 33-18, and ending before Tinrush-2P min per Table 33-11. After Tinrush-2P min, the PD shall not exceed its per pair set current threshold corresponding to its class level.

Type 2, Type 3 and Type 4 PDs with pse_power_type state variable set to 2, 3 and 4 respectively, prior to power-on shall behave like a Type 1 PD for at least Tdelay-2P min. Tdelay-2P for each pair-set starts when VPD-2P crosses the PD power supply turn on voltage, VOn. This delay is required so that the Type 2, Type 3 and Type 4 PD does not enter a high power state before the PSE has had time to switch current limits on each pair-set from Iinrush-2P to ILIM-2P.

# Overload – Section 33.2.7.6 Original

If IPort, the current supplied by the PSE to the PI, exceeds ICUT for longer than TCUT, the PSE may remove power from the PI. The cumulative duration of TCUT is measured with a sliding window of at least 1 second width.

The ICUT threshold may equal the IPeak value determined by Equation (33–4).

# Overload – Section 33.2.7.6 Changes

**Section 33.2.7.6 Changes:**

If Iport-2p, the current supplied per pair-set by the PSE to the PI, exceeds ICUT-2P for longer than TCUT-2P, the PSE may remove power from that ~~PI~~ pair-set. The cumulative duration of TCUT-2P is measured with a sliding window of at least 1 second width.

The ICUT-2P threshold may equal the Ipeak-2P value determined by Equation (33–4).

# Overload – Original Section 33.2.7.4

In addition to ICon as specified in Table 33–11, the PSE shall support the following AC current waveform parameters, while within the operating voltage range of VPort_PSE:

Ipeak minimum for TCUT minimum and 5 % duty cycle minimum, where

$$I_{peak} = \left\{ \frac{V_{PSE} - \sqrt{V_{PSE} - 4(R_{Chan})(P_{Peak\_PD})}}{2(R_{Chan})} \right\}_A \qquad (33\text{-}4)$$

$V_{PSE}$ is the voltage at the PSE PI as defined in 1.4.413

$R_{chan}$ is the channel loop resistance as defined in 33.1.4; this parameter has a worst- case value of RCh, defined in Table 33–1

$P_{peak\_PD}$ is the peak power a PD may draw for its class; see Table 33–18

# Overload – Section 33.2.7.4 Changes

In addition to Icon-2P as specified in Table 33–11, the PSE shall support the following AC current waveform parameters per pair-set, while within the operating voltage range of VPort_PSE-2P:

Ipeak-2P minimum for TCUT-2P minimum and 5 % duty cycle minimum, where

$$I_{peak-2P} = \left\{ \frac{V_{PSE-2P} - \sqrt{V_{PSE-2P} - 4(R_{Chan})(P_{Peak\_PD-2P})}}{2(R_{Chan})} \right\}_A + \mathrm{K} \qquad (33\text{-}4)$$

$V_{PSE\text{-}2P}$ is the voltage per pair-set at the PSE PI as defined in 1.4.413

$R_{chan}$ is the channel loop resistance as defined in 33.1.4; this parameter has a worst- case value of $R_{Ch}$, defined in Table 33–1

$P_{peak\_PD\text{-}2P}$ is the peak power a PD may draw per pair-set;

K is the factor due to “unbalance effect”

# Short Circuit – Original Section 33.2.7.7

A PSE may remove power from the PI if the PI current meets or exceeds the “PSE lowerbound template” in Figure 33–14. Power shall be removed from the PI of a PSE before the PI current exceeds the “PSE upperbound template” in Figure 33–14.

The maximum value of ILIM is the PSE upperbound template described by Equation (33–6) and Figure 33–14.

The PSE upperbound template, IPSEUT, is defined by the following segments:

$$I_{PSEUT}(t) = \left\{ \begin{array}{ll} 50.0 & \text{for}(0 \le t < 10.0X10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for}(10.0X10^{-6} \le t < 8.20X10^{-3}) \\ 1.75 & \text{for}(8.20X10^{-3} \le t < T_{cut\max}) \\ I_{\text{limmin}} & \text{for}(T_{\text{cutmax}} \le t) \end{array} \right\}_A \qquad (33\text{-}6)$$

Where

*t* is the duration in seconds that the PSE sources IPort

*K* is 0.025 $A^2s$, an energy limitation constant for the port current when it is not in steady state normal operation

*T*cutmax is TCUT max, as defined in Table 33–11

*I*limmin is ILIM min, as defined in Table 33–11

# Short Circuit – Section 33.2.7.7 Changes

A PSE may remove power from ~~the~~ a pair-set of a PI if the ~~PI~~ pair-set current meets or exceeds the "PSE lowerbound template" in Figure 33–14. Power shall be removed from ~~the~~ a pair-set ~~PI~~ of a PSE before the ~~PI~~ pair-set current exceeds the "PSE upperbound template" in Figure 33–14.

The maximum value of ILIM-2P is the PSE upperbound template described by Equation (33–6) and Figure 33–14.

The PSE upperbound template, IPSEUT-2P, is defined by the following segments:

$$I_{PSEUT-2P}(t) = \left\{ \begin{array}{ll} 50.0 & \text{for}(0 \le t < 10.0X10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for}(10.0X10^{-6} \le t < 8.20X10^{-3}) \\ 1.75 & \text{for}(8.20X10^{-3} \le t < T_{cut\,\max-2P}) \\ I_{\text{limmin}-2P} & \text{for}(T_{\text{cutmax-2P}} \le t) \end{array} \right\}_A \qquad (33\text{-}6)$$

Where

*t* is the duration in seconds that the PSE sources IPort

*K* is 0.025 $A^2s$, an energy limitation constant for the ~~port~~ pair-set current when it is not in steady state normal operation

*T*cutmax-2P is TCUT max per pair-set, as defined in Table 33–11

*I*limmin-2P is ILIM min per pair-set, as defined in Table 33–11

# Short Circuit – Original Section 33.2.7.7 contd

The PSE shall limit the current to ILIM for a duration of up to TLIM in order to account for PSE dV/dt transients at the PI. The cumulative duration of TLIM may be measured with a sliding window.

The PSE lowerbound template, IPSELT, is defined by the following segments:

$$I_{PSELT}(t) = \left\{ \begin{array}{ll} I_{\text{limmin}} & \text{for}(0 \le t < T_{\text{limmin}}) \\ I_{peak} & \text{for}(T_{\text{limmin}} \le t < T_{cut\,\text{min}}) \\ \dfrac{Pclass}{VPSE} & \text{for}(\text{T}_{\text{cutmin}} \le t) \end{array} \right\}_A$$

where

| | |
|---|---|
| $I_{\text{limmin}}$ | is the ILIM min value for the PSE (see Table 33–11) |
| *t* | is the duration that the PI sources IPort |
| Tlimmin | is TLIM min as defined in Table 33–11 |
| *T*cutmin | is TCUT min, as defined in Table 33–11 |
| *I*Peak | is IPeak, as defined in Equation (33–4) |
| *P*Class | is PClass, as defined in Table 33–7 |
| *V*PSE | is the voltage at the PSE PI |

If a short circuit condition is detected, power removal from the PI shall begin within TLIM as specified in Table 33–11. If IPort exceeds the PSE lowerbound template, the PSE output voltage may drop below VPort_PSE min.

# Short Circuit – Section 33.2.7.7 Changes contd

The PSE shall limit ~~the~~ a pair-set current to ILIM-2P for a duration of up to TLIM-2P in order to account for PSE dV/dt transients at the ~~PI~~ pair-set. The cumulative duration of TLIM-2P may be measured with a sliding window.

The PSE lowerbound template, IPSELT-2P, is defined by the following segments:

$$I_{PSELT-2P}(t) = \left\{ \begin{array}{ll} I_{\text{limmin}-2P} & \text{for}(0 \le t < T_{\text{limmin}-2P}) \\ I_{peak-2P} & \text{for}(T_{\text{limmin}-2P} \le t < T_{cut\,\text{min}-2P}) \\ TBD & \text{for}(T_{\text{cutmin-2P}} \le t) \end{array} \right\}_A$$

where

$I_{\text{limmin-2P}}$ is the ILIM min value per pair-set for the PSE (see Table 33–11)

$t$ is the duration that the PI sources IPort

$T_{\text{limmin-2P}}$ is TLIM min per pair-set as defined in Table 33–11

$T_{\text{cutmin-2P}}$ is TCUT min per pair-set, as defined in Table 33–11

$I_{\text{peak-2P}}$ is Ipeak per pair-set, as defined in Equation (33–4)

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If a short circuit condition is detected on a pair-set, power removal from ~~the~~ that pair-set shall begin within TLIM-2P as specified in Table 33–11. If IPort-2P exceeds the PSE lowerbound template, the PSE output voltage on that pair-set may drop below VPort_PSE-2P min.

# THANK YOU