**33.2.4 PSE state diagrams**

The PSE shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–9 continued, and

Figure 33–10.

**33.2.4.1 Overview**

Detection, classification, and power turn-on timing shall meet the specifications in Table 33–4, Table 33–10, and Table 33–11.

If power is to be applied, the PSE turns on power after a valid detection in less than Tpon as specified in Table 33–11. If the PSE cannot supply power within Tpon, it initiates and successfully completes a new detection cycle before applying power.

It is possible that two separate PSEs, one that implements Alternative A and one that implements Alternative B (see 33.2.1), may be attached to the same link segment. In such a configuration, and without the required backoff algorithm, the PSEs could prevent each other from ever detecting a PD by interfering with the detection process of the other.

A PSE performing detection using Alternative B may fail to detect a valid PD detection signature. When this occurs, the PSE backs off for at least Tdbo as specified in Table 33–11 before attempting another detection. During this backoff, the PSE shall not apply a voltage greater than VOff to the PI.

If a PSE performing detection using Alternative B detects an open circuit (see 33.2.5.5) on the link section, then that PSE may optionally omit the detection backoff.

If a PSE performing detection using Alternative A detects an invalid signature, it should complete a second detection in less than Tdbo min after the beginning of the first detection attempt. This allows an Alternative A PSE to complete a successful detection cycle prior to an Alternative B PSE present on the same link section that may have caused the invalid signature.

NOTE—A Type 1 PSE performing detection using Alternative A may need to have its DTE powering ability disabled when it is attached to the same link segment as a Type 2 Midspan PSE performing detection using Alternative B. This allows the Midspan PSE to successfully complete a detection cycle.

**33.2.4.2 Conventions**

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

**33.2.4.3 Constants**

The PSE state diagrams use the following constants: PSE\_TYPE

A constant indicating the type of the PSE Values: 1: Type 1 PSE

2: Type 2 PSE

3: Type 3 PSE

4: Type 4 PSE

**33.2.4.4 Variables**

The PSE state diagrams use the following variables:

class\_num\_events

A variable indicating the maximum number of classification events performed by the PSE. A variable that is set in an implementation-dependent manner.

Values: 0: PSE does not perform Physical Layer classification.

1: PSE performs 1-Event Physical Layer classification.

2: PSE performs Mulitple-Event Physical Layer classification with a maximum of 2 class events.

4: PSE performs Multiple-Event Physical Layer classification with a maximum of 4 class events.

5: PSE performs Multiple-Event Physical Layer classification with a maximum of 5 class events.

error\_condition

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 33–11 and that require the PSE not to source power. These error conditions are different from those monitored by the state diagrams in Figure 33–10.

Values: FALSE: No fault indication.

TRUE: A fault indication exists.

IInrush

Output current during POWER\_UP (see Table 33–11 and Figure 33–13).

IPort

Output current (see 33.2.7.6).

legacy\_powerup

This variable is provided for PSEs that monitor the PI voltage output and use that information to indicate the completion of PD inrush current during POWER\_UP operation. Using only the PI voltage information may be insufficient to determine the true end of PD inrush current; use of a fixed TInrush period is recommended. A variable that is set in an implementation-dependent manner.

Values: TRUE: The PSE supports legacy power up; this value is not recommended.

FALSE: The PSE does not support legacy power up. It is highly recommended that new equipment use this value.

mr\_mps\_valid

The PSE monitors either the DC or AC Maintain Power Signature (MPS, see 33.2.9.1). This variable indicates the presence or absence of a valid MPS.

Values: FALSE: If monitoring both components of the MPS, the DC component of MPS is absent or the AC component of MPS is absent. If monitoring only one component of MPS, that component of MPS is absent.

TRUE: If monitoring both components of the MPS, the DC component of MPS and the AC component of MPS are both present. If monitoring only one component of MPS, that component of MPS is present.

mr\_pse\_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table

33–2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.

Values: A: The PSE uses PSE pinout Alternative A.

B: The PSE uses PSE pinout Alternative B.

A & B: PSE uses PSE pinout Alternative A and Alternative B

mr\_pse\_enable

A control variable that selects PSE operation and test functions. This variable is provided by a management interface that may be mapped to the PSE Control register PSE Enable bits (11.1:0), as described below, or other equivalent functions.

Values: disable: All PSE functions disabled (behavior is as if there was no PSE

functionality). This value corresponds to MDIO register bits 11.1:0 =

'00'.

enable: Normal PSE operation. This value corresponds to MDIO register bits

11.1:0 = '01'.

force\_power: Test mode selected that causes the PSE to apply power to the PI when there are no detected error conditions. This value corresponds to MDIO register bits 11.1:0 = '10'.

option\_detect\_ted

This variable indicates if detection can be performed by the PSE during the ted\_timer interval. Values: FALSE: Do not perform detection during ted\_timer interval.

TRUE: Perform detection during ted\_timer interval. option\_vport\_lim

This optional variable indicates if VPSE is out of the operating range during normal operating state. Values: FALSE: VPSE is within the VPort\_PSE operating range as defined in Table 33–11.

TRUE: VPSE is outside of the VPort\_PSE operating range as defined in Table 33–11.

ovld\_detected

A variable indicating if the PSE output current has been in an overload condition (see 33.2.7.6) for at least TCUT of a one second sliding time.

Values: FALSE: The PSE has not detected an overload condition.

TRUE: The PSE has detected an overload condition. pd\_dll\_power\_type

A control variable output by the PSE power control state diagram (Figure 33–27) that indicates the type of PD as advertised through Data Link Layer classification.

Values: 1: PD is a Type 1 PD (default)

2: PD is a Type 2 PD

3: PD is a Type 3 PD4: PD is a Type 4 PD

pi\_powered

A variable that controls the circuitry that the PSE uses to power the PD. Values: FALSE: The PSE is not to apply power to the link (default).

TRUE: The PSE has detected a PD, classified it if applicable, and determined the PD

is to be powered; or power is being forced on in TEST\_MODE.

power\_applied

A variable indicating that the PSE has begun steady state operation by having asserted pi\_powered, completed the ramp of voltage, is not in a current limiting mode, and is operating beyond the POWER\_UP requirements of 33.2.7.5.

Values: FALSE: The PSE is either not applying power or has begun applying power but is still in POWER\_UP.

TRUE: The PSE has begun steady state operation. power\_not\_available

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power to support the attached PD. Sufficient power is defined by classification; see 33.2.6.

Values: FALSE: PSE is capable to continue to source power to a PD.

TRUE: PSE is no longer capable of sourcing power to a PD. pse\_available\_power

This variable indicates the highest power PD Class that could be supported. The value is determined in an implementation-specific manner.

Values: 0: Class 1

1: Class 2

2: Class 0 and Class 3

3: Class 4

4: Class 5

5: Class 6

6: Class 7

pse\_dll\_capable

This variable indicates whether the PSE is capable of performing optional Data Link Layer classification. See 33.6. This variable is provided by a management interface that may be mapped to the PSE Control register Data Link Layer Classification Capability bit (11.5), as described below, or other equivalent functions. A variable that is set in an implementation-dependent manner.

Values: FALSE: The PSE’s Data Link Layer classification capability is not enabled.

TRUE: The PSE’s Data Link Layer classification capability is enabled.

pse\_dll\_enabled

A variable indicating whether the Data Link Layer classification mechanism is enabled. See 33.6.

Values: FALSE: Data Link Layer classification is not enabled.

TRUE: Data Link Layer classification is enabled.

pse\_ready

Variable that is asserted in an implementation-dependent manner to probe the link segment. Values: FALSE: PSE is not ready to probe the link segment.

TRUE: PSE is ready to probe the link segment.

NOTE—Care should be taken when negating this variable in a PSE performing detection using Alternative A after an invalid signature is detected due to the delay it introduces between detection attempts (see 33.2.4.1).

pse\_reset

Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality. Values: FALSE: Do not reset the PSE state diagram.

TRUE: Reset the PSE state diagram. pse\_skips\_multiclass

The PSE can choose to bypass a portion of the classification state flow. A variable that is set in an implementation-dependent manner.

Values: FALSE: The PSE does not bypass MARK\_EV1 and all subsequent mark and class states.

TRUE: The PSE does bypass MARK\_EV1 and all subsequent mark and class states.

short\_detected

A variable indicating if the PSE output current has been in a short circuit condition for TLIM within a sliding window (see 33.2.7.7).

Values: FALSE: The PSE has not detected a short circuit condition.

TRUE: The PSE has detected qualified short circuit condition.

temp\_var

A temporary variable used to store the value of the state variable mr\_pd\_class\_detected.

PSEs shall meet at least one of the allowable variable definition permutations described in Table 33–3.

**Table 33–3—Allowed PSE variable definition permutations**

|  |  |  |
| --- | --- | --- |
| **PSE Type** | **Variables** | |
| **class\_num\_events** | **pse\_dll\_capable** |
| Type 4 | 5 | FALSE |
| TRUE |
| 1 | TRUE |
| Type 3 | 4 | FALSE |
| TRUE |
| 2 | FALSE2 |
| TRUE |
| 1 | FALSE1 |
| TRUE |
| Type 2 | 2 | FALSE |
| TRUE |
| 1 | TRUE |
| Type 1 | 1 | FALSE |
| TRUE |
| 0 | FALSE |
| TRUE |
| Note 1—A Type 3 PSE with a guaranteed power output of 15.4W or less can be limited to one class event without requiring dll capability. | | |
| Note 2—A Type 3 PSE with a guaranteed power output of 30W or less can be limited to two class events without requiring dll capability. | | |

**33.2.4.5 Timers**

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where “stop x\_timer” is asserted.

tcle1\_timer

A timer used to limit the first classification event time in Multiple-Event classification for Type 1 and Type 2 PSEs; see TCLE1 in Table 33–10.

tcle2\_timer

A timer used to limit the second classification event time in Multiple-Event classification; see TCLE2 in Table 33–10.

tcle3\_timer

A timer used to limit the third through fifth classification event time in Multiple Event classification; see TCLE3 in Table 33–10.

tlcf\_timer

A timer used to limit the first classification event time in Multiple-Event classification for Type 3 and Type 4 PSEs; see TLCF in Table 33–10.

tdbo\_timer

A timer used to regulate backoff upon detection of an invalid signature; see Tdbo in Table 33–11. tdet\_timer

A timer used to limit an attempt to detect a PD; see Tdet in Table 33–11. ted\_timer

A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal; see Ted in Table 33–11. The default state of this timer is ted\_timer\_done.

tinrush\_timer

A timer used to monitor the duration of the inrush event; see TInrush in Table 33–11. tme1\_timer

A timer used to limit the first mark event time in Multiple-Event classification; see TME1 in Table 33–10.

tme2\_timer

A timer used to limit the final mark event time in Multiple-Event classification; see TME2 in Table 33–10.

tmpdo\_timer

A timer used to monitor the dropout of the MPS; see TMPDO in Table 33–11. tpdc\_timer

A timer used to limit the classification time; see Tpdc in Table 33–10. tpon\_timer

A timer used to limit the time for power turn-on; see Tpon in Table 33–11.

**33.2.4.6 Functions**

do\_classification

This function returns the following variables:

pd\_requested\_power: This variable indicates the power class requested by the PD. A Type 1 PSE

that measures a Class 4 signature assigns that PD to Class 0. See 33.2.6.

|  |  |  |
| --- | --- | --- |
| Values: | 0: | Class 1 |
|  | 1: | Class 2 |
|  | 2: | Class 0 or Class 3 |
|  | 3: | Class 4 |
|  | 4: | Class 5 (mr\_pd\_class\_detected will have a value of 4 for the first two  class events and a value of ‘1’ for any subsequent class events) |
|  | 5: | Class 6 (mr\_pd\_class\_detected will have a value of 4 for the first two  class events and a value of ‘2’ for any subsequent class events) |
|  | 6: | Class 7 (mr\_pd\_class\_detected will have a value of 4 for the first two  class events and a value of ‘3’ for any subsequent class events) |

mr\_pd\_class\_detected: The PD classification signature seen during a classification event; see Table 33–7 and 33.2.6.

|  |  |  |
| --- | --- | --- |
| Values: | 0: | Class 0 |
|  | 1: | Class 1 |
|  | 2: | Class 2 |
|  | 3: | Class 3 |
|  | 4: | Class 4 |

do\_detection

This function returns the following variables:

signature:

This variable indicates the presence or absence of a PD.

Values: open\_circuit: The PSE has detected an open circuit. This value is optionally returned by a PSE performing detection using Alternative B.

valid: The PSE has detected a PD requesting power.

invalid: Neither open\_circuit, nor valid PD detection signature has been found.

mr\_valid\_signature:

This variable indicates that the PSE has detected a valid signature.

|  |  |  |
| --- | --- | --- |
| Values: | FALSE: | No valid signature detected. |
|  | TRUE: | Valid signature detected. |

do\_mark

This function produces the classification mark event voltage. This function does not return any variables.

set\_parameter\_type

This function is used by a Type 2, Type 3, or Type 4 PSE to evaluate the type of PD connected to the link based on Physical Layer classification or Data Link Layer classification results. The PSE’s PI electrical requirements defined in Table 33–11 are set to values corresponding to either a Type 1, Type 2, Type 3, or Type 4 PSE. This function returns the following variable:

parameter\_type: A variable used by a Type 2 PSE, Type 3 PSE, or Type 4 PSE to pick between Type 1, Type 2, Type 3, and Type 4 PI electrical requirement parameter values defined in Table 33–11.

|  |  |  |
| --- | --- | --- |
| Values: | 1: | Type 1 PSE parameter values (default) |
|  | 2: | Type 2 PSE parameter values |
|  | 3: | Type 3 PSE parameter values |
|  | 4: | Type 4 PSE parameter values |

When a Type 2 PSE powers a Type 2, Type 3, or Type 4 PD, the PSE may choose to assign a value of ‘1’ to parameter\_type if mutual identification is not complete (see 33.2.6) and shall assign a value of ‘2’ to parameter\_type if mutual identification is complete. When a Type 3 PSE powers a Type 2, Type 3, or Type 4 PD, the PSE may choose to assign a value of ‘1’ or ‘2’ to parameter\_type if mutual identification is not complete (see 33.2.6) and shall assign a value of ‘3’ to parameter type if mutual identification is complete. When a Type 4 PSE powers a Type 2, Type 3, or Type 4 PD, the PSE may choose to assign a value of ‘1’, ‘2’, or ‘3’ to parameter\_type if mutual identification is not complete (see 33.2.6) and shall assign a value of ‘4’ to parameter type if mutual identification is complete.

When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for ICon, ILIM, TLIM, and PType (see Table 33–11).

When a Type 3 PSE powers a Type 1 PD, the PSE shall meet the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 or Type 3 PSE for ICon, ILIM, TLIM, and PType , IInrush , ICUT (see Table 33–11).

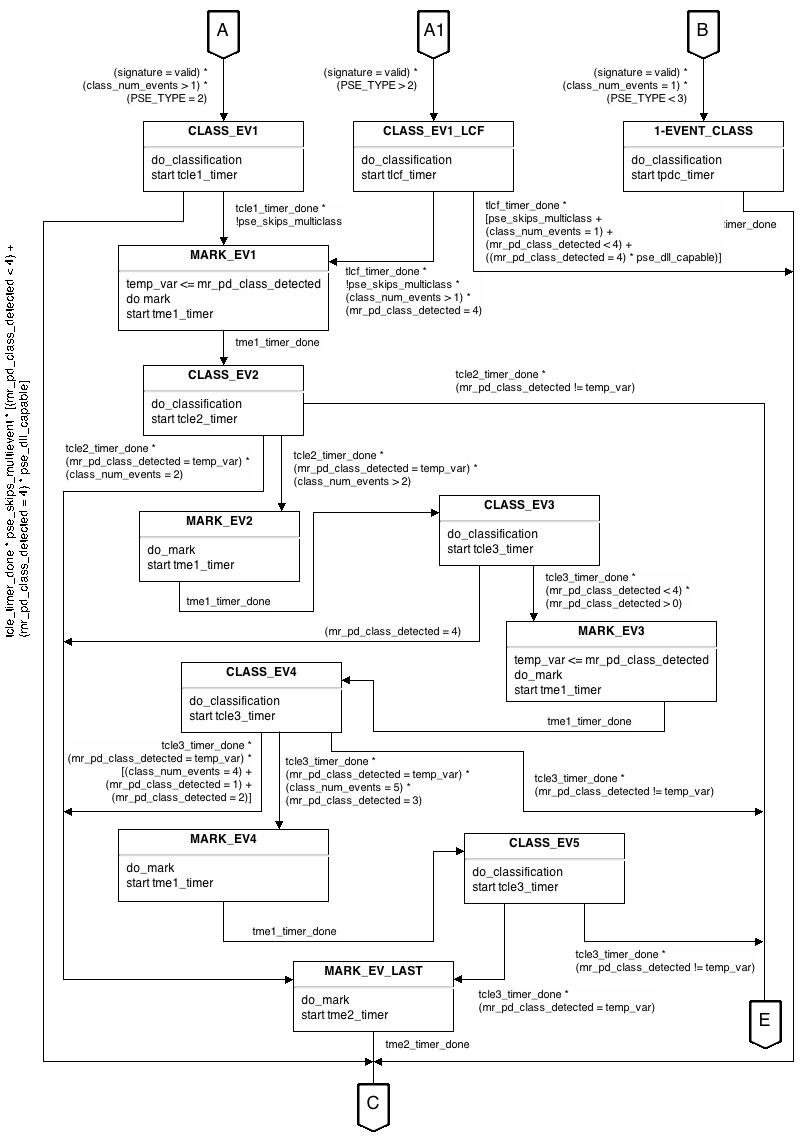
When a Type 3 PSE powers a Type 2 PD, the PSE shall meet the PI electrical requirements of a Type 2 PSE, but may choose to meet the electrical requirements of a Type 3 PSE for ICon, ILIM, TLIM, and PType , IInrush , ICUT (see Table 33–11).

When a Type 4 PSE powers a Type 1 PD, the PSE shall meet the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2, Type 3, or Type 4 PSE for ICon, ILIM, TLIM, and PType , IInrush , ICUT (see Table 33–11).

When a Type 4 PSE powers a Type 2 PD, the PSE shall meet the PI electrical requirements of a Type 2 PSE, but may choose to meet the electrical requirements of a Type 3 or Type 4 PSE for ICon, ILIM, TLIM, and PType , IInrush , ICUT (see Table 33–11).

When a Type 4 PSE powers a Type 3 PD, the PSE shall meet the PI electrical requirements of a Type 3 PSE, but may choose to meet the electrical requirements of a Type 4 PSE for ICon, ILIM, TLIM, and PType , IInrush , ICUT (see Table 33–11).

NOTE: This State Diagram is only representative of a single classification algorithm (single PD).

****

**Figure 33–9—PSE state diagram *(continued)***

**33.2.6 PSE classification of PDs and mutual identification**

The ability for the PSE to query the PD in order to determine the power requirements of that PD is called classification. The interrogation and power classification function is intended to establish mutual identification and is intended for use with advanced features such as power management.

Mutual identification is the mechanism that allows a Type 2, Type 3, or Type 4 PD to differentiate between Type 1, Type 2, Type3, and Type4 PSEs. Additionally, mutual identification allows a Type 2, Type 3, or Type 4 PSE to differentiate between Type 1, Type 2, Type 3, and Type 4 PDs. PDs or PSEs that do not implement classification will not be able to complete mutual identification and can only perform as Type 1 devices.

There are two forms of classification: Physical Layer classification and Data Link Layer classification.

Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto the PI and the PD responds with a current representing a limited number of power classifications. Based on the response of the PD, the minimum power level at the output of the PSE is *P*Class as shown in Equation (33–3). Physical Layer classification encompasses two methods, known as 1-Event Physical Layer classification (see 33.2.6.1) and Multiple-Event Physical Layer classification (see 33.2.6.2).

The minimum power output by the PSE for a particular PD class is defined by Equation (33–3). Alternatively, PSE implementations may use *V*PSE = VPort\_PSE min and *R*Chan = RCh max to arrive at over- margined values as shown in Table 33–7.

⎧ ⎛ –

2 – 4 × *R* × *P* ⎞ ⎫

= × *V*PSE *V*PSE----------------------C---h--a--n------------C---l-a--s--s-\_--P---D-

*P*Class

⎝

⎨ *V*PSE

⎩

⎜ ------------------------------ 2 × *R*

Chan

⎟ ⎬

⎠ ⎭W

(33–3)

where

*V*PSE is the voltage at the PSE PI as defined in 1.4

*R*Chan is the channel DC pair loop resistance

*P*Class\_PD is the PD’s power classification (see Table 33–18)

**Table 33–7—Physical Layer power classifications (*P*Class)**

|  |  |
| --- | --- |
| **Class** | **Minimum power levels at output of PSE (*P*Class)** |
| 0 | 15.4 Watts |
| 1 | 4.00 Watts |
| 2 | 7.00 Watts |
| 3 | 15.4 Watts |
| 4 | 30W or PType as defined in  Table 33–11, whichever is less |
| 5 (4/4/1) | 45W or PType as defined in  Table 33–11, whichever is less |
| 6 (4/4/2) | 60W or PType as defined in  Table 33–11, whichever is less |
| 7 (4/4/3) | PType as defined in  Table 33–11 |
| NOTE 1—This is the minimum power at the PSE PI. For maximum power available to PDs, see Table 33–18.  NOTE 2—Data Link Layer classification takes precedence over Physical Layer classification. | |

With Data Link Layer classification, the PSE and PD communicate using the Data Link Layer Protocol (see

33.6) after the data link is established. The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation.

A PSE shall meet one of the allowable classification permutations listed in Table 33–8.

Subsequent to successful detection, a Type 1 PSE may optionally classify a PD using 1-Event Physical Layer classification. Valid classification results are Classes 0, 1, 2, 3, and 4, as listed in Table 33–7. If a Type 1 PSE does not implement classification, then the Type 1 PSE shall assign all PDs to Class 0. A Type 1

PSE may optionally implement Data Link Layer classification.

**Table 33–8—PSE and PD classification permutations**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Permutations** | | | **PSE**  **allowed?** | **PD**  **allowed?** |
| **PSE/PD Type** | **Physical Layer classification** | **Data Link Layer classification** |
| Type 2, Type 3, or Type 4 | Multiple-Event | No | Yes | No |
| Yes | Yes | Yes |
| 1-Event | No | No1 | No |
| Yes | Yes | No |
| None | No | No | No |
| Yes | No | No |
| Type 1 | Multiple-Event | No | No | Yes |
| Yes | No | Yes |
| 1-Event | No | Yes | Yes |
| Yes | Yes | Yes |
| None | No | Yes | No |
| Yes | Yes | No |

NOTE 1—A Type 3 PSE that is limited to Type 1 power levels can be limited to 1-Event Physical Layer classification without required DLL capability.

Subsequent to successful detection, all Type 2, Type 3, and Type 4 PSEs perform classification using at least one of the following: Multiple-Event Physical Layer classification; Multiple-Event Physical Layer classification and Data Link Layer classification; or 1-Event Physical Layer classification and Data Link Layer classification.

If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall either return to the IDLE state or assign the PD to Class 0; a Type 2, Type 3, or Type 4 PSE shall return to the IDLE state.

**33.2.6.1 PSE 1-Event Physical Layer classification**

When 1-Event Physical Layer classification is implemented, classification consists of the application of VClass and the measurement of IClass in a single classification event—1-EVENT\_CLASS—as defined in the state diagram in Figure 33–9.

The PSE shall provide to the PI VClass with a current limitation of IClass\_LIM, as defined in Table 33–10. Polarity shall be the same as defined for VPort\_PSE in 33.2.3 and timing specifications shall be as defined by Tpdc in Table 33–10.

The PSE shall measure the resultant IClass and classify the PD based on the observed current according to

Table 33–9. All measurements of IClass shall be taken after the minimum relevant class event timing in Table

33–10. This measurement is referenced from the application of VClass min to ignore initial transients.

If the result of the class event is Class 4, a Type 1 PSE shall assign the PD to Class 0; a Type 2, Type 3, or Type 4 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the measured IClass is within the range of IClass\_LIM, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2, Type 3, or Type 4 PSE shall return to the IDLE state.

**33.2.6.2 PSE Multiple-Event Physical Layer classification**

When Multiple-Event Physical Layer classification is implemented, classification consists of the application of VClass and the measurement of IClass in a series of classification and mark events—CLASS\_EV1, MARK\_EV1, CLASS\_EV2, MARK\_EV2, CLASS\_EV3, MARK\_EV3, CLASS\_EV4, MARK\_EV4, CLASS\_EV5, and MARK\_EV\_LAST—as defined in the state diagram in Figure 33–9.

Type 2 PSEs shall provide a maximum of 2 class and 2 mark events. Type 3 PSEs shall provide a maximum of 4 class and 4 mark events. Type 4 PSEs shall provide a maximum of 5 class and 5 mark events.

A PSE in the state CLASS\_EV1 shall provide to the PI VClass as defined in Table 33–10. The timing specification shall be as defined by TCLE1 in Table 33–10 The PSE shall measure IClass and classify the PD based on the observed current according to Table 33–TBDA1.

A PSE in the state CLASS\_EV1\_LCF shall provide to the PI VClass as defined in Table 33–10. The timing specification shall be as defined by TLCF in Table 33–10. The PSE shall measure IClass and classify the PD based on the observed current according to Table 33–TBDA1.

When the PSE is in the state MARK\_EV1, the PSE shall provide to the PI VMark as defined in Table 33–10. The timing specification shall be as defined by TME1 in Table 33–10.

When the PSE is in the state CLASS\_EV2, the PSE shall provide to the PI VClass, subject to the TCLE2 timing specification, as defined in Table 33–10. The PSE shall measure IClass and classify the PD based on the observed current according to Table 33–TBDA1.

When the PSE is in the state MARK\_EV2, the PSE shall provide to the PI VMark as defined in Table 33–10. The timing specification shall be as defined by TME1 in Table 33–10.

When the PSE is in the state CLASS\_EV3, the PSE shall provide to the PI VClass, subject to the TCLE3 timing specification, as defined in Table 33–10. The PSE shall measure IClass and classify the PD based on the observed current according to Table 33–TBDA1.

When the PSE is in the state MARK\_EV3, the PSE shall provide to the PI VMark as defined in Table 33–10. The timing specification shall be as defined by TME1 in Table 33–10.

When the PSE is in the state CLASS\_EV4, the PSE shall provide to the PI VClass, subject to the TCLE3 timing specification, as defined in Table 33–10. The PSE shall measure IClass and classify the PD based on the observed current according to Table 33–TBDA1.

When the PSE is in the state MARK\_EV4, the PSE shall provide to the PI VMark as defined in Table 33–10. The timing specification shall be as defined by TME1 in Table 33–10.

When the PSE is in the state CLASS\_EV5, the PSE shall provide to the PI VClass, subject to the TCLE3 timing specification, as defined in Table 33–10. The PSE shall measure IClass and classify the PD based on the observed current according to Table 33–TBDA1.

When the PSE is in the state MARK\_EV\_LAST, the PSE shall provide to the PI VMark as defined in Table 33–10. The timing specification shall be as defined by TME2 in Table 33–10.

The mark event states, MARK\_EV1, MARK\_EV2, MARK\_EV3, MARK\_EV4, and MARK\_EV\_LAST, commence when the PI voltage falls below VClass min and end when the PI voltage exceeds VClass min. The VMark requirement is to be met with load currents in the range of IMark as defined in Table 33–17.

NOTE—In a properly operating system, the port may or may not discharge to the VMark range due to the combination of channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the VMark voltage. Discharge can be accomplished with a

2 mA load for 3 ms, after which VMark can be observed with minimum and maximum load current.

If any measured IClass is equal to or greater than IClass\_LIM min as defined in Table 33–10, a Type 2, Type3, or Type4 PSE shall return to the IDLE state. The class events shall meet the IClass\_LIM current limitation. The mark events shall meet the IMark\_LIM current limitation. All measurements of IClass shall be taken after the minimum relevant class event timing of Table 33–10. This measurement is referenced from the application of VClass min to ignore initial transients.

All class event voltages and mark event voltages shall have the same polarity as defined for VPort\_PSE in

33.2.3. The PSE shall complete Multiple-Event Physical Layer classification and transition to the POWER\_ON state without allowing the voltage at the PI to go below VMark min. If the PSE returns to the IDLE state, it shall maintain the PI voltage at VReset for a period of at least TReset min before starting a new detection cycle.

If the result of the first class event is Class 4, the PSE may omit the subsequent mark and class events only if the PSE implements Data Link Layer classification. In this case, a Type 2, Type 3, or Type 4 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the result of the first class event is any of Classes 0, 1, 2, or 3, a Type 2 PSE treats the PD as a Type 1 PD and may omit the subsequent mark and class events and classify the PD according to the result of the first class event. If the result of the first class event is any of Classes 0, 1, 2, or 3, a Type 3 or Type 4 PSE treats the PD as a Type 1 PD and shall omit the subsequent mark and class events and classify the PD according to the result of the first class event.

A Type 3 or Type 4 PSE shall skip all subsequent class events and transition directly to Mark\_EV\_LAST if the class signature detected during CLASS\_EV3 is 4. A Type 4 PSE shall skip MARK\_EV\_4 and CLASS\_EV5 and transition directly to Mark\_EV\_LAST if the class signature detected during CLASS\_EV4 is 1 or 2

**Table 33–9—PD classification**

|  |  |
| --- | --- |
| **Measured IClass** | **Classification** |
| 0 mA to 5.00 mA | Class 0 |
| > 5.00 mA and < 8.00 mA | May be Class 0 or 1 |
| 8.00 mA to 13.0 mA | Class 1 |
| > 13.0 mA and < 16.0 mA | Either Class 1 or 2 |
| 16.0 mA to 21.0 mA | Class 2 |
| > 21.0 mA and < 25.0 mA | Either Class 2 or 3 |
| 25.0 mA to 31.0 mA | Class 3 |
| > 31.0 mA and < 35.0 mA | Either Class 3 or 4 |
| 35.0 mA to 45.0 mA | Class 4 |
| > 45.0 mA and < 51.0 mA | Either Class 4 or invalid class |

NOTE—A Type 1 PSE may ignore IClass and report Class 0.

**Table 33–10—PSE Physical Layer classification electrical requirements**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Item** | **Parameter** | **Symbol** | **Units** | **Min** | **Max** | **1- or**  **Multiple-Event** | **Additional information** |
| 1 | Class event voltage | VClass | V | 15.5 | 20.5 | 1, Multiple |  |
| 2 | Class event current limitation | IClass\_LIM | A | 0.051 | 0.100 | 1, Multiple |  |
| 3 | Mark event voltage | VMark | V | 7.00 | 10.0 | Multiple |  |
| 4 | Mark event current limitation | IMark\_LIM | A | 0.005 | 0.100 | Multiple |  |
| 5 | 1st class event timing | TCLE1 | ms | 6.00 | 30.0 | Multiple |  |
| 6 | Mark event timing | TME1 | ms | 6.00 | 12.0 | Multiple |  |
| 7 | 2nd class event timing | TCLE2 | ms | 6.00 | 30.0 | Multiple |  |
| 8 | Final mark event timing | TME2 | ms | 6.00 |  | Multiple | Time from end of detection until power-on is limited  by 33.2.7.12. |
| 9 | Classification reset voltage | VReset | V | 0 | 2.80 | Multiple |  |
| 10 | Classification reset timing | TReset | ms | 15.0 |  | Multiple |  |
| 11 | 1-Event Physical Layer classification timing | Tpdc | ms | 6.00 | 75.0 | 1 |  |
| 12 | Long 1st class event timing | TLCF | ms | 85  (TBD) | 100  (TBD) | Multiple | Only applies to Type 3 and Type 4 PSEs. See 33.2.6.2. |
| 13 | 3rd-5th class event timing | TCLE3 | ms | 6.00 | 15 | Multiple | Only applies to Type 3 and Type 4 PSEs. See 33.2.6.2. |

**Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 12 | PSE Type power minimum | PType | W | ICable × (VPort\_PSE min) |  | 1, 2 | See 33.1.4. |
| ICable × (VPort\_PSE min) |  | 31 |
| 2 × ICable × (VPort\_PSE min) |  | 3 |
| 2 × ICable × (VPort\_PSE min) |  | 4 |

Note 1—A Type 3 PSE that chooses to limit itself to Type 1 or Type 2 power levels may use Type 1 or Type 2 system parameters respectively.