802.3 ca Contributions/Draft – COMMENTS

Adriaan de Lind van Wijngaarden, Nokia Bell Labs, Murray Hill

May 19, 2018

Description of the LDPC encoder and decoder – comments on the draft D1.0 clean, and han_3ca_1_0518.

[1] Draft D1.0 Clean, p. 54, L2-11:

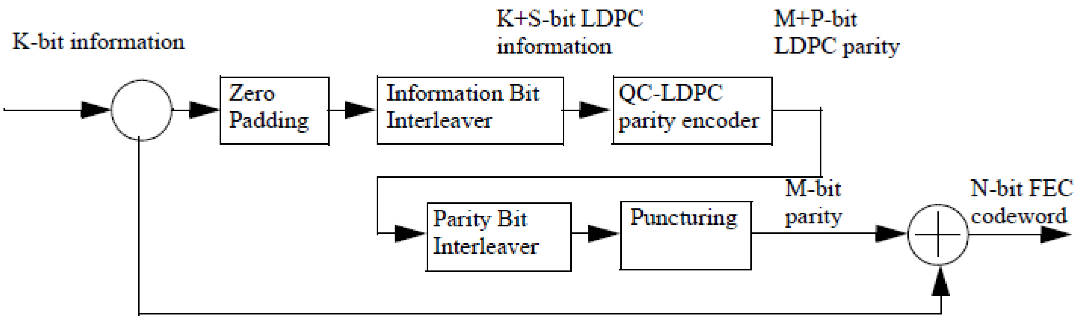

Figure 142–3—FEC encoder

Comment A1. If the puncturing of parity is standardized, and if 256-bit segments are used, then it is not clear why parity bits are first interleaved and then punctured. It seems more straightforward to puncture the two full 256-bit segments, and then to perform bit interleaving.

[2] Draft – D1.0 Clean, p.53, L27

The bit sequence input for a given code block to channel coding is denoted by $u_1, u_2, ..., u_K$, where K is the number of bits to be encoded. The parity check bit sequence produced by FEC Encoder is denoted by $p_1, p_2, ..., p_M$, where M is the number of parity check bits. The output of FEC Encoder is denoted by $c = [c_1, c_2, ..., c_N] = [u_1, u_2, ..., u_K \mid p_1, p_2, ..., p_M]$, where N = K + M is length of encoder output sequence.

Comment A2. It is important that the bit order for both the interleaver and the LDPC encoder is properly specified. The above (from draft D.0) may be ambiguous.

[3] Draft – D1.0 Clean, p.54, L33

where $a_{i,j} = -1$ for a zero sub-matrix in position (i,j), and a positive integer number $a_{i,j}$ defines the number of right column shifts of the identity matrix.

Comment A3. It may be an idea to further improve the description, and possibly provide an example. If the identity matrix is right-column shifted, I think this corresponds to a circular shift of a 256-bit segment to the left. We should also make sure how the information stream is being partitioned and indexed.

han_3ca_1_0518
LDPC Decoder

Figure x1 illustrates the receiver LDPC decoder with shortening/puncturing, interleaver/de-interleaver data path.

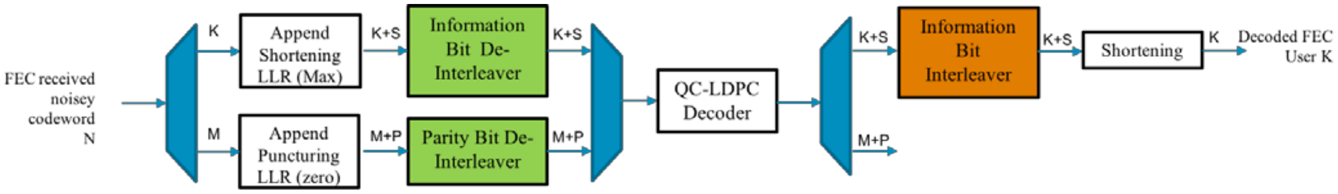
FEC received noisey codeword N
K
M
Append Shortening LLR (Max)
Append Puncturing LLR (zero)
K+S
M+P
Information Bit De-Interleaver
Parity Bit De-Interleaver
K+S
M+P
QC-LDPC Decoder
K+S
M+P
Information Bit Interleaver
K+S
Shortening
K
Decoded FEC User K

Figure x1 – FEC decoder

Comment A4. The FEC decoder figure in han_3ca_1_0518 should be improved; as shown in Fig. 142-3, the information bits are interleaved prior to entering the LDPC encoder, but they are transmitted non-interleaved. Therefore, the information portion of the received word should be "**interleaved**", and the (interleaved) information portion at the output of the LDPC decoder should be "**deinterleaved**".

Comment A5. There are several other inaccuracies in Fig. x1. For instance, "FEC received noisey codeword N" is a bit ambiguous. For the downstream direction, the length is indeed fixed, but for the upstream, it is not. I am not sure whether this will be described separately. In the upstream, one would need to know the length of the received word, and then append zeros after the information part. On the right-hand side, it is not clear whether the intention is to also output parity check bits (there is an arrow with (M+P) segments. It is also strange to reuse the parameter K in the label "Decoded FEC User K".

Comment A6. In the draft text (han_3ca_1_0518), an interleaver and de-interleaver is specified. It is recommended to provide the description of the information bit interleaver in/near the FEC encoder section, and the de-interleaver description near the FEC decoder section. The description itself is quite verbose, and it is ambiguous as well. A few issues:

- A so-called Omega network is used, which has been more succinctly described in the literature. One could start with such a definition, possibly parameterized, such that one can also describe a smaller example.
- The first paragraphs and Figure x2 concentrate on "reverse-omega networks" – one would expect a discussion of the interleaver first.
- The depiction of the data and deinterleaver in Fig. x2 is quite bulky and not very useful.
- The text below Fig. x2 mentions 12 interleavers for the parity segments, and, later, 10 seed values are specified in Table x3. Given that the eleventh and twelfth parity segments are punctured, it is better to state that the 10 256-bit parity segments are interleaved at the encoder, and deinterleaved at the decoder.
- Figures x3 and x4 are bulky.
- Figures x5 and x6 may be useful, but it would be good to better define the functionality and properly describe the example and the seed sequence used.
- The example sequences at the end of the section are not very helpful (a cyclic shift of a bit sequence by 17 and 34, respectively). It would be more useful to have sample hexadecimal input and output sequences for an interleaver (for several seed sequences).

.