Text and Tables in dark red font is for ref only, not to be included in the draft
Text in dark green font will need to be updated by the Editor (for links & cross-references) or comment.

# 45. Management Data Input/Output (MDIO) Interface

## 45.2 MDIO Interface Registers

**Table 45–1— MDIO Manageable Device addresses**

| Register Address | MMD Name | Clause |
|---|---|---|
| 0 | Reserved | |
| 1 | PMA/PMD | 45.2.1 |
| 2 | WIS | 45.2.2 |
| 3 | PCS | 45.2.3 |
| 4 | PHY XS | 45.2.4 |
| 5 | DTE XS | 45.2.5 |
| 6 | TC | 45.2.6 |
| 7 | Auto-Negotiation | 45.2.7 |
| 8 | Separated PMA (1) | |
| 9 | Separated PMA (2) | |
| 10 | Separated PMA (3) | |
| 11 | Separated PMA (4) | |
| 12 | OFDM PMA/PMD | 45.2.8 |
| 13 | Power Unit | 45.2.9 |
| 14 to 27 | Reserved | |
| 28 | PLCA | 45.2.13 |
| 29 | Clause 22 extension | 45.2.10 |
| 30 | Vendor specific 1 | 45.2.11 |
| 31 | Vendor specific 2 | 45.2.12 |

### 45.2.1 PMA/PMD registers

*Change the identified rows in Table 45-3 (as modified by IEEE Std 802.3cb-2018 and {IEEE Std 802.cd-TBD}) and insert new rows immediately below the changed rows as follows (unchanged rows not shown):*

**Table 45–3—PMA/PMD registers**

| Register Address | Title | Clause |
|---|---|---|
| 1.29 | ~~Reserved~~ PMA/PMD control 3 | 45.2.1.23a |
| 1.901 through 1.999 ~~1.1099~~ | Reserved | |
| 1.1000 through 1.1002 | Nx25G-EPON PMA/PMD extended ability | 45.2.1.134a |
| 1.1003 through 1.1099 | Reserved | |

*Insert 45.2.1.23a after 45.2.1.23 as follows:*

### 45.2.1.23a PMA/PMD control 3 register (Register 1.29)

The assignment of bits in the PMA/PMD control 3 register is shown in Table 45–26a.

45.2.1.23a PMA/PMD control 3 register (Register 1.29)

**Table 45–26a—PMA/PMD control 3 register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.29.15:6 | Reserved | Value always 0 | RO |
| 1.29.5:0 | PMA/PMD type selection | 543210<br>11xxxx = Reserved<br>101xxx = Reserved<br>100111 = 50GBASE-PQX-U3<br>100110 = 50GBASE-PQX-U2<br>100101 = 50GBASE-PQX-D3<br>100100 = 50GBASE-PQX-D2<br>100011 = 50GBASE-PQG-U3<br>100010 = 50GBASE-PQG-U2<br>100001 = 50GBASE-PQG-D3<br>100000 = 50GBASE-PQG-D2<br>011111 = 50/25GBASE-PQX-U3<br>011110 = 50/25GBASE-PQX-U2<br>011101 = 50/25GBASE-PQX-D3<br>011100 = 50/25GBASE-PQX-D2<br>011011 = 50/25GBASE-PQG-U3<br>011010 = 50/25GBASE-PQG-U2<br>011001 = 50/25GBASE-PQG-D3<br>011000 = 50/25GBASE-PQG-D2<br>010111 = 50/10GBASE-PQX-U3<br>010110 = 50/10GBASE-PQX-U2<br>010101 = 50/10GBASE-PQX-D3<br>010100 = 50/10GBASE-PQX-D2<br>010011 = 50/10GBASE-PQG-U3<br>010010 = 50/10GBASE-PQG-U2<br>010001 = 50/10GBASE-PQG-D3<br>010000 = 50/10GBASE-PQG-D2<br>001111 = 25GBASE-PQX-U3<br>001110 = 25GBASE-PQX-U2<br>001101 = 25GBASE-PQX-D3<br>001100 = 25GBASE-PQX-D2<br>001011 = 25GBASE-PQG-U3<br>001010 = 25GBASE-PQG-U2<br>001001 = 25GBASE-PQG-D3 | R/W |

| | | | |
|---|---|---|---|
| | | 001000 = 25GBASE-PQG-D2<br>000111 = 25/10GBASE-PQX-U3<br>000110 = 25/10GBASE-PQX-U2<br>000101 = 25/10GBASE-PQX-D3<br>000100 = 25/10GBASE-PQX-D2<br>000011 = 25/10GBASE-PQG-U3<br>000010 = 25/10GBASE-PQG-U2<br>000001 = 25/10GBASE-PQG-D3<br>000000 = 25/10GBASE-PQG-D2 | |

[a]R/W = Read/Write, RO = Read only

#### 45.2.1.23a.1 PMA/PMD type selection (1.29.5:0)

The PMA/PMD type of the PMA/PMD is selected using bits 5 to 0. The PMA/PMD type abilities of the PMA/PMD are advertised in the Nx25G-EPON PMA/PMD extended ability registers (Registers 1.1000 through 1.1002, see 45.2.1.134a). A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

*The above para is modeled after 45.2.1.6.3*

*Insert 45.2.1.134a after 45.2.1.134 as follows:*

### 45.2.1.134a Nx25G-EPON PMA/PMD extended ability register (Registers 1.1000 through 1.1002)

The assignment of bits in the Nx25G-EPON PMA/PMD extended ability register is shown in Table 45–103a.

**Table 45–103a—Nx25G-EPON PMA/PMD extended ability registers bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.1000.15 | 25GBASE-PQX-U3 | 1 = is 25GBASE-PQX-U3 compliant<br>0 = is not 25GBASE-PQX-U3 compliant | RO |
| 1.1000.14 | 25GBASE-PQX-U2 | 1 = is 25GBASE-PQX-U2 compliant<br>0 = is not 25GBASE-PQX-U2 compliant | RO |
| 1.1000.13 | 25GBASE-PQX-D3 | 1 = is 25GBASE-PQX-D3 compliant<br>0 = is not 25GBASE-PQX-D3 compliant | RO |
| 1.1000.12 | 25GBASE-PQX-D2 | 1 = is 25GBASE-PQX-D2 compliant<br>0 = is not 25GBASE-PQX-D2 compliant | RO |
| 1.1000.11 | 25GBASE-PQG-U3 | 1 = is 25GBASE-PQG-U3 compliant<br>0 = is not 25GBASE-PQG-U3 compliant | RO |
| 1.1000.10 | 25GBASE-PQG-U2 | 1 = is 25GBASE-PQG-U2 compliant<br>0 = is not 25GBASE-PQG-U2 compliant | RO |
| 1.1000.9 | 25GBASE-PQG-D3 | 1 = is 25GBASE-PQG-D3 compliant<br>0 = is not 25GBASE-PQG-D3 compliant | RO |
| 1.1000.8 | 25GBASE-PQG-D2 | 1 = is 25GBASE-PQG-D2 compliant<br>0 = is not 25GBASE-PQG-D2 compliant | RO |
| 1.1000.7 | 25/10GBASE-PQX-U3 | 1 = is 25/10GBASE-PQX-U3 compliant<br>0 = is not 25/10GBASE-PQX-U3 compliant | RO |
| 1.1000.6 | 25/10GBASE-PQX-U2 | 1 = is 25/10GBASE-PQX-U2 compliant<br>0 = is not 25/10GBASE-PQX-U2 compliant | RO |
| 1.1000.5 | 25/10GBASE-PQX-D3 | 1 = is 25/10GBASE-PQX-D3 compliant<br>0 = is not 25/10GBASE-PQX-D3 compliant | RO |
| 1.1000.4 | 25/10GBASE-PQX-D2 | 1 = is 25/10GBASE-PQX-D2 compliant<br>0 = is not 25/10GBASE-PQX-D2 compliant | RO |
| 1.1000.3 | 25/10GBASE-PQG-U3 | 1 = is 25/10GBASE-PQG-U3 compliant<br>0 = is not 25/10GBASE-PQG-U3 compliant | RO |
| 1.1000.2 | 25/10GBASE-PQG-U2 | 1 = is 25/10GBASE-PQG-U2 compliant<br>0 = is not 25/10GBASE-PQG-U2 compliant | RO |
| 1.1000.1 | 25/10GBASE-PQG-D3 | 1 = is 25/10GBASE-PQG-D3 compliant<br>0 = is not 25/10GBASE-PQG-D3 compliant | RO |
| 1.1000.0 | 25/10GBASE-PQG-D2 | 1 = is 25/10GBASE-PQG-D2 compliant<br>0 = is not 25/10GBASE-PQG-D2 compliant | RO |
| 1.1001.15 | 50/25GBASE-PQX-U3 | 1 = is 50/25GBASE-PQX-U3 compliant<br>0 = is not 50/25GBASE-PQX-U3 compliant | RO |
| 1.1001.14 | 50/25GBASE-PQX-U2 | 1 = is 50/25GBASE-PQX-U2 compliant<br>0 = is not 50/25GBASE-PQX-U2 compliant | RO |
| 1.1001.13 | 50/25GBASE-PQX-D3 | 1 = is 50/25GBASE-PQX-D3 compliant<br>0 = is not 50/25GBASE-PQX-D3 compliant | RO |
| 1.1001.12 | 50/25GBASE-PQX-D2 | 1 = is 50/25GBASE-PQX-D2 compliant<br>0 = is not 50/25GBASE-PQX-D2 compliant | RO |
| 1.1001.11 | 50/25GBASE-PQG-U3 | 1 = is 50/25GBASE-PQG-U3 compliant<br>0 = is not 50/25GBASE-PQG-U3 compliant | RO |

| | | | |
|---|---|---|---|
| 1.1001.10 | 50/25GBASE-PQG-U2 | 1 = is 50/25GBASE-PQG-U2 compliant<br>0 = is not 50/25GBASE-PQG-U2 compliant | RO |
| 1.1001.9 | 50/25GBASE-PQG-D3 | 1 = is 50/25GBASE-PQG-D3 compliant<br>0 = is not 50/25GBASE-PQG-D3 compliant | RO |
| 1.1001.8 | 50/25GBASE-PQG-D2 | 1 = is 50/25GBASE-PQG-D2 compliant<br>0 = is not 50/25GBASE-PQG-D2 compliant | RO |
| 1.1001.7 | 50/10GBASE-PQX-U3 | 1 = is 50/10GBASE-PQX-U3 compliant<br>0 = is not 50/10GBASE-PQX-U3 compliant | RO |
| 1.1001.6 | 50/10GBASE-PQX-U2 | 1 = is 50/10GBASE-PQX-U2 compliant<br>0 = is not 50/10GBASE-PQX-U2 compliant | RO |
| 1.1001.5 | 50/10GBASE-PQX-D3 | 1 = is 50/10GBASE-PQX-D3 compliant<br>0 = is not 50/10GBASE-PQX-D3 compliant | RO |
| 1.1001.4 | 50/10GBASE-PQX-D2 | 1 = is 50/10GBASE-PQX-D2 compliant<br>0 = is not 50/10GBASE-PQX-D2 compliant | RO |
| 1.1001.3 | 50/10GBASE-PQG-U3 | 1 = is 50/10GBASE-PQG-U3 compliant<br>0 = is not 50/10GBASE-PQG-U3 compliant | RO |
| 1.1001.2 | 50/10GBASE-PQG-U2 | 1 = is 50/10GBASE-PQG-U2 compliant<br>0 = is not 50/10GBASE-PQG-U2 compliant | RO |
| 1.1001.1 | 50/10GBASE-PQG-D3 | 1 = is 50/10GBASE-PQG-D3 compliant<br>0 = is not 50/10GBASE-PQG-D3 compliant | RO |
| 1.1001.0 | 50/10GBASE-PQG-D2 | 1 = is 50/10GBASE-PQG-D2 compliant<br>0 = is not 50/10GBASE-PQG-D2 compliant | RO |
| 1.1002.8:15 | Reserved | Value always 0 | RO |
| 1.1002.7 | 50GBASE-PQX-U3 | 1 = is 50GBASE-PQX-U3 compliant<br>0 = is not 50GBASE-PQX-U3 compliant | RO |
| 1.1002.6 | 50GBASE-PQX-U2 | 1 = is 50GBASE-PQX-U2 compliant<br>0 = is not 50GBASE-PQX-U2 compliant | RO |
| 1.1002.5 | 50GBASE-PQX-D3 | 1 = is 50GBASE-PQX-D3 compliant<br>0 = is not 50GBASE-PQX-D3 compliant | RO |
| 1.1002.4 | 50GBASE-PQX-D2 | 1 = is 50GBASE-PQX-D2 compliant<br>0 = is not 50GBASE-PQX-D2 compliant | RO |
| 1.1002.3 | 50GBASE-PQG-U3 | 1 = is 50GBASE-PQG-U3 compliant<br>0 = is not 50GBASE-PQG-U3 compliant | RO |
| 1.1002.2 | 50GBASE-PQG-U2 | 1 = is 50GBASE-PQG-U2 compliant<br>0 = is not 50GBASE-PQG-U2 compliant | RO |
| 1.1002.1 | 50GBASE-PQG-D3 | 1 = is 50GBASE-PQG-D3 compliant<br>0 = is not 50GBASE-PQG-D3 compliant | RO |
| 1.1002.0 | 50GBASE-PQG-D2 | 1 = is 50GBASE-PQG-D2 compliant<br>0 = is not 50GBASE-PQG-D2 compliant | RO |

[a]RO = Read only

*The paras below are modeled after 45.2.1.7.8.*

### 45.2.1.134a.1 25GBASE-PQX-U3 (1.1000.15)

When read as a one, bit 1.1000.15 indicates that the PMA/PMD is able to support a 25GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1000.15 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-U3 PMA/PMD type.

#### 45.2.1.134a.2 25GBASE-PQX-U2 (1.1000.14)

When read as a one, bit 1.1000.14 indicates that the PMA/PMD is able to support a 25GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1000.14 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.3 25GBASE-PQX-D3 (1.1000.13)

When read as a one, bit 1.1000.13 indicates that the PMA/PMD is able to support a 25GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1000.13 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.3 25GBASE-PQX-D2 (1.1000.12)

When read as a one, bit 1.1000.12 indicates that the PMA/PMD is able to support a 25GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1000.12 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.3 25GBASE-PQG-U3 (1.1000.11)

When read as a one, bit 1.1000.11 indicates that the PMA/PMD is able to support a 25GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1000.11 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.3 25GBASE-PQG-U2 (1.1000.10)

When read as a one, bit 1.1000.10 indicates that the PMA/PMD is able to support a 25GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1000.10 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-U2 PMA/PMD type.

#### 45.2.1.134a.3 25GBASE-PQG-D3 (1.1000.9)

When read as a one, bit 1.1000.9 indicates that the PMA/PMD is able to support a 25GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1000.9 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-D3 PMA/PMD type.

#### 45.2.1.134a.3 25GBASE-PQG-D2 (1.1000.8)

When read as a one, bit 1.1000.8 indicates that the PMA/PMD is able to support a 25GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1000.8 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-D2 PMA/PMD type.

#### 45.2.1.134a.3 25/10GBASE-PQX-U3 (1.1000.7)

When read as a one, bit 1.1000.7 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1000.7 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-U3 PMA/PMD type.

#### 45.2.1.134a.3 25/10GBASE-PQX-U2 (1.1000.6)

When read as a one, bit 1.1000.6 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1000.6 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.3 25/10GBASE-PQX-D3 (1.1000.5)

When read as a one, bit 1.1000.5 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1000.5 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.3 25/10GBASE-PQX-D2 (1.1000.4)

When read as a one, bit 1.1000.4 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1000.4 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.3 25/10GBASE-PQG-U3 (1.1000.3)

When read as a one, bit 1.1000.3 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1000.3 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.3 25/10GBASE-PQG-U2 (1.1000.2)

When read as a one, bit 1.1000.2 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1000.2 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-U2 PMA/PMD type.

#### 45.2.1.134a.3 25/10GBASE-PQG-D3 (1.1000.1)

When read as a one, bit 1.1000.1 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1000.1 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-D3 PMA/PMD type.

#### 45.2.1.134a.3 25/10GBASE-PQG-D2 (1.1000.0)

When read as a one, bit 1.1000.0 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1000.0 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-D2 PMA/PMD type.

#### 45.2.1.134a.3 50/25GBASE-PQX-U3 (1.1001.15)

When read as a one, bit 1.1001.15 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1001.15 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-U3 PMA/PMD type.

#### 45.2.1.134a.3 50/25GBASE-PQX-U2 (1.1001.14)

When read as a one, bit 1.1001.14 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1001.14 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.3 50/25GBASE-PQX-D3 (1.1001.13)

When read as a one, bit 1.1001.13 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1001.13 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.3 50/25GBASE-PQX-D2 (1.1001.12)

When read as a one, bit 1.1001.12 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1001.12 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.3 50/25GBASE-PQG-U3 (1.1001.11)

When read as a one, bit 1.1001.11 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1001.11 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.3 50/25GBASE-PQG-U2 (1.1001.10)

When read as a one, bit 1.1001.10 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1001.10 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-U2 PMA/PMD type.

#### 45.2.1.134a.3 50/25GBASE-PQG-D3 (1.1001.9)

When read as a one, bit 1.1001.9 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1001.9 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-D3 PMA/PMD type.

#### 45.2.1.134a.3 50/25GBASE-PQG-D2 (1.1001.8)

When read as a one, bit 1.1001.8 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1001.8 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-D2 PMA/PMD type.

#### 45.2.1.134a.3 50/10GBASE-PQX-U3 (1.1001.7)

When read as a one, bit 1.1001.7 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1001.7 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-U3 PMA/PMD type.

#### 45.2.1.134a.3 50/10GBASE-PQX-U2 (1.1001.6)

When read as a one, bit 1.1001.6 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1001.6 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.3 50/10GBASE-PQX-D3 (1.1001.5)

When read as a one, bit 1.1001.5 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1001.5 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.3 50/10GBASE-PQX-D2 (1.1001.4)

When read as a one, bit 1.1001.4 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1001.4 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.3 50/10GBASE-PQG-U3 (1.1001.3)

When read as a one, bit 1.1001.3 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1001.3 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.3 50/10GBASE-PQG-U2 (1.1001.2)

When read as a one, bit 1.1001.2 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1001.2 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-U2 PMA/PMD type.

#### 45.2.1.134a.3 50/10GBASE-PQG-D3 (1.1001.1)

When read as a one, bit 1.1001.1 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1001.1 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-D3 PMA/PMD type.

#### 45.2.1.134a.3 50/10GBASE-PQG-D2 (1.1001.0)

When read as a one, bit 1.1001.0 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1001.0 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-D2 PMA/PMD type.

#### 45.2.1.134a.3 50GBASE-PQX-U3 (1.1002.7)

When read as a one, bit 1.1002.7 indicates that the PMA/PMD is able to support a 50GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1002.7 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-U3 PMA/PMD type.

#### 45.2.1.134a.3 50GBASE-PQX-U2 (1.1002.6)

When read as a one, bit 1.1002.6 indicates that the PMA/PMD is able to support a 50GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1002.6 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.3 50GBASE-PQX-D3 (1.1002.5)

When read as a one, bit 1.1002.5 indicates that the PMA/PMD is able to support a 50GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1002.5 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.3 50GBASE-PQX-D2 (1.1002.4)

When read as a one, bit 1.1002.4 indicates that the PMA/PMD is able to support a 50GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1002.4 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.3 50GBASE-PQG-U3 (1.1002.3)

When read as a one, bit 1.1002.3 indicates that the PMA/PMD is able to support a 50GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1002.3 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.3 50GBASE-PQG-U2 (1.1002.2)

When read as a one, bit 1.1002.2 indicates that the PMA/PMD is able to support a 50GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1002.2 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-U2 PMA/PMD type.

#### 45.2.1.134a.3 50GBASE-PQG-D3 (1.1002.1)

When read as a one, bit 1.1002.1 indicates that the PMA/PMD is able to support a 50GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1002.1 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-D3 PMA/PMD type.

#### 45.2.1.134a.3 50GBASE-PQG-D2 (1.1002.0)

When read as a one, bit 1.1002.0 indicates that the PMA/PMD is able to support a 50GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1002.0 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-D2 PMA/PMD type.