Text and Tables in dark red font is for ref only, not to be included in the draft
Text in dark green font will need to be updated by the Editor (links & cross-references).

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

45.2.1 WIS registers

45.2.3 PCS registers

Change the identified rows in Table 45-176 (as modified by IEEE Std 802.3cb-2018) and insert new row as follows (unchanged rows not shown):

Table 45–176—PCS registers

Register address	Register name	Subclause
3.76, 3.77	10/1GBASE-PRX, ~~and~~ 10GBASE-PR, 10GBASE-Q, and 25GBASE-Q corrected FEC codewords counter	45.2.3.41
3.78, 3.79	10/1GBASE-PRX, ~~and~~ 10GBASE-PR, 10GBASE-Q, and 25GBASE-Q uncorrected FEC codewords counter	45.2.3.42
3.83 through 3.135	Nx25G-EPON synchronization pattern	45.2.1.45a
~~3.83~~ 3.136 through 3.199	Reserved	

45.2.3.1 PCS control 1 register (Register 3.0)

Change the identified row in Table 45-177 (as modified {IEEE Std 802.cd-TBD}) as follows (unchanged rows not shown):

Table 45–177—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.5:2	Speed selection	5432 11xx = Reserved 1011 = 25/10 Gb/s ~~Reserved~~ 1010 = 400 Gb/s 1001 = 200 Gb/s 1000 = 5 Gb/s 0111 = 2.5 Gb/s 0110 = 50 Gb/s 0101 = 25 Gb/s 0100 = 100 Gb/s 0011 = 40 Gb/s 0010 = 10/1 Gb/s 0001 = 10PASS-TS/2BASE-TL 0000 = 10 Gb/s	R/W

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.6 PCS control 2 register (Register 3.7)

Change the identified rows in Table 45-180 (as modified by IEEE Std 802.3cb-2018 and {IEEE Std 802.cd-TBD}) as follows (unchanged rows not shown):

45.2.3.6 PCS control 2 register (Register 3.7)

Table 45–180—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
~~3.7.15:4~~ 3.7.15:5	Reserved	Value always 0	RO
~~3.7.3:0~~ 3.7.4:0	PCS type selection	~~3210~~ 43210 11xxx = reserved 101xx = reserved 1001x = reserved 10001 = Select 25GBASE-Q PCS type 10000 = Select 25/10GBASE-Q PCS type 01111 = Select 5GBASE-R PCS type 01110 = Select 2.5GBASE-X PCS type 01101 = Select 400GBASE-R PCS type 01100 = Select 200GBASE-R PCS type 01011 = Select 5GBASE-T PCS type 01010 = Select 2.5GBASE-T PCS type 01001 = Select 25GBASE-T PCS type 01000 = Select 50GBASE-R PCS type 00111 = Select 25GBASE-R PCS type 00110 = Select 40GBASE-T PCS type 00101 = Select 100GBASE-R PCS type 00100 = Select 40GBASE-R PCS type 00011 = Select 10GBASE-T PCS type 00010 = Select 10GBASE-W PCS type 00001 = Select 10GBASE-X PCS type 00000 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

Change subclause 45.2.3.6.1 as follows:

45.2.3.6.1 PCS type selection (~~3.7.3:0~~ 3.7.4:0)

The PCS type shall be selected using bits ~~3~~4 through 0. The PCS type abilities of the PCS are advertised in bits 3.8.9, 3.8.7:0, and 3.9.1:0 3.9.5:0. A PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the PCS status 2 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

45.2.3.8 PCS status 3 register (Register 3.9)

Change the identified rows in Table 45-182 (as modified by IEEE Std 802.3cb-2018) and insert new row as follows (unchanged rows not shown):

Table 45–182—PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
~~3.9.15:4~~ 3.9.15:6	Reserved	Value always 0	RO
3.9.5	25GBASE-Q capable	1 = PCS is able to support 25GBASE-Q PCS type 0 = PCS is not able to support 25GBASE-Q PCS type	RO
3.9.4	10GBASE-Q capable	1 = PCS is able to support10GBASE-Q PCS type 0 = PCS is not able to support 10GBASE-Q PCS type	RO

[a]RO = Read only

Insert 45.2.3.8.aa and 45.2.3.8.ab (before 45.2.3.8.a as modified by IEEE Std 802.3cb-2018) as follows.

45.2.3.8.aa 25GBASE-Q capable (3.9.5)

When read as a one, bit 3.9.5 indicates that the PCS is able to support the 25GBASE-Q PCS type. When read as a zero, bit 3.9.5 indicates that the PCS is not able to support the 25GBASE-Q PCS type.

45.2.3.8.ab 10GBASE-Q capable (3.9.4)

When read as a one, bit 3.9.4 indicates that the PCS is able to support the 10GBASE-Q PCS type. When read as a zero, bit 3.9.4 indicates that the PCS is not able to support the 10GBASE-Q PCS type.

Change 45.2.3.41, 45.2.3.42 and associated table titles as follows:

45.2.3.41 10/1GBASE-PRX, ~~and~~ 10GBASE-PR, 10GBASE-Q, and 25GBASE-Q corrected FEC codewords counter (Register 3.76, 3.77)

The assignment of bits in the 10/1GBASE-PRX, ~~and~~ 10GBASE-PR, 10GBASE-Q, and 25GBASE-Q corrected FEC codewords counter register is shown in Table 45–213. See 76.3.3.3.2 for a definition of ~~this~~ the 10/1GBASE-PRX and 10GBASE-PR counters and 142.3.4 for the definition of the 10GBASE-Q, and 25GBASE-Q counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–213—10GBASE-PR and 25GBASE-Q corrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.76.15:0	corrected FEC codewords lower	corrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.77.15:0	corrected FEC codewords upper	corrected_FEC_codewords_counter[31:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.42 10/1GBASE-PRX, ~~and~~ 10GBASE-PR, 10GBASE-Q, and 25GBASE-Q uncorrected FEC codewords counter (Register 3.78, 3.79)

The assignment of bits in the 10/1GBASE-PRX, ~~and~~ 10GBASE-PR, 10GBASE-Q, and 25GBASE-Q uncorrected FEC codewords counter register is shown in Table 45–214. See 76.3.3.3.2 for a definition of ~~this~~ the 10/1GBASE-PRX and 10GBASE-PR counters and 142.3.4 for the definition of the 10GBASE-Q, and 25GBASE-Q counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–214—10GBASE-P and 25GBASE-Q uncorrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.78.15:0	uncorrected FEC codewords lower	uncorrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.79.15:0	uncorrected FEC codewords upper	uncorrected_FEC_codewords_counter[31:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

Insert 45.2.3.45a, associated Tables and subclauses after 45.2.3.45 as follows:

45.2.3.45a Nx25G-EPON synchronization pattern registers (Registers 3.83 through 3.134)

The assignment of bits in registers 3.83 through 3.134 is shown in Table 45–217a. The Nx25G-EPON synchronization pattern (see 142.1.3 and 144.3.4.7) is used in the upstream data transmissions to facilitate the OLT in locking to the incoming data burst.

Table 45–217a—Nx25G-EPON synchronization pattern registers bit definitions

Bit(s)	Name	Description	R/W[a]
3.83.0	SP1 balanced	Balance setting for SP1	R/W
3.83.1	SP1 bit 257	The MSB of the 257-bit SP1	R/W
3.83.2	SP2 balanced	Balance setting for SP2	R/W
3.83.3	SP2 bit 257	The MSB of the 257-bit SP2	R/W
3.83.4	SP3 balanced	Balance setting for SP3	R/W
3.83.5	SP3 bit 257	The MSB of the 257-bit SP3	R/W
3.84.0 through 3.99.15	SP1 pattern	The lower 256 bits of SP1	R/W
3.100.0:15	SP1 length	The number of times SP1 is to be repeated	R/W
3.101.0 through 3.116.15	SP2 pattern	The lower 256 bits of SP2	R/W
3.117.0:15	SP2 length	The number of times SP2 is to be repeated	R/W
3.118.0 through 3.133.15	SP3 pattern	The lower 256 bits of SP3	R/W
3.134.0:15	SP3 length	The number of times SP3 is to be repeated	R/W

[a]R/W = Read/Write, RO = Read only

45.2.3.45a.1 SP3 bit 257 (3.83.5)

In the Nx25G PCS, bit 3.83.5 indicates the value to be used for the 257th bit of SP3. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.2 SP3 balanced (3.83.4)

In the Nx25G PCS, bit 3.83.4 indicates that repeating SP3 synchronization patterns are to have a balanced number of one and zero bits transmitted. When bit this bit is set to a zero then SP3 is to remain unbalanced, i.e., SP3 is always transmitted using the values from 3.83.5 and 3.118.0 through 3.133.15. When this bit is set to a one SP3 is to be balanced, i.e., each 257-bit block of SP3 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.3 SP2 bit 257 (3.83.3)

In the Nx25G PCS, bit 3.83.3 indicates the value to be used for the 257th bit of SP2. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.4 SP2 balanced (3.83.2)

In the Nx25G PCS, bit 3.83.2 indicates that repeating SP2 synchronization patterns are to have a balanced number of one and zero bits transmitted. When bit this bit is set to a zero then SP2 is to remain unbalanced, i.e., SP2 is always transmitted using the values from 3.83.3 and 3.101.0 through 3.116.15. When this bit is set to a one SP2 is to be balanced, i.e., each 257-bit block of SP2 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.5 SP1 bit 257 (3.83.1)

In the Nx25G PCS, bit 3.83.1 indicates the value to be used for the 257th bit of SP1. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.6 SP1 balanced (3.83.0)

In the Nx25G PCS, bit 3.83.0 indicates that repeating SP1 synchronization patterns are to have a balanced number of one and zero bits transmitted. When bit this bit is set to a zero then SP1 is to remain unbalanced, i.e., SP1 is always transmitted using the values from 3.83.1 and 3.84.0 through 3.99.15. When this bit is set to a one SP1 is to be balanced, i.e., each 257-bit block of SP1 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.7 SP1 pattern (3.84.0 through 3.99.15)

In the Nx25G PCS, bits 3.84.0 through 3.99.15indicate the value to be used for the lower 256 bit of the initial SP1 transmitted in a burst. If present, subsequent transmissions of the lower 256 bit of SP1 are determined by bit 3.83.0. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.8 SP1 length (3.100.0:15)

In the Nx25G PCS, bits 3.100.0:15 indicate the number of times the 257 bit SP1 is transmitted in a given burst. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.9 SP2 pattern (3.101.0 through 3.116.15)

In the Nx25G PCS, bits 3.101.0 through 3.116.15indicate the value to be used for the lower 256 bit of the initial SP2 transmitted in a burst. If present, subsequent transmissions of the lower 256 bit of SP2 are determined by bit 3.100.0:15. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.10 SP2 length (3.117.0:15)

In the Nx25G PCS, bits 3.117.0:15 indicate the number of times the 257 bit SP2 is transmitted in a given burst. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.11 SP3 pattern (3.118.0 through 3.133.15)

In the Nx25G PCS, bits 3.118.0 through 3.133.15indicate the value to be used for the lower 256 bit of the initial SP3 transmitted in a burst. If present, subsequent transmissions of the lower 256 bit of SP3 are determined by bit 3.117.0:15. See 142.1.3 and 144.3.4.7 for additional details.

45.2.3.45a.12 SP3 length (3.134.0:15)

In the Nx25G PCS, bits 3.134.0:15 indicate the number of times the 257 bit SP3 is transmitted in a given burst. See 142.1.3 and 144.3.4.7 for additional details.