MDIO interface for PCS

Motivation

- During the call on 12/?? It was pointed out that, because we consider a PCS to be a single channel entity, there exists a possibility to implement a multi-channel Nx25G EPON system using separate PCS devices
  - If this is done it implies that each device would have the same Cl 45 address space

MDIO (per Cl 22.2.4.5)

Table 22–12—Management frame format

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

- Basic MDIO frame structure (ref. in 45.1.1)
  - PRE: preamble, all 1's
  - ST: Start of frame
  - OP: Operation (R/W)
  - PHYAD: Phy Address (allows addressing up to 32 Phys on a single MDIO
  - REGAD: Register Address (up to 32 registers)
  - TA: turnaround (time for slave to switch from rx to tx)
  - DATA: data for register

Cl 45 MDIO extensions

Table 45–352—Extensions to management frame format for indirect access

	Management frame fields							
Frame	PRE	ST	OP	PRTAD	DEVAD	TA	ADDRESS / DATA	IDLE
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDI	
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDI	
Post-read-increment-address	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDI	

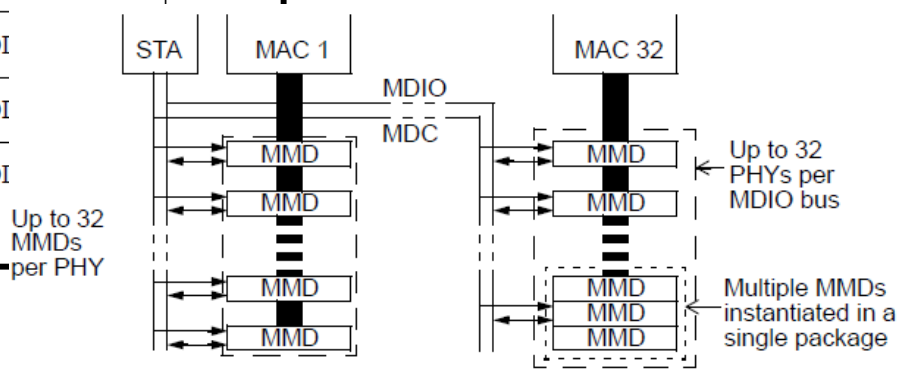
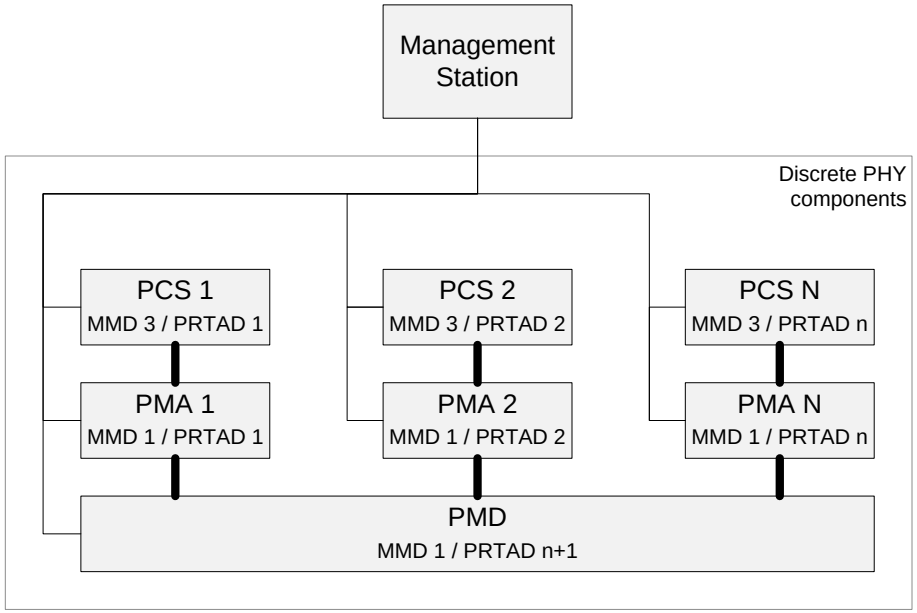
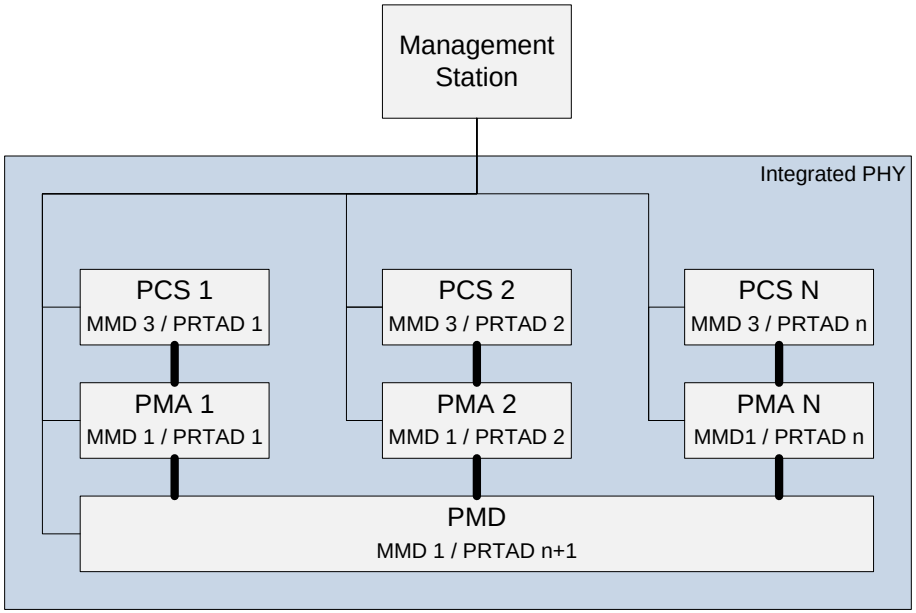


Figure 45-1—DTE and MMD devices

- OP – expanded
  - 00 – frame includes Register Address,
  - 01 – data for previously addressed register (from 00 frame)
  - 10 – read operation
  - 11 – post-read-increment-address operation
- PRTAD – Port Address (up to 32 Ports)
- DEVAD – Device Address (up to 32 Devices) in Cl 45 == MMD
- ADDRESS/DATA: depending on OP
- A very informative ref (see slide 10 in particular):
  http://www.ieee802.org/3/efm/public/nov02/oam/pannell_oam_1_1102.pdf

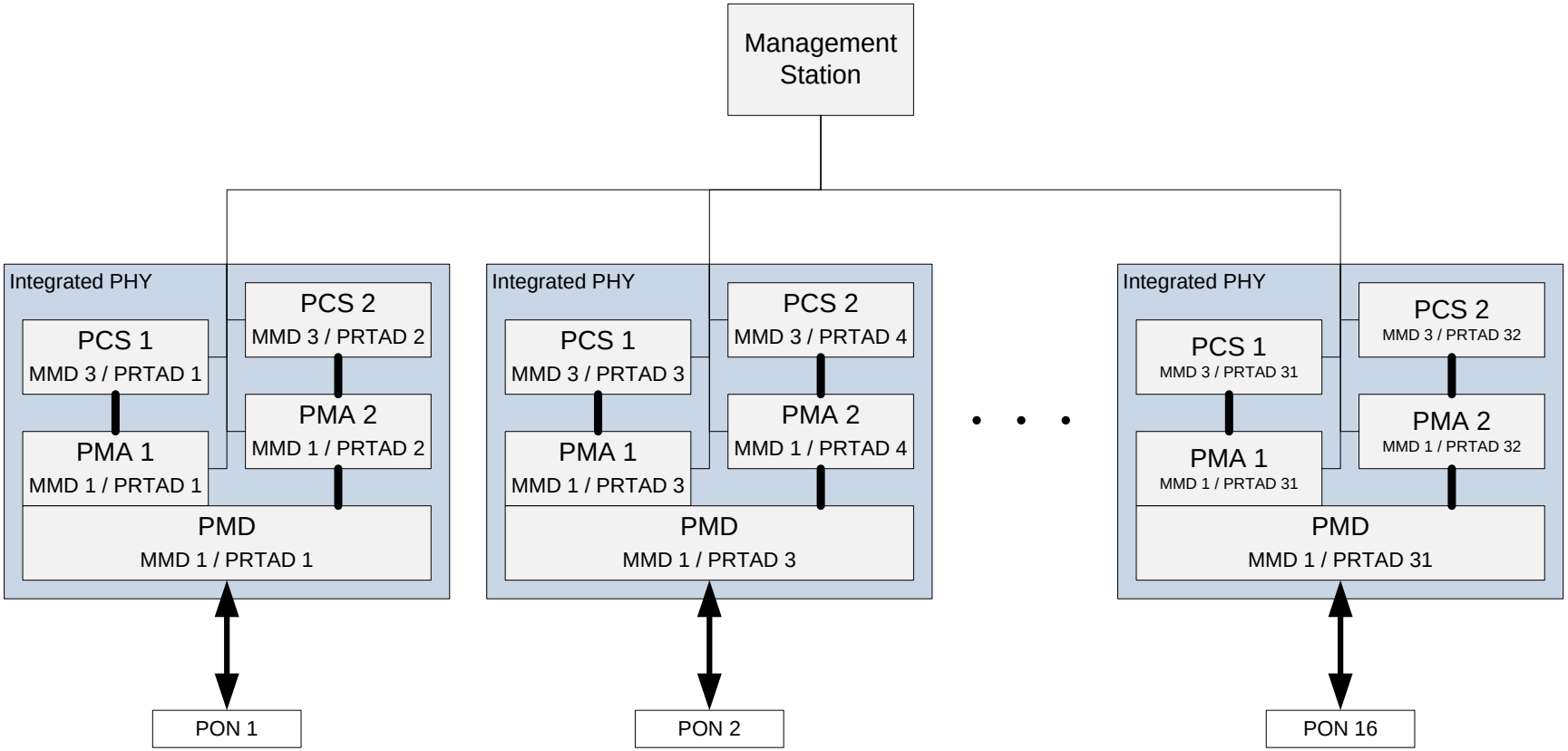
802.3ca – discrete/integrated PHY





- Use PRTAD to distinguish channel/layer in both cases
- Each channel PCS/PMA uses the same register address space

IMPLEMENTATION w/ 16 PONs



Cl 45 PCS changes

- Modify registers 3.0, 3.7, 3.9, & 3.76-3.79
- Add registers 3.83-3.135

45.2.3 PCS registers

Table 45–176—PCS registers

Register address	Register name	Subclaus
3.0	PCS control 1	45.2.3.1
3.7	PCS control 2	45.2.3.6
3.9	PCS status 3	45.2.3.8
3.76, 3.77	10/1GBASE-PRX, ~~and~~ 10GBASE-PR, 10GBASE-Q, and 25GBASE-Q corrected FEC codewords counter	45.2.3.41
3.78, 3.79	10/1GBASE-PRX, ~~and~~ 10GBASE-PR, 10GBASE-Q, and 25GBASE-Q uncorrected FEC codewords counter	45.2.3.42
3.80	10GBASE-PR and 10/1GBASE-PRX BER monitor timer control	45.2.3.43
3.81	10GBASE-PR and 10/1GBASE-PRX BER monitor status	45.2.3.44
3.82	10GBASE-PR and 10/1GBASE-PRX BER monitor threshold control	45.2.3.45
3.83 through 3.135	Nx25G-EPON Synchronization Pattern	45.2.1.192
~~3.83~~ 3.136 through 3.199	Reserved	

Table 45-177

- Modify table to add 25/10G speed selection

45.2.3.1 PCS control 1 register (Register 3.0)

Table 45–177—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.5:2	Speed selection	5432 11xx = Reserved	R/W
		1011 = 25/10 Gb/s ~~Reserved~~	
		1010 = 400 Gb/s	
		1001 = 200 Gb/s	
		1000 = 5 Gb/s	
		0111 = 2.5 Gb/s	
		0110 = 50 Gb/s	
		0101 = 25 Gb/s	
		0100 = 100 Gb/s	
		0011 = 40 Gb/s	
		0010 = 10/1 Gb/s	
		0001 = 10PASS-TS/2BASE-TL	
		0000 = 10 Gb/s	

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

Table 45-180

- Modify table to add selection for 25GBASE-Q or 10GBASE-Q PCS types

45.2.3.6 PCS control 2 register (Register 3.7)

Table 45–180—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
~~3.7.15:4~~ 3.7.15:5	Reserved	Value always 0	RO
~~3.7.3:0~~ 3.7.4:0	PCS type selection	~~3210~~ 43210	R/W
		11xxx = reserved	
		101xx = reserved	
		1001x = reserved	
		10001 = Select 25GBASE-Q PCS type	
		10000 = Select 25/10GBASE-Q PCS type	
		01111 = Select 5GBASE-R PCS type	
		01110 = Select 2.5GBASE-X PCS type	
		01101 = Select 400GBASE-R PCS type	
		01100 = Select 200GBASE-R PCS type	
		01011 = Select 5GBASE-T PCS type	
		01010 = Select 2.5GBASE-T PCS type	
		01001 = Select 25GBASE-T PCS type	
		01000 = Select 50GBASE-R PCS type	
		00111 = Select 25GBASE-R PCS type	
		00110 = Select 40GBASE-T PCS type	
		00101 = Select 100GBASE-R PCS type	
		00100 = Select 40GBASE-R PCS type	
		00011 = Select 10GBASE-T PCS type	
		00010 = Select 10GBASE-W PCS type	
		00001 = Select 10GBASE-X PCS type	
		00000 = Select 10GBASE-R PCS type	

[a]RO = Read only, R/W = Read/Write

Table 45-182

- Modify table to add 25GBASE-Q and 10GBASE-Q PCS types

45.2.3.8 PCS status 3 register (Register 3.9)

Table 45–182—PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
~~3.9.15:2~~ 3.9.15:4	Reserved	Value always 0	RO
3.9.3	25GBASE-Q capable	1 = PCS is able to support 25GBASE-Q PCS type 0 = PCS is not able to support 25GBASE-Q PCS type	RO
3.9.2	10GBASE-Q capable	1 = PCS is able to support10GBASE-Q PCS type 0 = PCS is not able to support 10GBASE-Q PCS type	RO
3.9.1	400GBASE-R capable	1 = PCS is able to support 400GBASE-R PCS type 0 = PCS is not able to support 400GBASE-R PCS type	RO
3.9.0	200GBASE-R capable	1 = PCS is able to support 200GBASE-R PCS type 0 = PCS is not able to support 200GBASE-R PCS type	RO

aRO = Read only

Table 45-217a

- Add new table for Sync Pattern

45.2.3.45a Nx25G-EPON Synchronization pattern registers (Registers 3.xx through 3.yy)

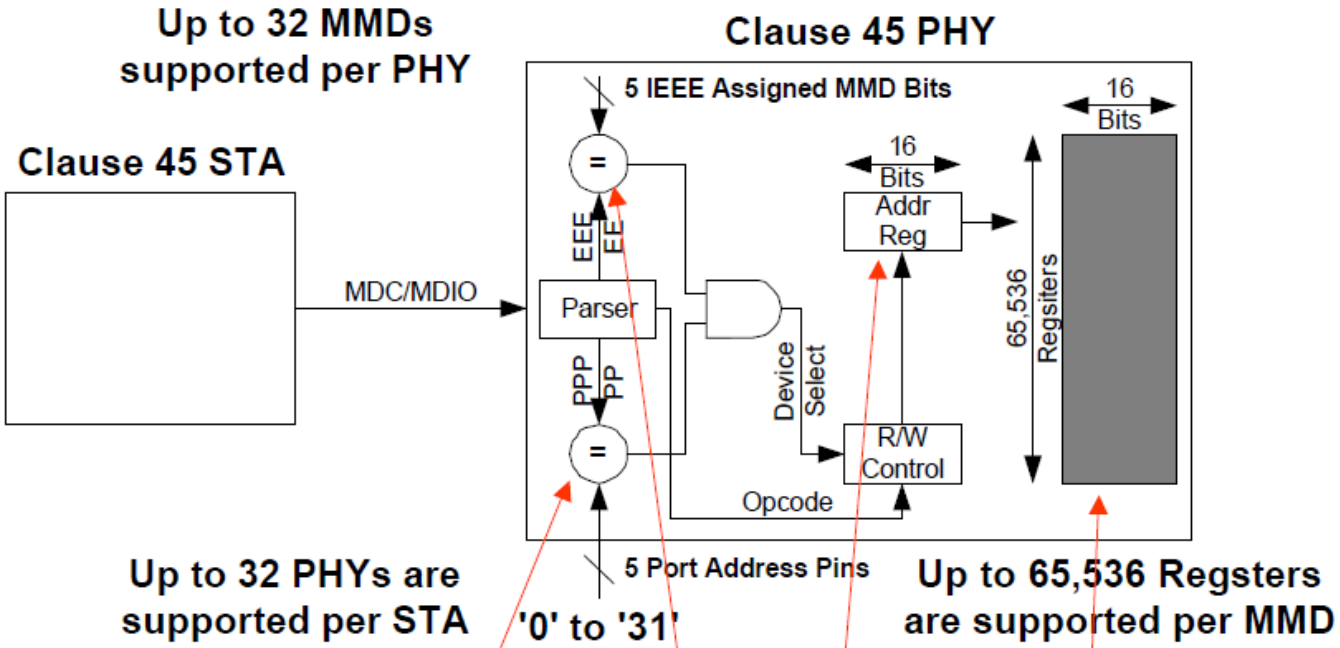
Table 45–217a—Nx25G-EPON Synchronization pattern registers bit definitions

Bit(s)	Name	Description	R/W[a]
3.83.0	SP1 balanced	Balance setting for SP1	R/W
3.83.1	SP1 bit 257	The MSB of the 257-bit SP1	R/W
3.83.2	SP2 balanced	Balance setting for SP2	R/W
3.83.3	SP2 bit 257	The MSB of the 257-bit SP2	R/W
3.83.4	SP3 balanced	Balance setting for SP3	R/W
3.83.5	SP3 bit 257	The MSB of the 257-bit SP3	R/W
3.84.0 through 3.99.15	SP1 pattern	The lower 256 bits of SP1	R/W
3.100.0:15	SP1 length	The number of times SP1 is to be repeated	R/W
3.101.0 through 3.116.15	SP2 pattern	The lower 256 bits of SP2	R/W
3.117.0:15	SP2 length	The number of times SP2 is to be repeated	R/W
3.118.0 through 3.133.15	SP3 pattern	The lower 256 bits of SP3	R/W
3.134.0:15	SP3 length	The number of times SP3 is to be repeated	R/W

[a]R/W = Read/Write, RO = Read only

Thank you

Clause 45 STA & PHY



	Management Frame Fields - Clause 45							
Frame	PRE	ST	OP	PRTAD	DEVAD	TA	DATA	IDLE
Address	1 . . .1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1 . . .1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1 . . .1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Read Inc.	1 . . .1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

10