Cl **46** *SC* **46.3.3.3** *P* **45** *L* **14** # r02-1

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

The text inserted here is about "a 2.5GBASE-X MAC/RS implementation". But a MAC/RS is generic, not specific to 2.5GBASE-X; as stated in 125.1.3, 2.5GBASE-X is "a family of Physical Layer implementations". and per 1.4.372 the PHY is between the MDI and the GMII. So, the term "2.5GBASE-X MAC/RS" should be corrected.

SuggestedRemedy

Change "a 2.5GBASE-X MAC/RS implementation " to "a 2.5 Gb/s MAC/RS implementation connected to a 2.5GBASE-X PHY".

Response *Response Status* **W**

ACCEPT.

Cl **130** *SC* **130.7.1.4** *P* **149** *L* **46** # r02-4

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

In all other PMD clauses, both the maximum and minimum voltages are tested under the same conditions, including with the same test pattern, since the test establishes the limits of the same parameter.

See for example 70.7.1.5, 71.7.1.4, 72.7.1.11, and 85.8.3.3.

I see no reason to deviate from precedence and use different patterns for minimum and maximum.

SuggestedRemedy

Change FROM "The maximum differential output voltage test pattern" TO "The differential output voltage test pattern".

Delete the next sentence about the minimum differential voltage test pattern.

Apply corresponding changes in PICS.

Response *Response Status* **W**

ACCEPT.

Cl **128** *SC* **128.7.1.4** *P* **115** *L* **50** # r02-5

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

"the square wave test pattern defined in 52.9.1.2, with a run of at least eight consecutive ones followed by an equal number of consecutive zeros"

This PMD is used with an 8B/10B PCS. This PCS can't generate pattern with a run longer than 5 bits. It should not be tested with a signal of eight or more bits, since it does not represent voltages expected in actual traffic. Also, there is no defined way to generate such a pattern.

The similar PMDs in clauses 70 and 71 use the test patterns in 36A.2 and 48A.2 respectively. These test patterns can be generated by the PCS and will create the voltages expected with actual traffic.

Also, in all other PMD clauses, both the maximum and minimum voltages are tested with the same test pattern, since the test establishes the limits of the same parameter. I see no reason to deviate from precedence and use different patterns for minimum and maximum.

48A.2 is suitable for 3.125 GBd as used in this clause.

SuggestedRemedy

Change FROM
"The maximum differential output voltage test pattern is the square wave test pattern defined in 52.9.1.2, with a run of at least eight consecutive ones followed by an equal number of consecutive zeros"
TO
"The differential output voltage test pattern is the test pattern specified in 48A.2".

Delete the next sentence about the minimum differential voltage test pattern.

Apply corresponding changes in PICS.

Response *Response Status* **W**

ACCEPT.

Cl **128** *SC* **128.7.2.1** *P* **119** *L* **26** # r02-10

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

The test pattern in 48A.4 (CRPAT) is defined there as "This pattern is not intended for jitter compliance testing". There is another test pattern which is intended for compliance testing, in 48A.5 (CJPAT).

The received interference tolerance test in the similar PMD in clause 71 is performed with CJPAT (see 71.7.2.1) and with the same method used here (Annex 69A). For consistency, this pattern should be used here too.

SuggestedRemedy

Change "48A.4" to "48A.5".

Response *Response Status* **W**

ACCEPT.

Cl **128** *SC* **128.7.2.5** *P* **120** *L* **24** # r02-11

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

"This differential input return loss requirement applies to all valid input levels"

This sentence is a residue from the similar text in the transmitter, but it is meaningless for the receiver; The receiver does not generate an "input level" the way a transmitter generates an "output level".

This text does not appear in recent receiver specifications (from clause 93 and on). It should be removed here to reduce maintenance activity.

Also in 130.7.2.5.

SuggestedRemedy

Delete the quoted sentence from both places.

Response *Response Status* **W**

ACCEPT.

Cl **128** *SC* **128.7.1.8** *P* **118** *L* **36** # r02-13

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **R**

*** Field CommentType updated on 12/15/2017 from T to TR ***
"The data pattern for jitter measurements shall be a low-frequency test pattern as defined in 48A.2"

This data pattern is a square wave, so the measurement will not include any data-dependent jitter (due to ISI or transmitter limited bandwidth).

This is fine if there are other specifications that limit the transmitter's ISI, but I don't see any such specifications in this clause.

Receiver tests are performed with a lossy channel but not with a lossy transmitter. This may lead to lack of interoperability.

To prevent a transmitter with high ISI/DDJ/loss, the transmit jitter should be measured with a frequency-rich signal such as CJPAT (48A.5). This is specified in the similar clause 71. The jitter specification limits should also be similar to those of clause 71.

SuggestedRemedy

Change "low-frequency test pattern as defined in 48A.2" to "jitter tolerance test pattern defined in Annex 48A.5".

Change the jitter maximum values in Table 128-4 to be equal to the ones in Table 71-4.

Apply corresponding changes in PICS.

Response *Response Status* **W**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **130** *SC* **130.10.4.2** *P* **158** *L* **50** # r02-15

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

Mismatch between delay limits in PICS and in the referenced subclause

SuggestedRemedy

change 256 to 1024

Response *Response Status* **W**

ACCEPT.

Cl **30** *SC* **30.3.2.1.2** *P* **31** *L* **18** # r02-21

Marris, Arthur — Cadence Design Syst

Comment Type **ER** *Comment Status* **A**

802.3cb will be a revision of IEEE Std 802.3-2017 which will incorporate IEEE Std 802.3bz-2016 so there is no need to include the text "(as inserted by IEEE Std 802.3bz-2016)" in the editing instruction

SuggestedRemedy

Delete the text:
"(as inserted by IEEE Std 802.3bz-2016)"

Scrub the entire document to update to make the editing instructions to refer to the new base standard.

Also delete the editor's note on line 3 pf page 31.

Also if 802.3cb is to be published after 802.3cd then the editing instructions need to take into account any changes introduced by 802.3cd. This is particularly relevant for the Clause 73 edits.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Change the draft to be an amendment to the output of the current revision project.

The Working Group Chair has indicated that this will be Amendment 1.

Remove the changes to the third paragraph of 73.6.4 and the fourth paragraph of 78.1.3.3.1 from the draft as these are no longer needed.

Cl **31B** *SC* **31B.4.3** *P* **164** *L* **7** # r02-22

RAN, ADEE — Intel Corporation

Comment Type **ER** *Comment Status* **A**

The editorial instructions refer to item labels that have been inserted by 802.3bz, but in the revision project these labels were modified.

Also applies to 31B.4.6.

SuggestedRemedy

In the editorial instruction, change "MIIca" to "MIId" and "MIIcb" to "MIIe".

Change item labels from "MIIcaa" to "MIId1" and "MIIca1" to "MIIe1" in the instruction and in the table.

Apply similar changes in 31B.4.6.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Modify the changes to 31B.4 to be appropriate to an amendment to the output of the revision project.

Cl **69B** *SC* **69B.4.3** *P* **173** *L* **3** # r02-24

RAN, ADEE — Intel Corporation

Comment Type **TR** *Comment Status* **A**

Figure 69B-5a and Figure 69B-5b don't include the "high confidence region" label (which appears in the similar existing figures).

SuggestedRemedy

Add "high confidence region" labels at the appropriate places.

Response *Response Status* **W**

ACCEPT.

Cl **128A** *SC* **128A.1** *P* **182** *L* **2** # r02-30

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

"Figure 128A-2 (one direction shown) and Equation (128A-1) depict a typical 2.5GSEI application and summarize the informative differential insertion loss budget, which is shown in Figure 128A-3"

This is inaccurate.

Figure 128A-2 depicts the the informative differential insertion loss budget at a certain frequency (Nyquist frequency is 1.5625 GHz; this is mentioned in the figure title but not in the text).

Equation 128A-1 and Figure 128A-3 are not about a loss budget, they are the informative maximum insertion loss from TP0 to TP5 for frequencies from 0.05 to 2.34375 GHz.

Similar issue with similar text in 130A.1.

SuggestedRemedy

Change the quoted text to:

"Figure 128A-2 (one direction shown) depicts the informative differential insertion loss budget at 1.5625 GHz for a typical 2.5GSEI application.
The informative maximum differential insertion loss from TP0 to TP5 is given in Equation (128A-1) and depicted in Figure 128A-3."

In 130A.1, change
"(one direction shown) and Equation (130A-1) depict a typical 5GSEI application and summarize the informative differential insertion loss budget, which is shown in Figure 130A-2."

To
"Figure 130A-2 (one direction shown) depicts informative differential insertion loss budget at 2.578125 GHz for a typical 5GSEI application.
The informative maximum differential insertion loss from TP0 to TP5 is given in Equation (130A-1) and depicted in Figure 130A-2."

Response *Response Status* **W**

ACCEPT.

Cl **128A** *SC* **128A.1** *P* **183** *L* **2** # r02-32

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

Figure 128A-3 does not show which side of the line is good, and its title is vague.

SuggestedRemedy

Add a label "meets equation constraints" above the curve.

Change the title to "Informative maximum differential insertion loss from TP0 to TP5".

Response *Response Status* **W**

ACCEPT.

Cl **129** *SC* **129.1.4** *P* **131** *L* **19** # r02-35

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

"The nominal rate of the PMA service interface is 322.27 Mtransfers/s"

This should be exactly 1/16 of the nominal rate of PMD service interface, which is stated in the next paragraph as 5.15625 Gb/s.

This yields exactly 322.265625 Mtransfers/s.

Numbers in the standard are exact; there is no reason for truncating digits.

SuggestedRemedy

Change "322.27" to "322.265625".

Response *Response Status* **W**

ACCEPT.

Cl **128A** *SC* **128A.3.1** *P* **186** *L* **5** # r02-37

RAN, ADEE Intel Corporation

Comment Type **GR** *Comment Status* **A**

Host output measurements should be performed with AC coupling to the test equipment, since the host transmitter is normally used with an AC-coupled receiver.

This is shown in the test setup diagrams (e.g. Figure 128B-1), but not mentioned here.

Also applies to drive output measurements, 128A.3.3.

SuggestedRemedy

In the paragraph starting at L39, change:

"A test system with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth is to be used for all output signal measurements"

to
"A test system as depicted in Figure 128B-1, with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth, is to be used for all output signal measurements"

Apply a similar change in 128A.3.3.

Response *Response Status* **W**

ACCEPT.

Cl **128A** *SC* **128A.3.1.3** *P* **188** *L* **3** # r02-38

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

Figure 128A-7 does not show which side of the line is good.

SuggestedRemedy

Add a label "meets equation constraints" below the curve.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Also add "limit" to the end of the title of Figure 128A-7 (and check others).

Cl **128A** *SC* **128A.3.1.7** *P* **189** *L* **10** # r02-42

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **R**

PRBS9 is not a defined test pattern for a 2.5GBASE-X PHY. Neither the PMD nor the PCS have these test pattern even as optional capabilities.

In addition, the PCS never generates or expects a run of more than 5 bits, while this pattern has multiple runs up to 9 bits long. So even loopback may be impossible, since the receiver may not be able to receive PRBS9 correctly.

Since PRBS9 is used here only for the SNDR measurement (which uses the linear-fit procedure), we can remove it if the SNDR is defined in another way, such as with a square wave pattern.

SuggestedRemedy

Change the test definition in this clause as follows:

Use the test pattern defined in Annex 48A.5 (five 1's and five 0's); maintain the reference equalizer from 93A.1.4.3, with values from Table 128A-2.

Capture a large enough number of cycles of the test pattern to enable the desired measurement accuracy, sampling 10 samples per cycle such that the samples closest to the zero-crossings are approximately 0.5 UI away from the zero-crossing. The reference equalizer is applied in the measurement. Label the samples v_1 to v_N, where N is the ten times the number of cycles.

Define V_avg as the average of the samples.
Define A as the mean of the absolute difference between each sample and V_avg (A = Sigma[abs(V_i-V_avg)]/N, i=1 to N).
Define sigma_n+ as the RMS of the difference between each positive sample and A (sigma_n+ = Sqrt(Sigma[(V_i-A)^2]*2/N), for all i where V_i>0).
Define sigma_n- as the RMS of the difference between each negative sample and -A (sigma_n- = Sqrt(Sigma[(V_i+A)^2]*2/N), for all i where V_i<0).

Define SNDR as 10*log10(A^2/((sigma_n+)^2 + (sigma_n-)^2), with the reference equalizer setting that yields the highest value for that ratio.

Response *Response Status* **W**

REJECT.

While it is true that the 8B/10B code is restricted to a run length of 5 bits, the sutibility of a test pattern should be based on its low frequency content and not its run length.

It has not been demonstrated that the suggested remedy provides an adequate measure of distortion and noise.

In addition this comment is out of scope because it does not relate to changes made between D3.1 and D3.2 or an unsatisfied negative comment.

Cl **128A** *SC* **128A.3.2.2** *P* **190** *L* **33** # r02-43

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

"The data pattern used for the receiver interference tolerance test shall be PRBS7"

PRBS7 is not a valid pattern for a 2.5GBASE-KX PHY, and there is no error counting capability defined for this pattern (it is actually not use by any clause in 802.3). Even if the test is performed with loopback, the receiver or its transmitter may be unable to handle this pattern correctly.

Receiver tolerance should be done with a test pattern representing real traffic; for example Clause 128 specifies using the test pattern defined in 48A.4 (proposed to be changed to 48A.5 in comment r02-10).

Also applies to the drive interference tolerance test in 128A.3.4.2 and to the host and drive jitter tolerance tests in 128A.3.2.3 and 128A.3.4.3.

SuggestedRemedy

Change "PRBS7" to "the test pattern defined in 48A.5", here and in 128A.3.2.3, 128A.3.4.2, and 128A.3.4.3.

Update the PICS accordingly.

Response *Response Status* **W**

ACCEPT.

Cl **128A** *SC* **128A.3.1.4** *P* **188** *L* **28** # r02-45

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

The transmitter output waveform specification uses the procedure in 92.8.3.5.1. But that procedure uses a PRBS9 test pattern which is not a valid pattern for a 2.5GBASE-KX PHY.

This test may not be possible to conduct with some compliant transmitters. Also, since an 8B/10B transmitter does not generate all possible combinations of ISI cursors (for example, it can't generate long unbalanced sequences or long runs), this kind of analysis is not meaningful. Specifically the steady-state voltage from this analysis cannot appear with valid data (unlike in BASE-R PHYs).

Clause 128 has different measurement methods. They should be followed here, and extended if necessary. The limit values for these specifications may be different due to the measurement point.

The drive output characteristics in 128A.3.3.1 have the same issue.

These specifications are also referenced in the receiver interference tolerance tests and their associated tables, so those should be changed too.

SuggestedRemedy

For the host output:

Delete 128A.3.1.4 entirely. (possibly add instead specifications similar to those of 128.7.1.4 (Output amplitude) and 128.7.1.7 (Transition time), but these can be referenced directly).

In Table 128A-1:
- Delete the "Output waveform" row.

- Add a row for Peak-to-peak differential output voltage (min) with value 580 mV and (max) with value 1200 mV, measured per 128.7.1.4. (The min value accounts for the expected attenuation of a 10-UI-period square wave launched at 800 mV, with the maximum IL).

- Add a row for Maximum transition time (20%-80%) with value 460 ps, measured per 128.7.1.7. (The value matches the pulse-peak-to-steady-state ratio: 60%*UI/0.42).

Update and reorder 128A.3.4.2 (drive input receiver interference tolerance) so that in step c) the amplitude is adjusted to meet the PTP output voltage in Table 128A-8, and in step d) the ISI channel is adjusted to meet the transition time in Table 128A-8. Update table 128A-8 accordingly, replacing the first two rows with the min PtP output voltage and max transition time of the host.
Apply the same changes in 128A.3.4.3 (drive input receiver jitter tolerance) replacing Table 128A-8 with Table 128A-9.

For the drive output:

Delete 128A.3.3.1, 128A.3.3.2 and 128A.3.3.3.

In Table 128A-6:
- Delete the "Output waveform" row.
- Add a row for Peak-to-peak differential output voltage (min) with value 800 mV, and (max) with value 1200 mV, measured per 128.7.1.4. (The expected attenuation of a 10-UI-period square wave at the drive output is negligible).

- Add a row for Maximum transition time (20%-80%) with value 229 ps, measured per 128.7.1.7. (The value matches the pulse-peak-to-steady-state ratio: 60%*UI/0.84).

Update and reorder 128A.3.2.2 (host input receiver tolerance) so that in step c) the amplitude is adjusted to meet the PTP output voltage in Table 128A-3, and in step d) the ISI channel is adjusted to meet the transition time in Table 128A-3. Update table 128A-3 accordingly, replacing the first two rows with the min PtP output voltage and max transition time of the drive.
Apply the same changes in 128A.3.2.3 (host input receiver jitter tolerance) replacing Table 128A-3 with Table 128A-4.

Update the PICS accordingly.

Response *Response Status* **W**

ACCEPT.

Cl **130A** *SC* **130A.3.1** *P* **216** *L* **5** # r02-53

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

Host output measurements should be performed with AC coupling to the test equipment, since the host transmitter is normally used with an AC-coupled receiver.

This is shown in the PMD test setup diagrams (e.g. Figure 128B-1), but not mentioned here.

Also applies to Drive output measurements, 130A.5.

SuggestedRemedy

In the paragraph starting at L40, change:

"A test system with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth is to be used for all output signal measurements"

to
"A test system as depicted in Figure 128B-1, with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth, is to be used for all output signal measurements".

Apply a similar change in 130A.5.

Response *Response Status* **W**

ACCEPT.

Cl **130A** *SC* **130A.3.1** *P* **216** *L* **29** # r02-62

RAN, ADEE
Intel Corporation

Comment Type **TR** *Comment Status* **A**

In Table 130A-1, Pre-cursor equalization ratio is specified as 0.65 +/- 0.65 which means 0 to 1.3. From the definition of Rpre in 130.7.1.10, this means that v2 (the voltage 1 UI before a transition) can be from 0 to 1.3 times higher than the steady-state voltage.

This wide range does not make sense; it is effectively saying "anything goes".

Note that At the PMD's transmitter, the pre-cursor ratio should be 1.2 to 1.3 (Table 130-4) due to pre-emphasis. But ISI created by the channel will reduce this ratio at TP4H-D. A value of 1 is ideal; any deviation from 1 is the ISI left to the receiver. Simple receivers will not be able to deal with a large precursor, so the precursor has to be controlled.

The pre-cursor ratio as defined in 130.7.1.10 is difficult to measure after the host channel, since the value v2 will not be on a "flat" voltage as in Figure 130-7.

Instead, the linear fit procedure specified in 130A.3.3.1 (defined in 92.8.3.5.1) can also be used to limit the pre-cursor ISI; this procedure yields c(-1) which is effectively the normalized precursor value - exactly what we want to control.

A recommended range for c(-1) is between -0.05 to +0.05. This corresponds to Rpre values from 1.11 to 0.9 respectively, which would leave precursor noise up to 10% of the main pulse (for receivers which do not handle precursor at all, this will create vertical eye closure of ~10%).

This may also apply to 130A.5 which measures the drive output; at that test point, the c(-1) should still be negative since it is in short distance from the PMD's transmitter, which is pre-emphasized (originally with Rpre=1.25, correponding to c(-1)=-0.125).

SuggestedRemedy

Create new subclause 130A.3.3.3 titled "Pre-cursor coefficient" with the text:

The Pre-cursor coefficient, c(-1), is determined according to 130A.3.3.1.

In Table 130A-1, replace "Pre-cursor equalization ratio" with "Pre-cursor coefficient", referenced to 130A.3.3.3, with value +/- 0.05.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Apply suggested remedy with the exception that '… value +/- 0.05.' is replaced by '… value +/- 0.1.'.