Achieving closure on TDECQ/SRS

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Background

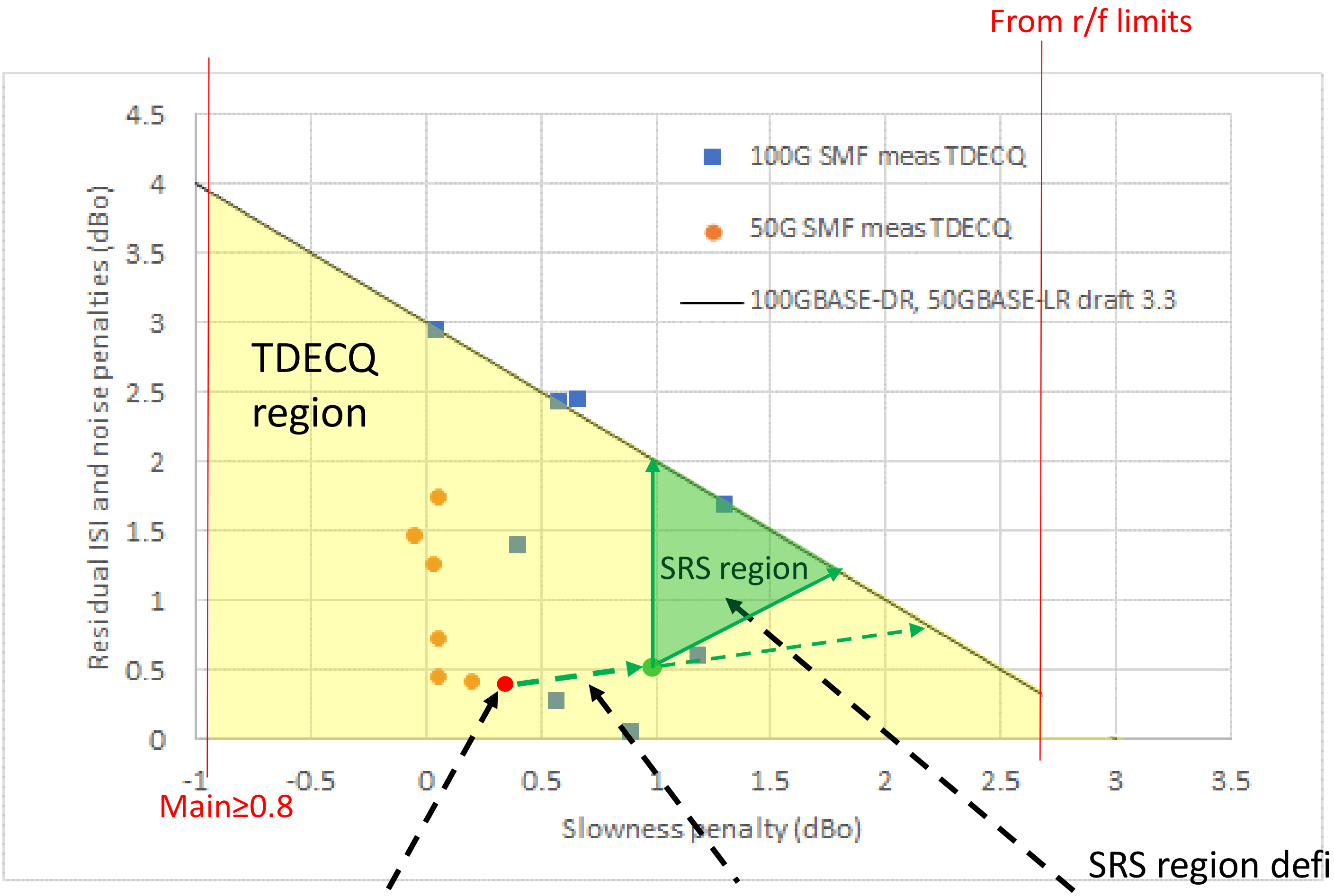
Several discussions have been taking place about TDECQ method and limit, which drive SECQ limits for SRS implementation.

In this presentation we summarize most of these into two main topics which are linked together, together with our proposal to resolve:

1. Align the Receiver SRS testing criteria to match the range of allowable Transmitters defined by TDECQ
   - Opportunity to remove the SECQ constraint due to Low-pass filter.

2. TDECQ region (aka transmitter map) optimization.

1. Align Receiver SRS criteria with Transmitter TDECQ criteria



SRS criteria covers a subset of range allowable transmitter.

SRS region defined by the SECQ constraint criteria that requires half the stress be due to filtering.

Propose to remove SECQ constraint to match the range of Transmitter TDECQ.

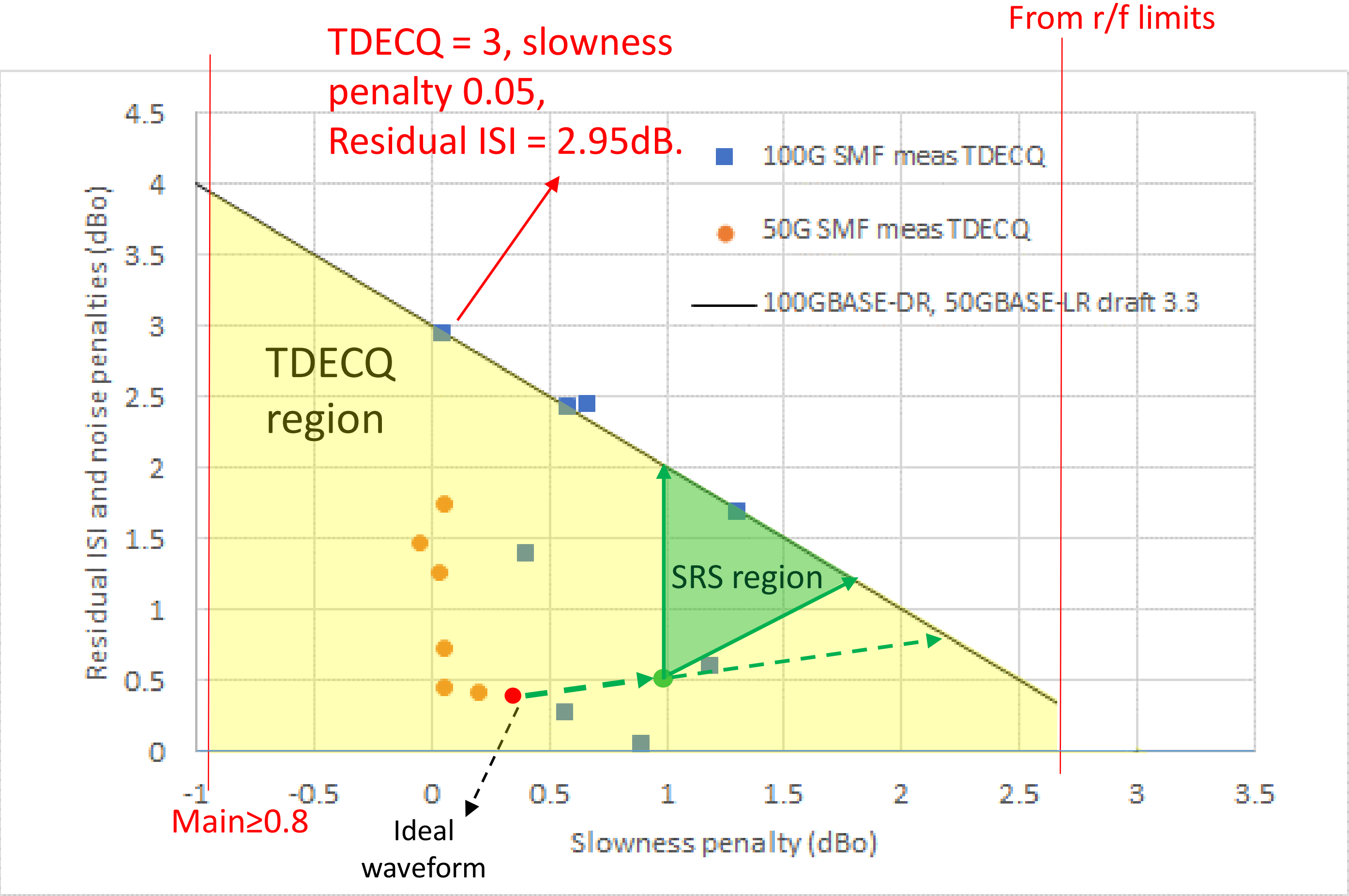
SECQ Criteria

1 Start from "Ideal Waveform"

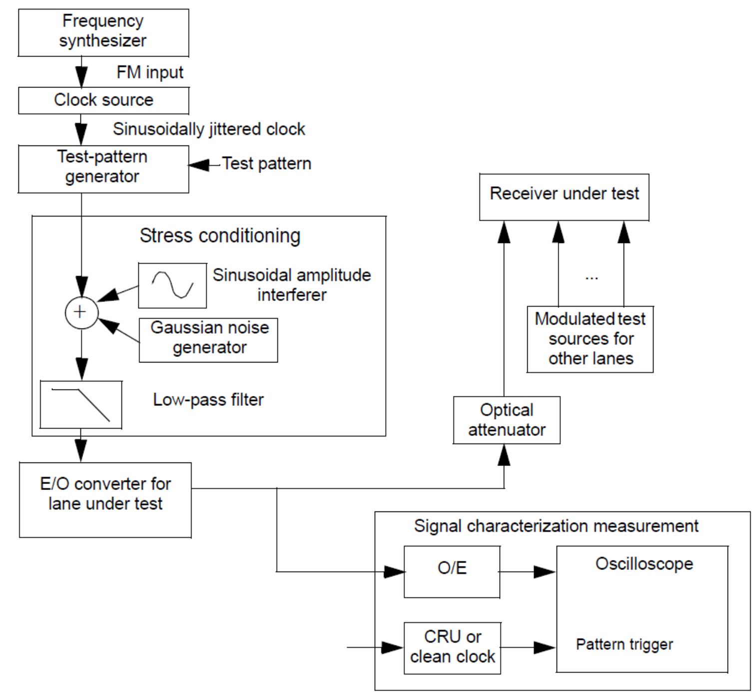
2 Add at least 50% SECQ penalty due to filtering

3 SRS region defined by additional penalties adding SJ than noise and/or ISI up to SECQ limit

1. Opportunity to remove the SECQ constraint due to Low-pass filter.



50/100G Transmitter map versus current tap constraint and SRS.



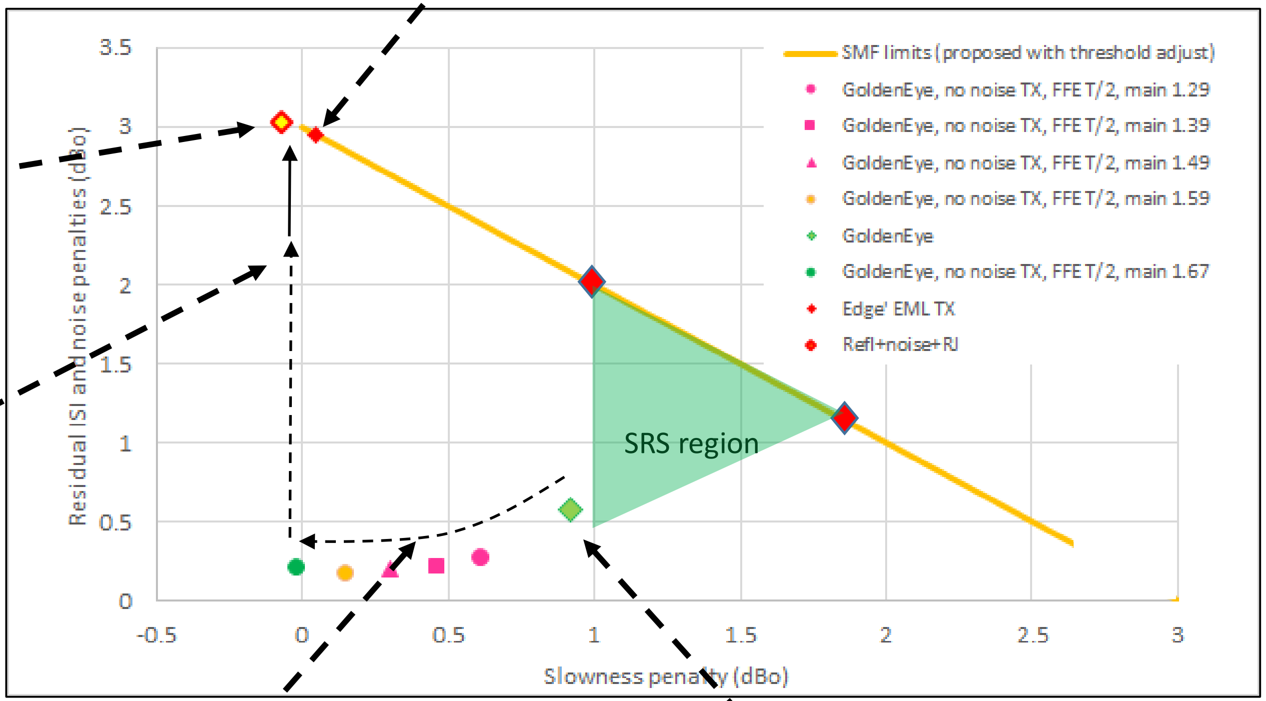
*From **121.8.9.1** 'The low-pass filter is used to create ISI. The combination of the low-pass filter and the E/O converter should have a frequency response that results in at least half of the dB value of the stressed eye closure (SECQ) specified in Table…'.*

- Most of the 50G and 100G SMF transmitters are outside the SRS (Green) calibration region.
  - *(Note: example about 50GBASE-LR and 100GBASE-DR that currently share same TDECQ/SECQ limits).*
- There's a risk to not screen receivers against transmitter limits, which would contain some heavy distorted (but allowable) cases.

Evaluation Approach

Experimental
100G PAM4 EML

4 Added RJ (990fs) and noise (90uW, ≈1% signal strength) -> TDECQ = 2.95dB



Start from shared GoldenEye waveform.

Apply distortions to emulate shared experimental EML TDECQ data

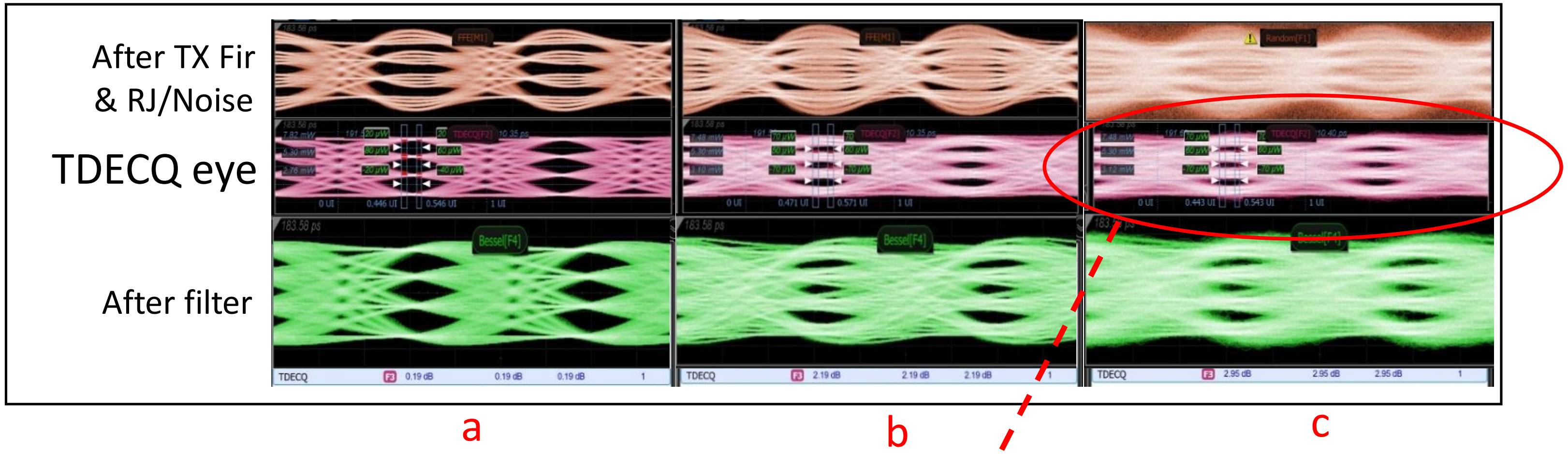
3 To emulate noise from residual distortion, a reflection was added at 6UI -> TDECQ = 2.3dB

2 Apply 5T/2 TX FIR using Keysight FlexDCA sim tool. TDECQ improvement achieved with eye pre-distortion (pre-emphasis)

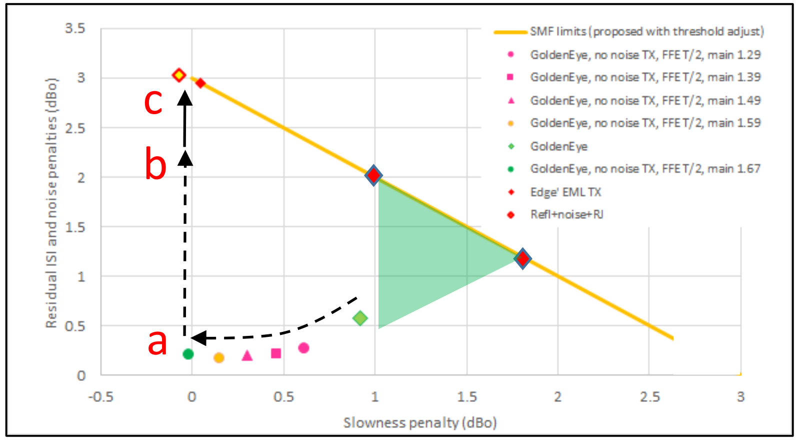
1 Start from “GoldenEye” from [mazzini_062018_3cd_adhoc]

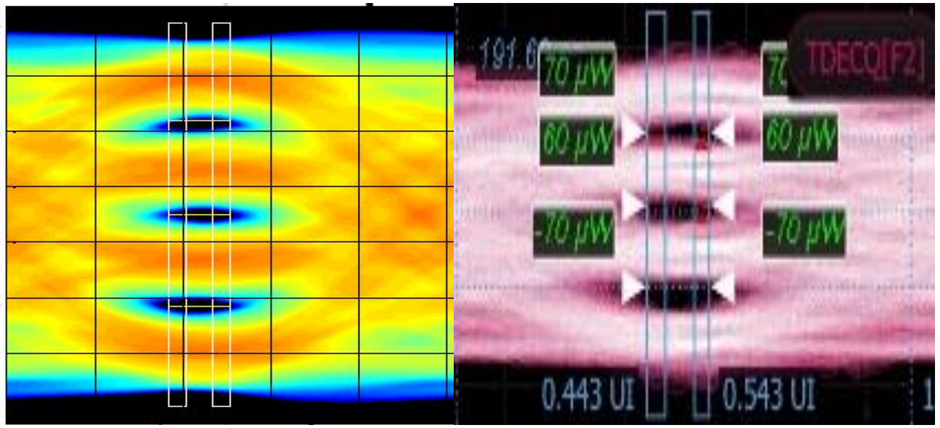
Used PRBS13Q for faster processing

1. Opportunity to remove the SECQ constraint due to Low-pass filter.



	GoldenEye	Reflection	Noise
TDECQ (dBo)	1.37	2.19	2.95
Slowness penalty (dBo)	0.92	-0.11	-0.07
Residual ISI, noise penalties (dBo)	0.58	2.3	3.02





Similar eye as the one simulated into
dawe_061318_3cd_adhoc-v2

Will current SRS test ensure Rx can accept this allowable signal?

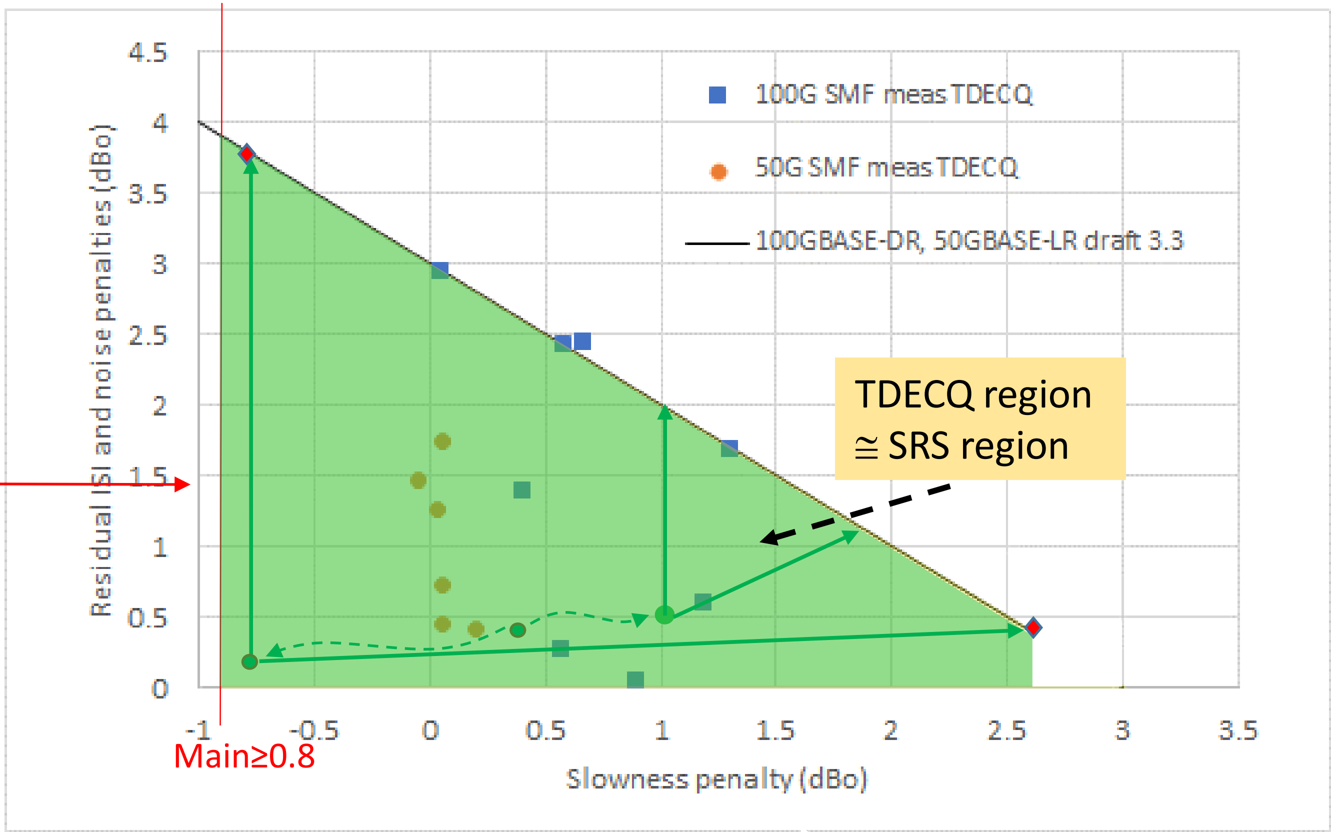
This case is potentially worse (in terms of noise floor and RX noise margins) with respect the limits we can reach with the current SRS tester definition (chang_3cd_01_1117 – showed greater error floor sensitivity to noise than ISI).

Note: we are not protected against this eye by RINxOMA specs itself (SRS should eventually emulate).

1. Proposal: Align Receiver SRS criteria with Transmitter TDECQ criteria

Where RINxOMA start to limit this region?

Do we accept any kind of (residual) distortion that pass TDECQ?



To ensure that implemented solution won't have interoperability issues, SRS (SECQ) calibration region should be allowed to at least overlap with TDECQ transmitter map.

To extend the SRS (SECQ) region:

- remove the constraint on SECQ due to Low-pass filter,
- allow emphasis to the SRS tester
- allow freedom to any combination of Sinusoidal Interference and Gaussian noise to build-up the stressor up to SECQ limits.

Note: Top-left corner is hard to implement into SRS too. Next slides show proposal to limit Transmitter specs in this region

2. TDECQ region (aka transmitter map) optimization

TDECQmax

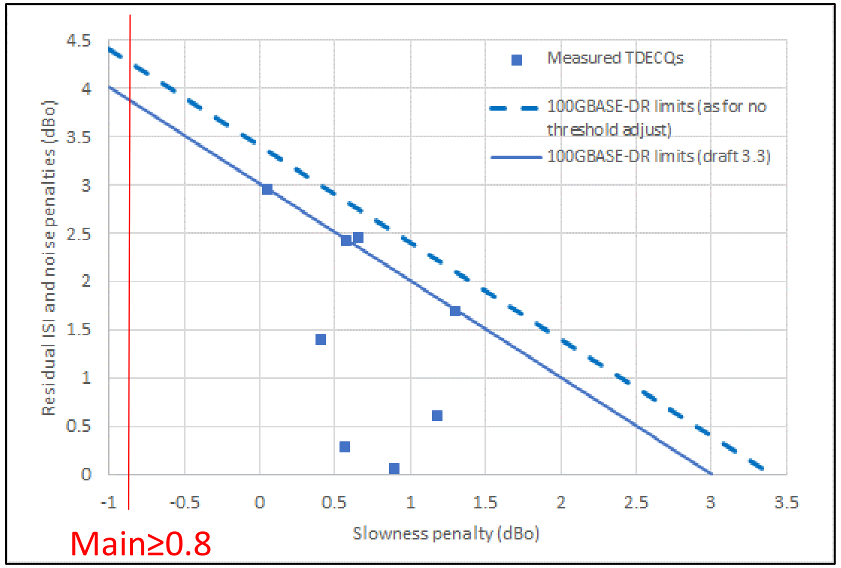
- D3.3 lowered TDECQmax by 0.4dB for all optical PMDs.
- Experimental evidence suggested that there was margin supporting this for MMF PMDs.
- Recent SMF experimental data (especially for 100GBASE-DR) suggests reversion to D3.2 values would be beneficial.

Constraining TDECQmax in upper left region

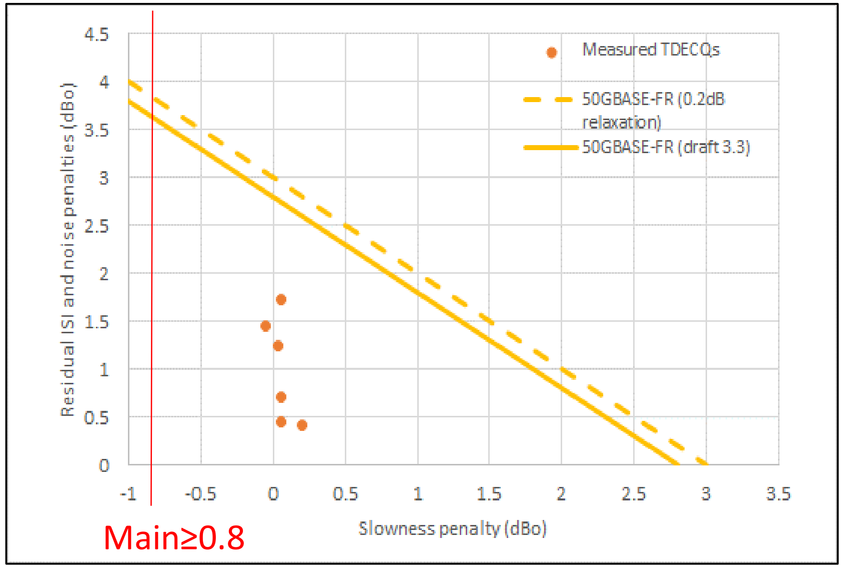
- Proposed to limit allowable Transmitters away from this region.
- Not expected to impact population yields of known devices/designs.
- Simplifies receiver design complexity and equalization power.

2. $TDECQ_{max}$ relaxation.

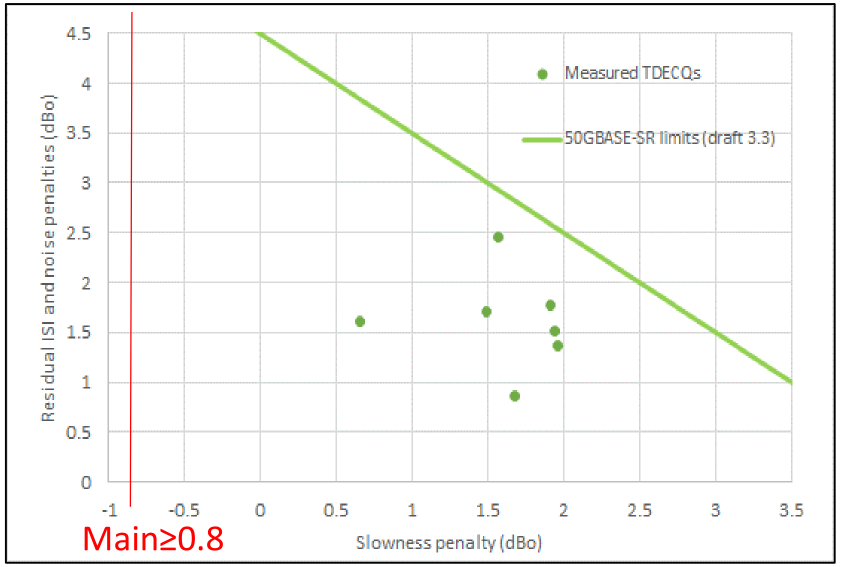
Measured TDECQs versus 802.3cd PMD types (includes EML, DML and SiPhotonics transmitters).



100GBASE-DR



50GBASE-FR and 50GBASE-LR (with 50GBASE-FR limit)



50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4

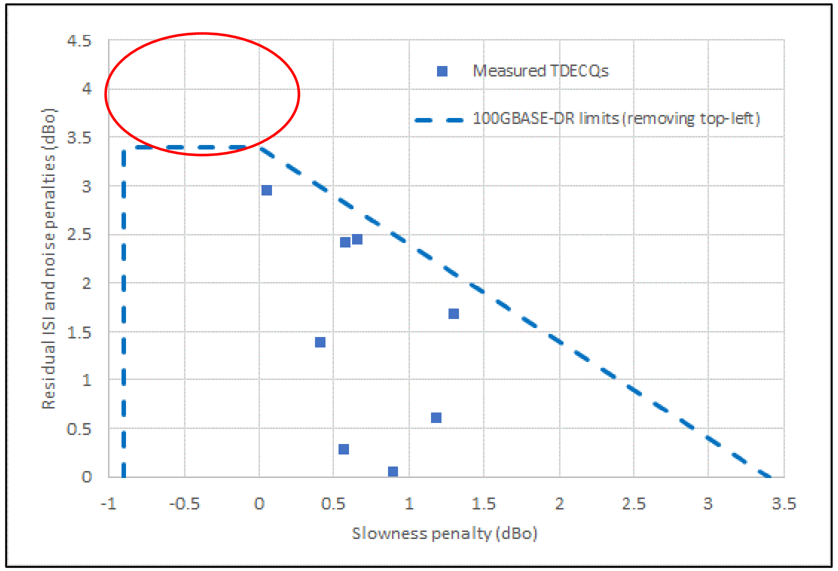
- Consider measured TDECQs as representative of current technologies
  - Draft 3.3 limits (represented by solid lines) seem tight especially for 100GBASE-DR.
- Proposals to relax $TDECQ_{max}$ for SMF PMDs.
  - 0.4dB relaxation with respect Draft 3.3 for 10GBASE-DR, 0.2dB relaxation with respect Draft 3.3 for 50GBASE-FR/LR.

2. Constraining $TDECQ_{max}$ in upper left region

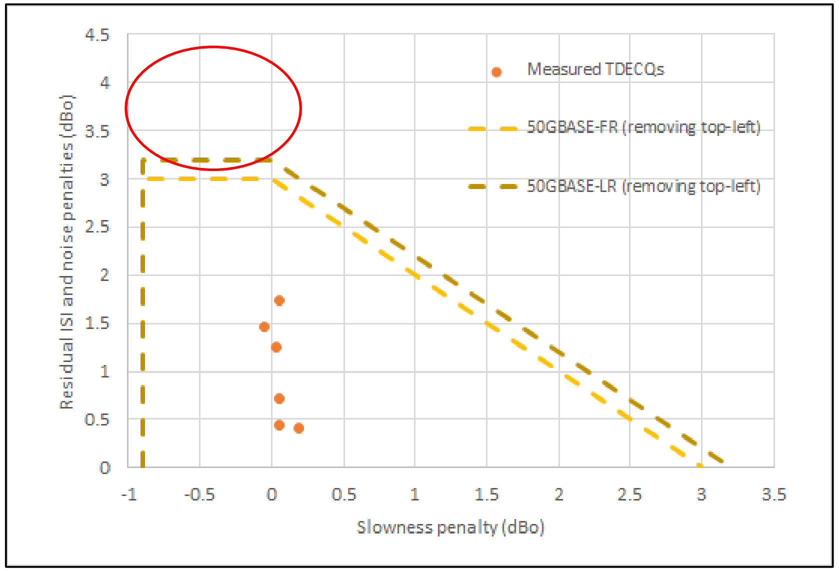
Propose to bound the top-left region by adding a limit equivalent to TDECQ -10*log10(Ceq)

- Aligned with the proposed $TDECQ_{max}$ increase in previous slide

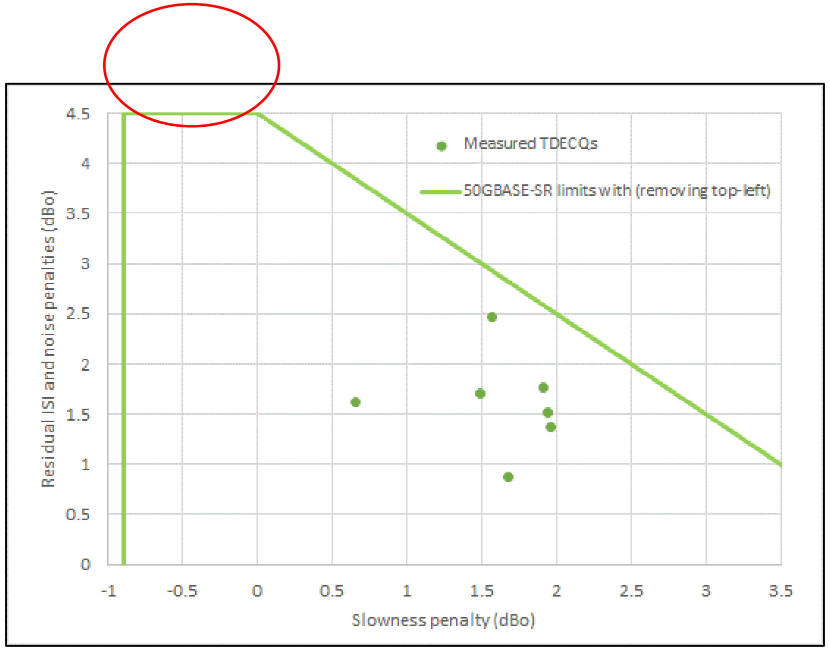
Negligible impact to Tx yield



100GBASE-DR: limit to 3.4dB



50GBASE-FR: limit to 3dB
50GBASE-LR: limit to 3.2dB



50GBASE-SR, 100GBASE-SR2
and 200GBASE-SR4: limit to 4.5dB

Why add this constraint?

- Very difficult region to verify SRS compliance
- Adds additional equalizer power and design complexity to receiver
- Real transmitters not expected to be realizable in this region

Summary

Two proposals to address TDECQ and SRS improvements to P802.3cd draft

1. Align Receiver SRS criteria with Transmitter TDECQ criteria.
   - To ensure SRS testing alignment, remove the ‘half SECQ’ constraint from filter during calibration.
   - The SRS tester should include emphasis capability.

2. TDECQ region (aka transmitter map) optimization.
   - Relax $TDECQ_{max}$ specs by 0.4dBo for 100GBASE-DR, 0.2dBo for 50GBASE-FR/LR.
   - Add a limit equivalent to TDECQ -10*log10(Ceq) minor or equal to TDECQ (max)

     This can be done with just two footnotes into tables 138–8, 139-6 and 140-6.

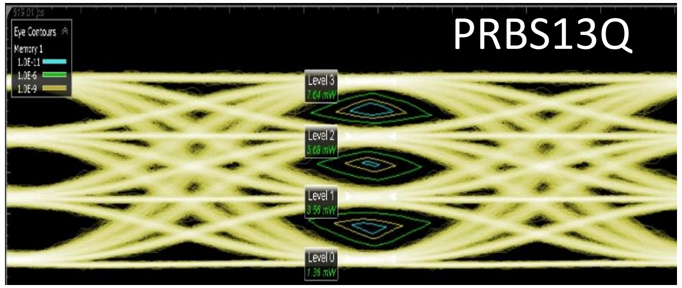
     a) TDECQ - 10Log10(Ceq) has to be ≤ TDECQ (max).
     b) Ceq is defined into 121–9. Is a coefficient which accounts for the reference equalizer noise enhancement.

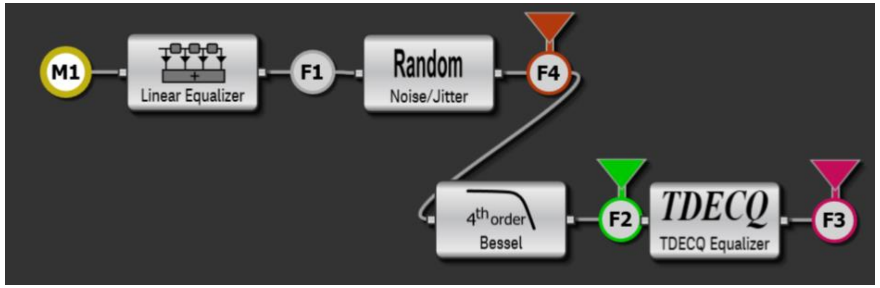
THANK YOU

BACK-UP

mazzini_062018_3cd_adhoc

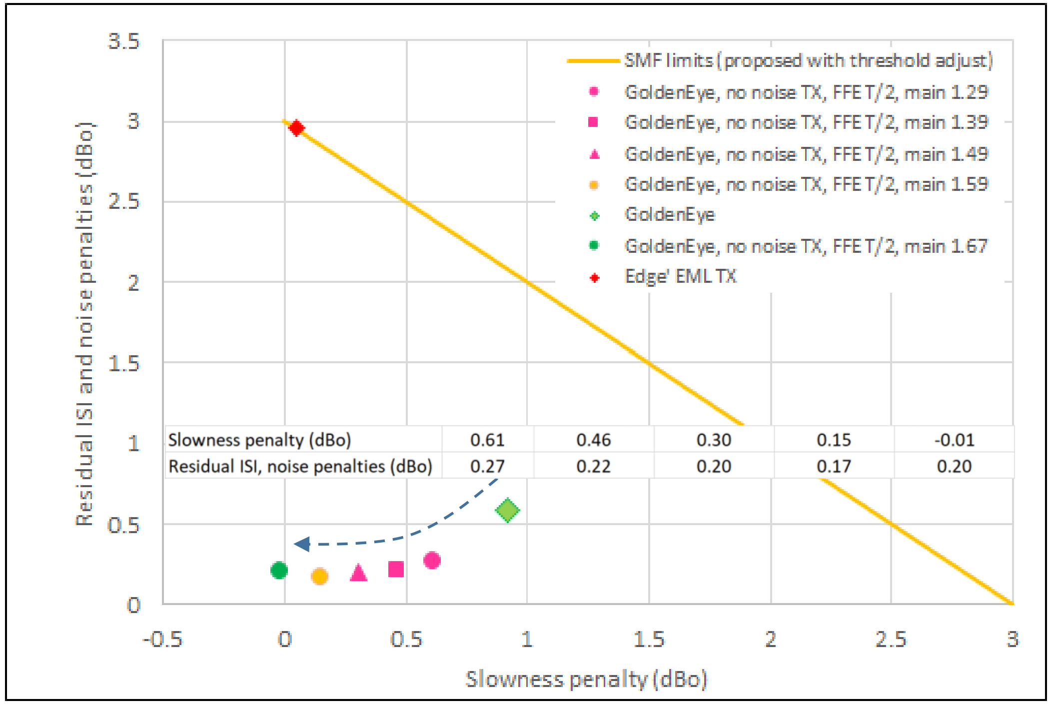
Simulation environment, conditions and results (1).





Using Keysight FlexDCA sim tool.
Added 5T/2 TX Fir over GoldenEye shared waveform (kept PRBS13Q for faster processing), random Noise/Jitter block and 4th order BT filter.

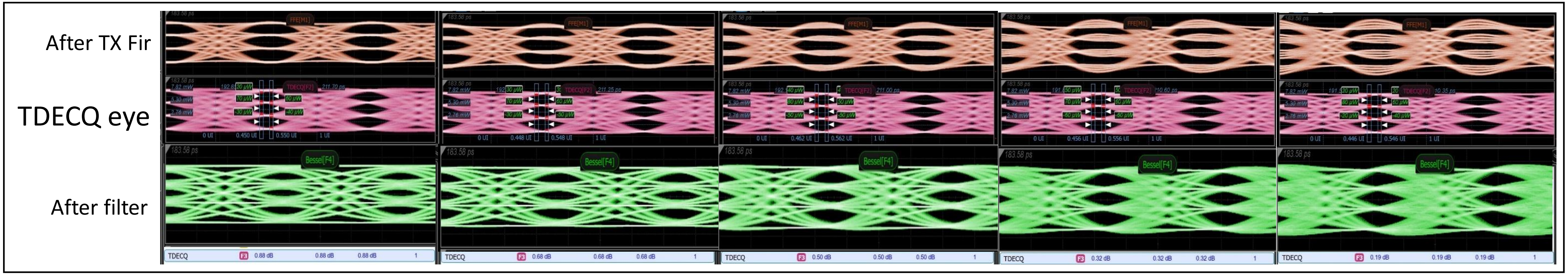
Slowness penalty (dBo)	0.92
Residual ISI, noise penalties (dBo)	0.58



Note the above is not a truly implementation, just a way to show that with proper emphasis it is possible to 'walk' the transmitter over the map.

Next slide showing F4 (TX Fir), F2 (filtered w/Nyquist) and F3 (TDECQ with reference equalizer) eye diagrams evolution for left cases from M1, for different TX Fir.

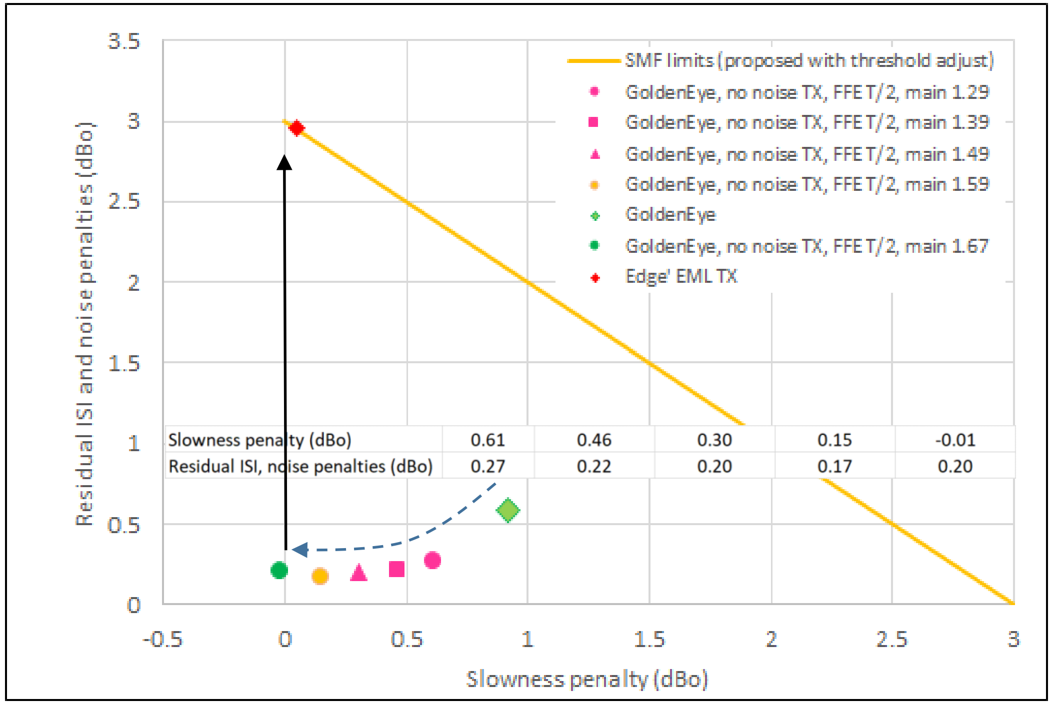
Opportunity to remove the SECQ constraint due to Low-pass filter.



TDECQ	0.88	0.68	0.5	0.32	0.19
Slowness penalty (dBo)	0.61	0.46	0.30	0.15	-0.01
Residual ISI, noise penalties (dBo)	0.27	0.22	0.20	0.17	0.20

Using Keysight FlexDCA sim tool, where 5T/2 TX Fir was applied over GoldenEye shared waveform (kept PRBS13Q for faster processing), together random Noise/Jitter block and 4th order BT filter (see mazzini_062018_3cd_adhoc).

TDECQ improvement achieved with eye pre-distortion.

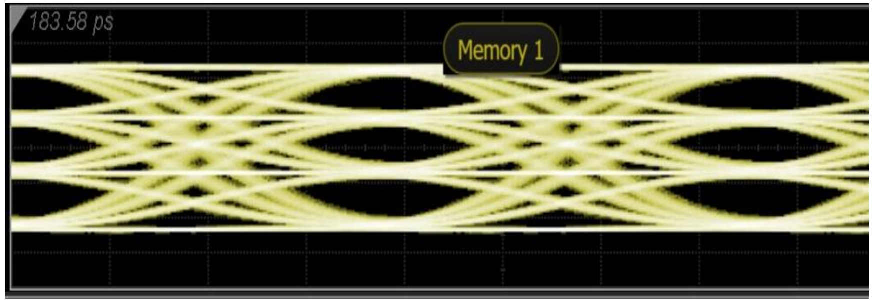


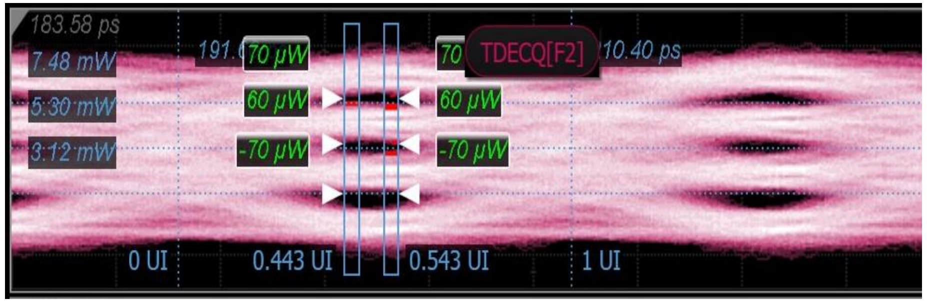
Next slide showing a posible way to get close to the 'red diamond' point at the top-left of the transmitter map (just one of the possible path).

Is the transmitter naturally bounded against distortion?

802.3cd June 2018

RINxOMA and SNDR (see 120D.3.1.6) are two parameters that can give and idea of the degradation occurring for the right case in terms of noise and distortion (Left: not equalized GoldenEye, right: distorted and noisy TDECQ = 2.95dB).





$$RIN_xOMA = -20 \times \log_{10}(Q_{sq}) - 10 \times \log_{10}(BW) \qquad \text{dB/Hz}$$

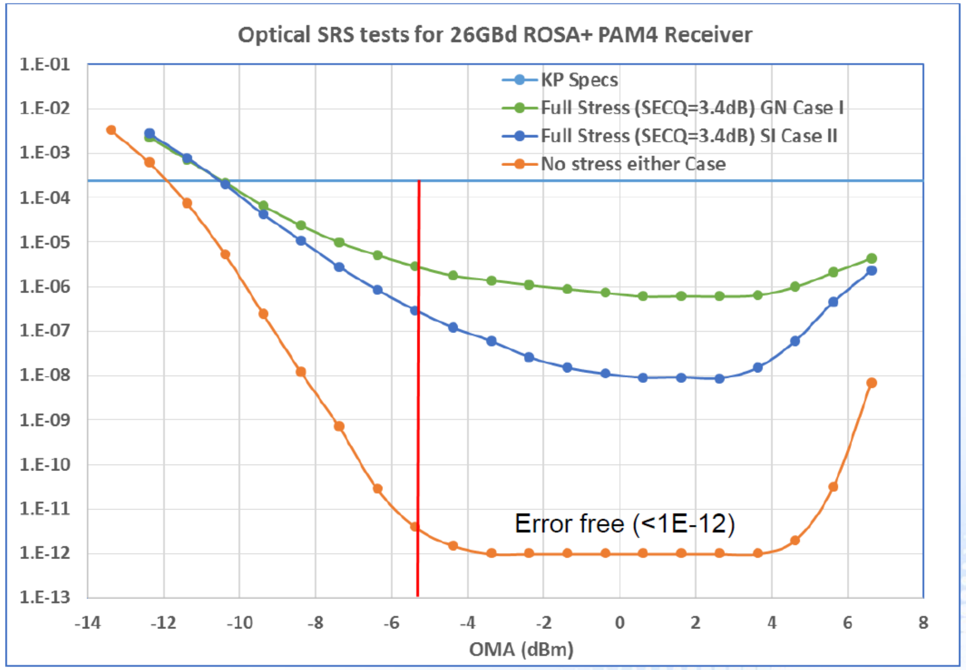
$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)$$

(SNDR 'transmit equalizer' should be set equivalent to TDECQ receiver reference equalizer).

Are these two parameters contained into the single definition of TDECQ -10*log10(Ceq) < xx dB ?

GN impact measurements – (chang_3cd_01_1117)

- Same SECQ=3.4dB but with different BER behavior



As per schube_011718_3cd_adhoc, and according to chang_3cd_01_1117, the top-left transmitter should represent a case in which we are '***Overstressing** the receiver (e.g. if more Gaussian noise is used than the worst-case allowable transmitter) and causing unnecessary yield hit*'.

A barely compliant receiver to 'full stress Case II' can get into troubles when interoperate with a transmitter closer to 'full stress Case I'. Should the (simulated) distortion be well emulated by SI in the SRS tester? (blue curve).

mazzini_01_082415_elect.pdf, slide 18

- Another item to be discussed –
Vertical eye closure (VEC) at TP1a.

Table 16-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Eye Width at 10^{-6} probability (EW6)[3]	0.25	-	UI	See Section 16.3.10
Eye Height at 10^{-6} probability (EH6)[3]	50	-	mV	See Section 16.3.10
Eye linearity[4]	-	1.5	-	

3. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE) applicable to all three PAM4 eyes
4. Eye linearity = (max(AVupp, AVmid, AVlow) / min(AVupp, AVmid, AVlow))

Table 16-2. Host-to-Module Electrical Specifications (module input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP1a	900	-	mV	See Section 16.3.11

-For TP1a compliance test, at least one of the nine CTLE settings that meets both the EH6 and EW6 settings defined for TP1a in Table 16-1 indicates a pass. As for the TP4 compliance test, at least one of the two CTLE settings that meets both the EH6 and EW6 settings defined for TP4 in Table 16-4 indicates a pass.

At TP1a, passing is defined as a single equalizer setting that meets the EH6 and EW6 specifications defined in Table 16-1 for the lower, upper and middle eyes. At TP4, passing is defined as a single equalizer setting that meets the EH6, EW6 and VEC specifications given in Table 16-4.

$$\mathrm{VEC} = 20 \cdot \mathrm{LOG}\left(\mathrm{Min}\left(\left(\frac{\mathrm{AVupp}}{\mathrm{Vupp}}\right), \left(\frac{\mathrm{AVmid}}{\mathrm{Vmid}}\right), \left(\frac{\mathrm{AVlow}}{\mathrm{Vlow}}\right)\right)\right)$$

Same EW, EH can be achieved with different VEC at TP1a.
Define a maximum VEC at TP1a too would help to constrain host output and calibrate the TP1 input stressor to the CDAUI-8 module.