Some 50 Gb/s PAM4 VCSEL results

IEEE P802.3cd ad hoc

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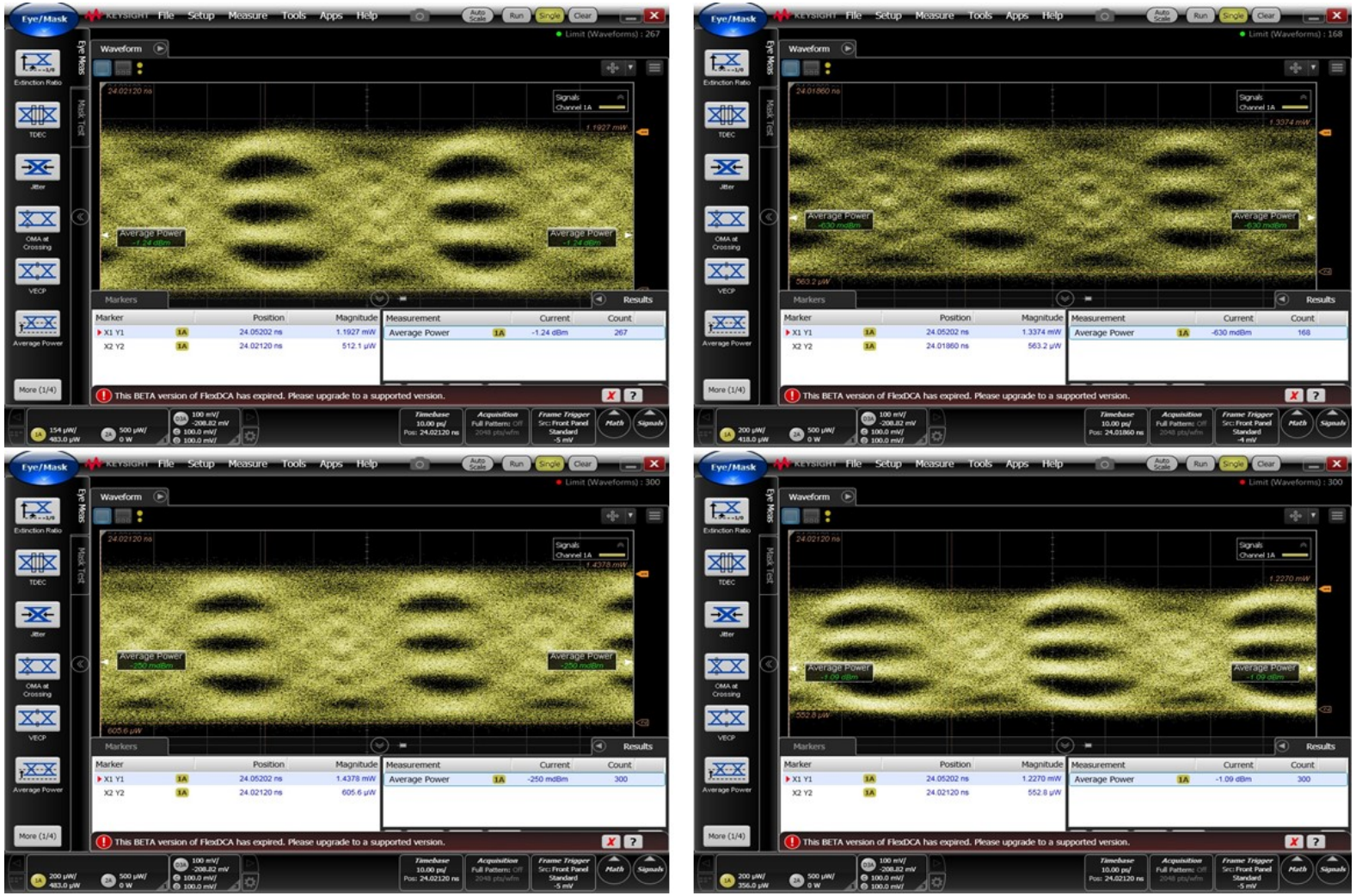
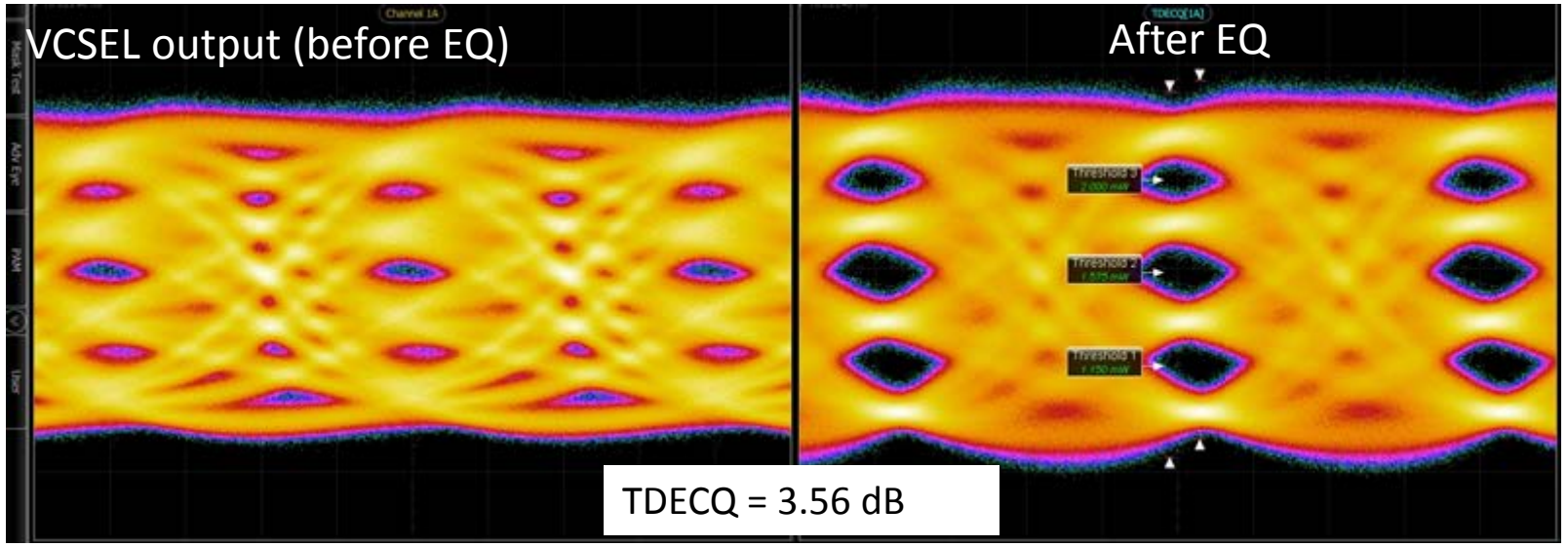
PAM4 VCSEL samples: eyes at 53.1 Gb/s -1

- Evaluation board mounted commercial drivers and test-board mounted 50Gb/s PAM4 VCSELs
  - PRBS15
- Open eyes, with reasonable timing window

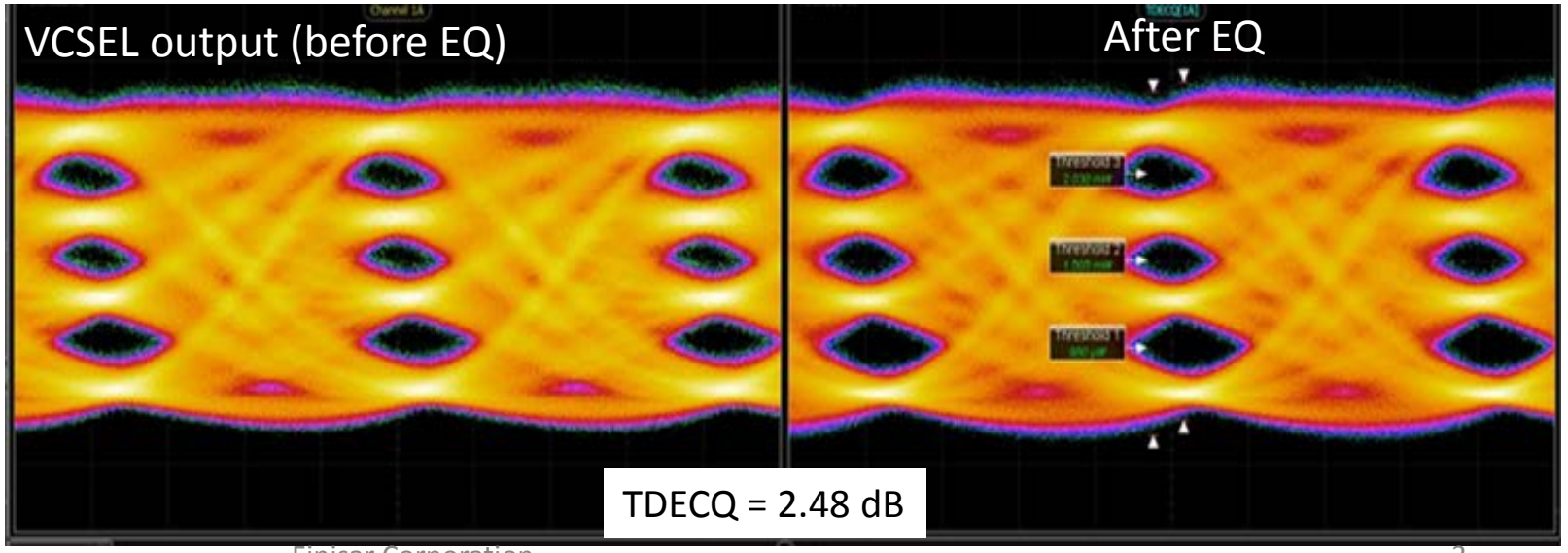


PAM4 VCSEL samples eyes and TDECQ at 53.1 Gb/s -2

- VCSEL driver without pre-emphasis
  - Unequal eye heights
- **TDECQ = 3.6 dB**
  - PRBS15
  - ER_{outer} = 5.0 dB



- VCSEL driver with pre-emphasis representative of 'real' driver
- **TDECQ = 2.5 dB**
  - PRBS15
  - ER_{outer} = 3.8 dB

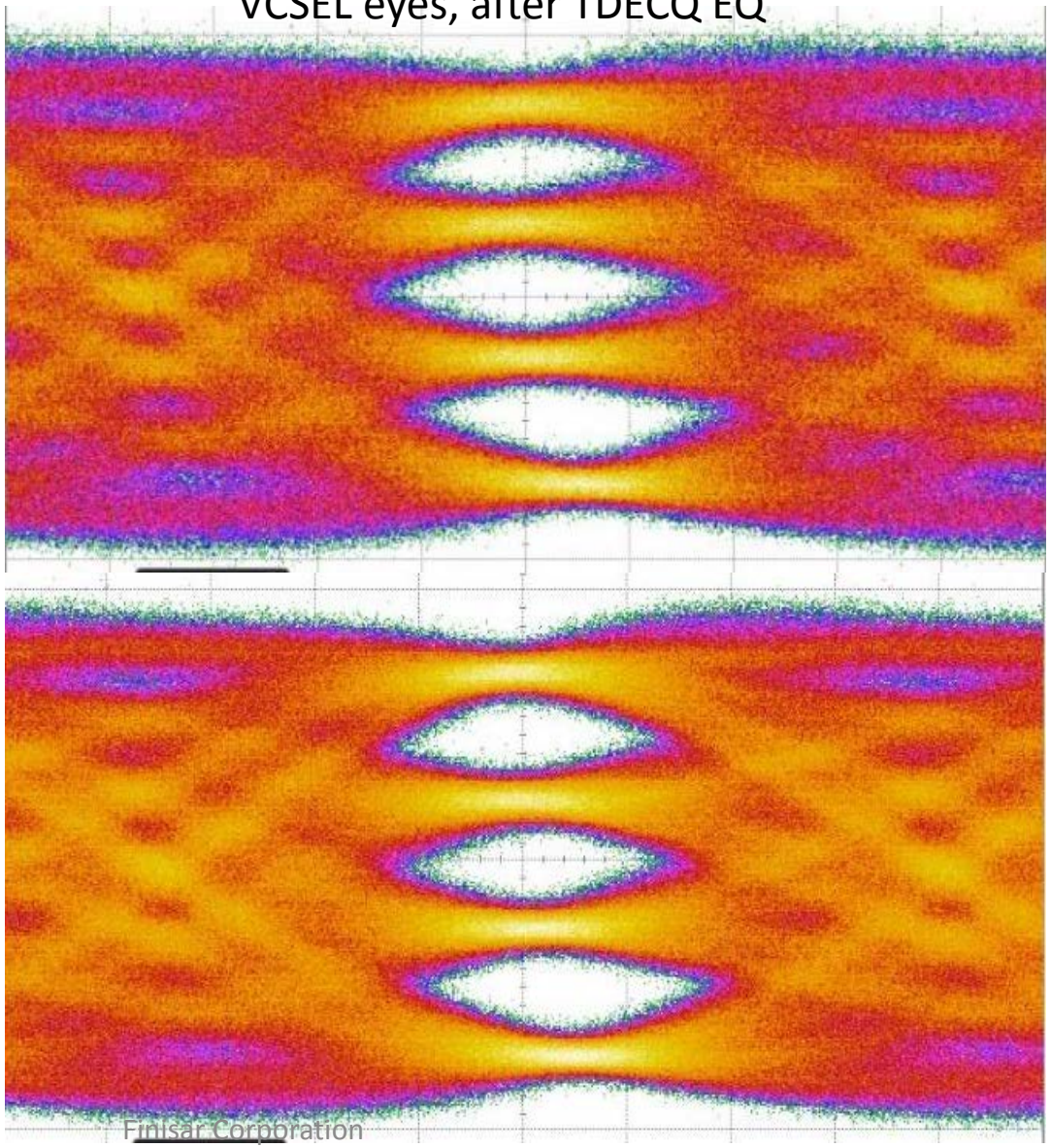


PAM4 VCSEL samples: eyes at 53.1 Gb/s and TDECQ - 2

- VCSEL driven without pre-emphasis
  - Unequal eye heights
- **TDECQ = 3.6 dB**
  - PRBS15
  - ER_{outer} = 3.5 dB

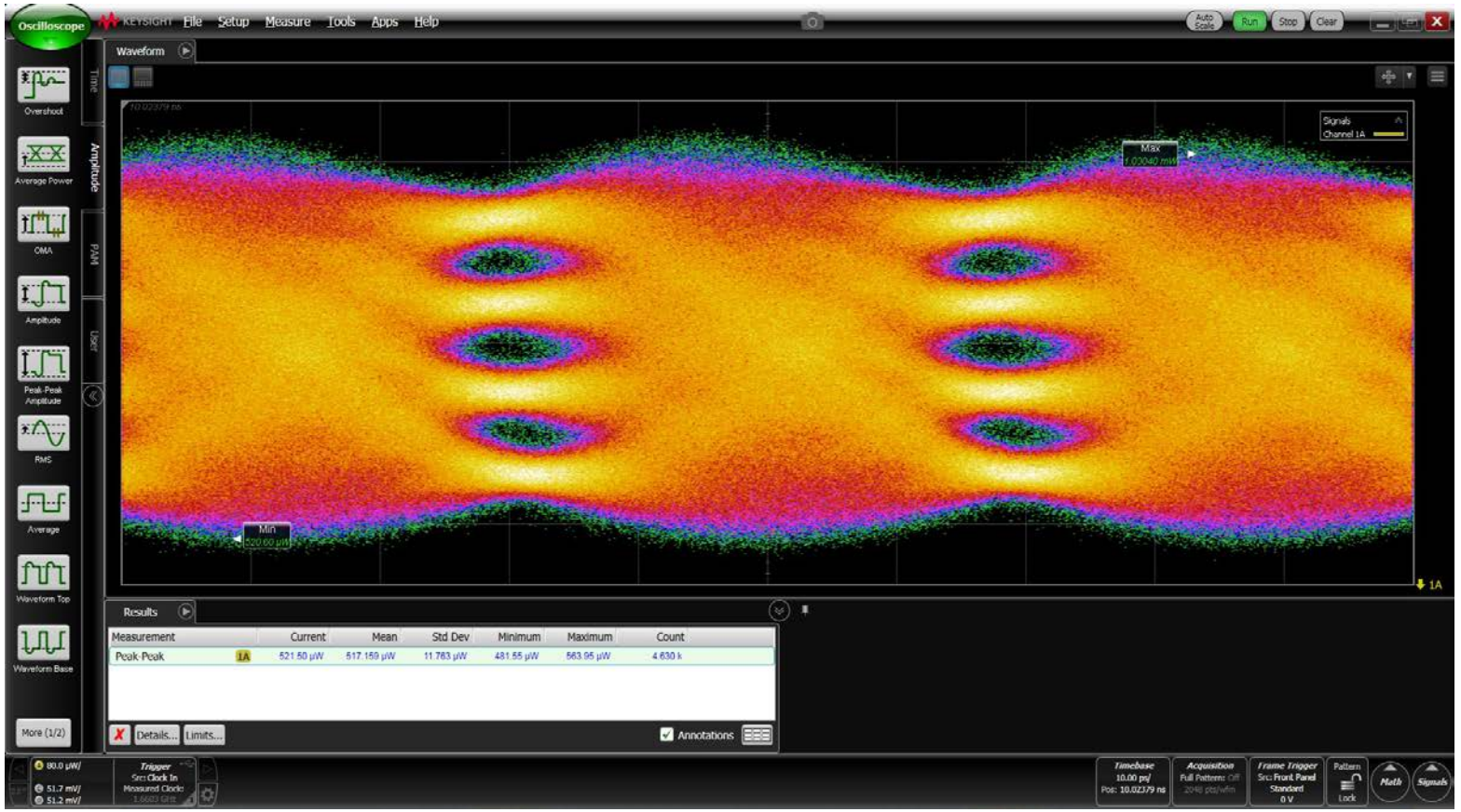
- VCSEL driven with pre-emphasis
  - Equal eye heights
- **TDECQ = 2.0 dB**
  - PRBS15
  - ER_{outer} = 3.4 dB

VCSEL eyes, after TDECQ EQ



PAM4 VCSEL samples: eyes at 53.1 Gb/s and TDECQ - 3

- VCSEL driven with pre-emphasis
  - Open eyes, reasonable timing window



Summary

- 50 Gb/s PAM4 VCSELs samples
- 3 commercial driver chips on evaluation board assemblies
  - Each has ability to shape the VCSEL driver waveform to give substantially equal height sub-eyes
- Encouraging results - open eyes, and a couple of TDECQ measurements showing margin to the 802.3cd specs (draft 3.0 definition)
- More results anticipated in January