

# 10 Mb/s Single Twisted Pair Ethernet 10BASE-T1L MDI Return Loss

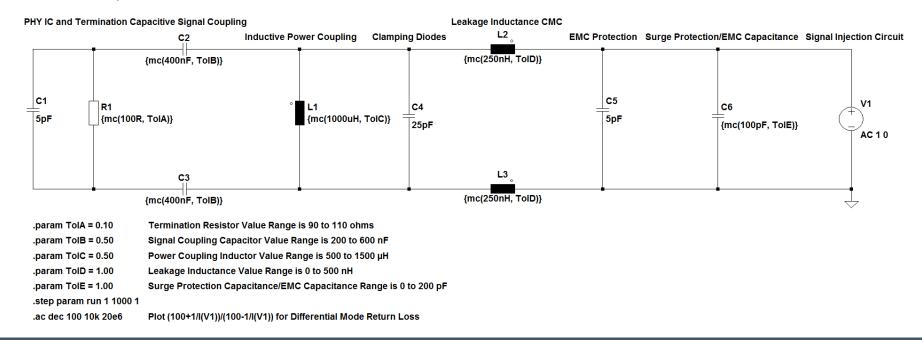
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### Content

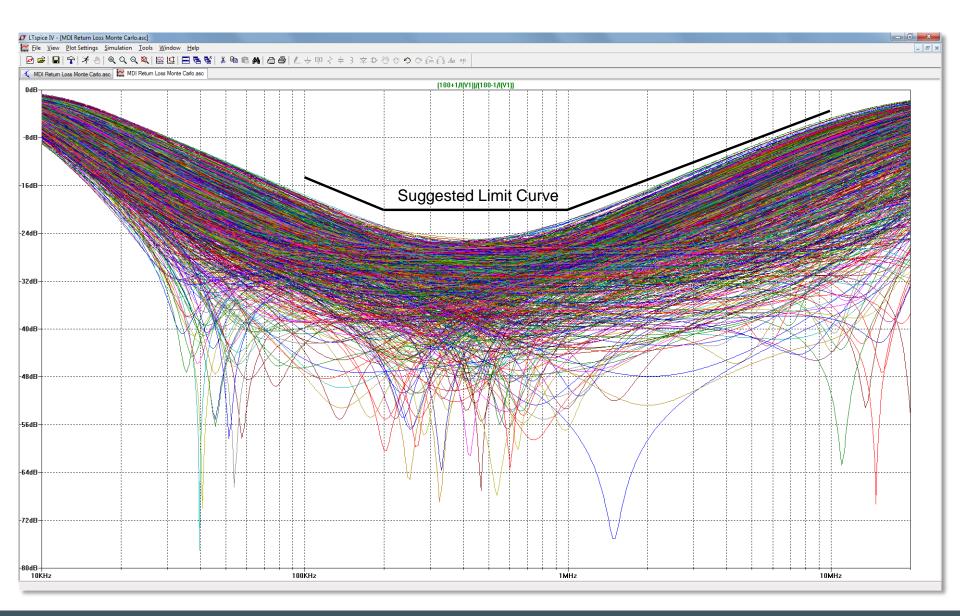
- MDI Return Loss Simulation
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#### **MDI Return Loss Simulation**

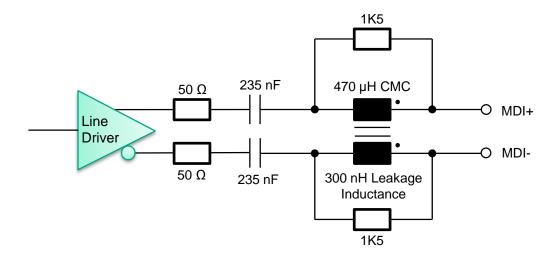
- The MDI Return Loss of a 10BASE-T1L PHY has been simulated using a simple LTSpice model with the following parameters:
  - PHY termination resistance: 90 to 110  $\Omega$  (100  $\Omega$  ± 10 %) in parallel to 5 pF parasitic capacitance
  - Signal coupling capacitance: 200 to 600 nF (400 nF ± 50 % to allow DC biasing and have a minimum of 200 nF)
  - Power coupling inductors: 500  $\mu$ H to 1500  $\mu$ H (1000  $\mu$ H ± 50 %)
  - Clamping diodes across the power coupling inductors: 25 pF
  - CMC leakage inductance: 0 to 1 μH (500 nH ± 100 %)
  - EMC/ESD Protection: 5 pF
  - Surge protection and other EMC capacitances: 0 to 200 pF (100 pF ± 100 %)
- With the LTSpice model a Monte Carlo simulation has been run with the above mentioned tolerances.



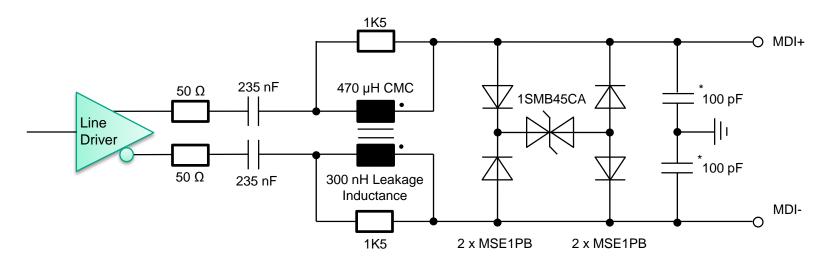
## **MDI Return Loss Simulation**



- To verify the simulation results the MDI Return Loss has been measured with a typical FPGA based Evaluation Board.
- To perform the measurement, the signal transmission (not the driver) of the Evaluation Board has been disabled.
- The power coupling network was not powered, but had the power supply connection being shorted.
- For each of the following measurements the termination resistors were changed to 45  $\Omega$ , 50  $\Omega$ , and 55  $\Omega$  (90  $\Omega$ , 100  $\Omega$  and 110  $\Omega$  differential resistance).
- The following setups have been measured:
  - PHY including a 470 μH CMC, in parallel with two 1500 Ω resistors to prevent resonance effects, without additional EMC protection (no ESD/surge/EFT protection):

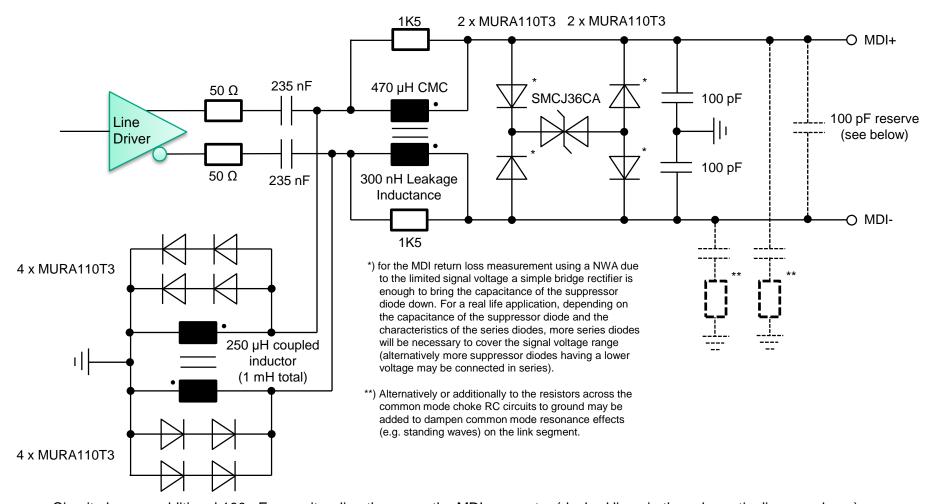


• Standard Evaluation Board EMC protection (470 µH CMC, ESD/simple surge protection (5 pF), 100 pF capacitor from each line to ground (50 pF differential capacitance)):



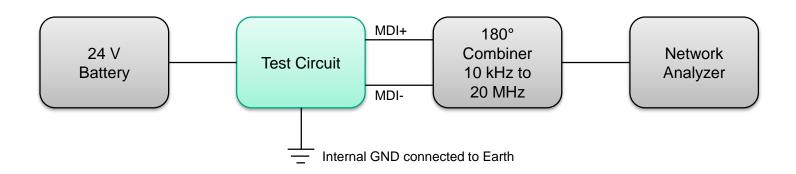
<sup>\*)</sup> A good matching (± 1 % to ± 2 %) of the EMC capacitors to GND is important for a good EMC behavior.

• Standard Evaluation Board EMC protection + PHY side PoDL power injection circuit (1 mH and clamping diodes (25 pF)) + additional robust surge protection (additional 50 pF differential capacitance):

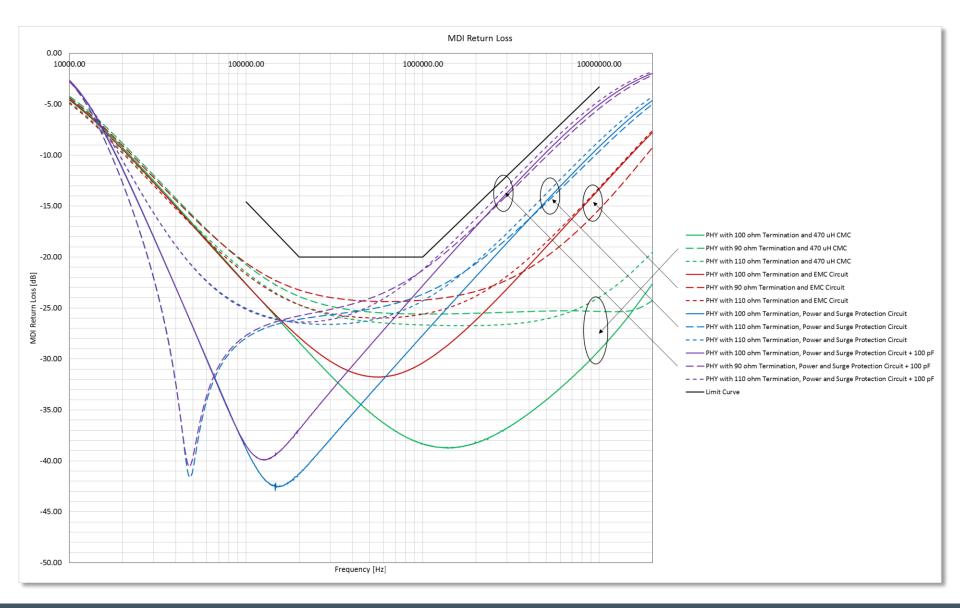


Circuit above + additional 100 pF capacitor directly across the MDI connector (dashed lines in the schematic diagram above).

The following measurement setup has been used for the MDI return loss measurement:



- As test circuit the circuits described on the three previous pages have been used.
- As combiner a Mini Circuits ZFSCJ-2-2-S splitter has been used.
- The network analyzer has been calibrated to the MDI port position.



#### **MDI Return Loss Limit Curve**

 Based on the simulation results and the measurements with the FPGA based evaluation board the following limits for the MDI return loss are suggested:

$$MDI\ Return\ Loss\ \geq \begin{cases} 20\ dB\ -18\ dB\cdot log_{10}\bigg(\frac{0.2\ MHz}{f_{MHz}}\bigg) & for\ 0.1\ MHz \leq f < 0.2\ MHz\\ for\ 0.2\ MHz \leq f \leq 1\ MHz\\ 20\ dB\ -16.7\ dB\cdot log_{10}\bigg(\frac{f_{MHz}}{1\ MHz}\bigg) & for\ 1\ MHz < f \leq 10\ MHz \end{cases}$$

- The suggested MDI Return Loss limit curve is similar to the MDI Return Loss limit curve of 1000BASE-T1, scaled down in frequency by a factor of 100 (as 1000BASE-T1 transmits 750 MS/s vs. 7.5 MS/s for 10BASE-T1L).
- While 1000BASE-T1 has a base line of the MDI Return Loss limit curve of 18 dB, the base line of the suggested 10BASE-T1L Return Loss limit curve is 20 dB as it is also for 100BASE-T1.

# **Thank You**