



Canova Tech

The Art of Silicon Sculpting

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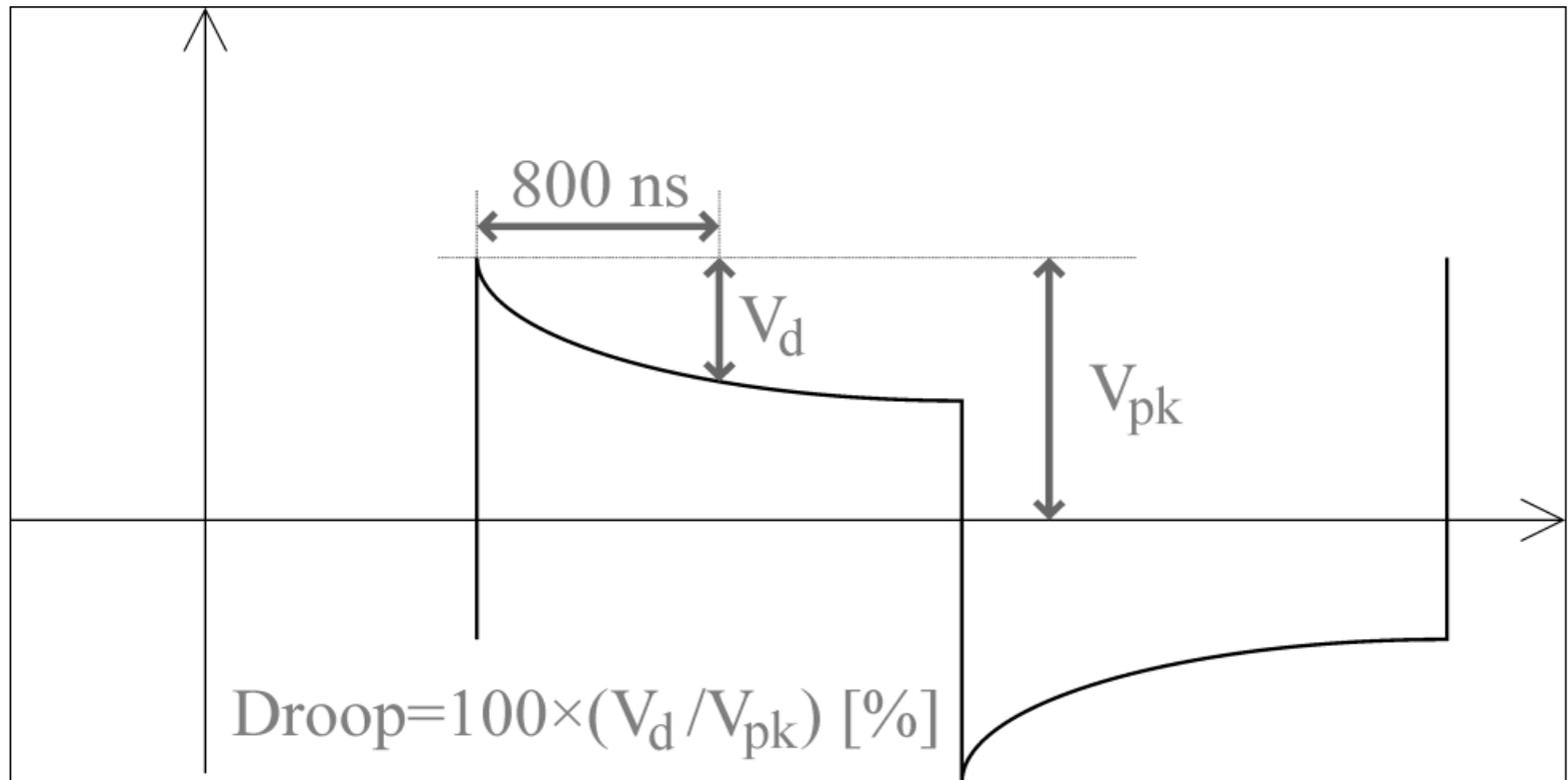
IEEE802.3cg TF

T1S transmitter droop

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- To allow for reliable measurement, the duration of the pulses must be significantly greater than nominal bit period
- Proposed to define the transmitter test mode 2 with 20 bit time duration, to allow measurement after 10 bit time (800ns nominally)
- Droop shall be lower than 30%
 - Equivalent to 30dB SNR

- Proposed droop measurement



Text changes: test mode 2 definition

- Increase the duration of positive and negative level transmitter output in test mode 2 — not DME. Proposed to change in 147.5.1,
- Change “When test mode 2 is enabled, the PHY shall transmit ten +1 symbols followed by ten -1 symbols. This sequence is repeated continually” with “When test mode 2 is enabled, the PHY shall transmit a positive differential voltage for twenty nominal bit periods followed by a negative differential voltage for twenty nominal bit periods at $1V_{pp} \pm 30\%$ amplitude. This sequence is repeated continuously”

- Add a paragraph for defining the transmitter output droop test, between “147.5.3.1 Transmitter output voltage” and “147.5.3.2 Transmitter timing jitter”
- 147.5.3.2 Transmitter output droop
- Transmitter output droop shall be measured using test mode 2 and with the test fixture shown in Figure 147–11. The magnitude of both the positive and negative droop measured with respect to the initial peak value after the zero crossing and the value 800 ns after the initial peak, shall be less than 30%.