IEEE P802.3cg
10BASE-T1S Detection of Collisions on a Mixing Segment

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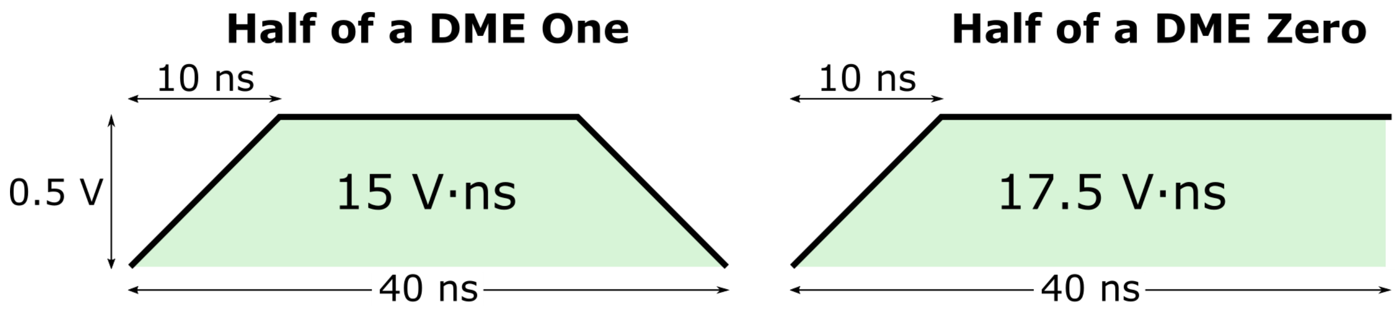
Purpose

- Inspired by Comment i-417
- Questions to be addressed:
  - When operating a T1S mixing segment, can collisions be detected based on the signal present at the MDI?
    - See also beruto_3cg_collision_detection
  - Is echo cancellation required in order to detect collisions on a mixing segment?

DME Signal Integration

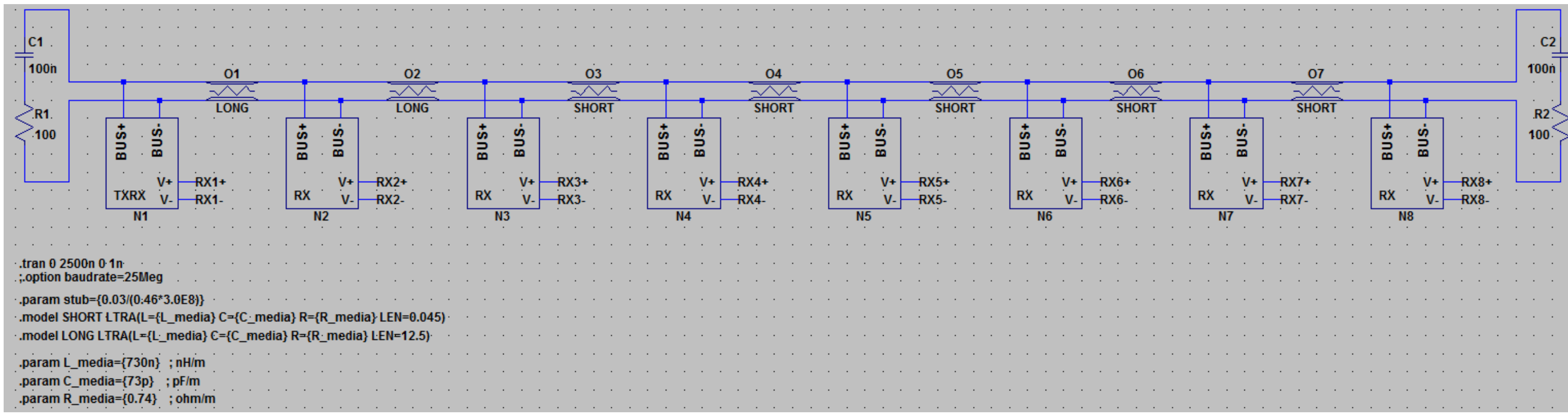
- PHY may incorporate an integrator for signal detection
  - Analog or digital integrator
- Expect magnitude between 15 – 17.5 V·ns for a 40 ns half clock period with a perfect DME signal



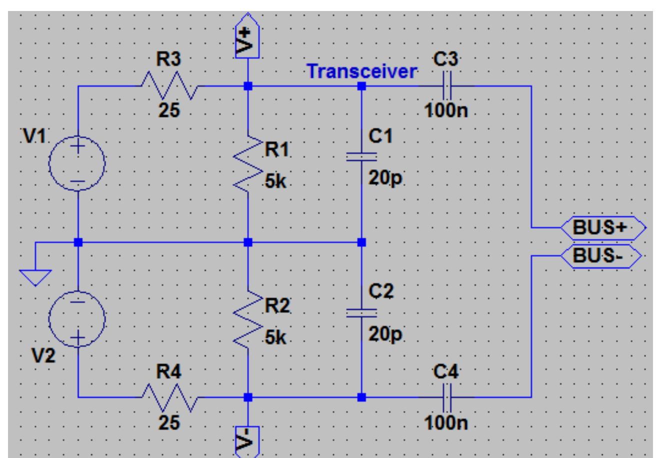
- Postulate most integrated half clock periods have a magnitude of 12.5 – 22.5 V·ns

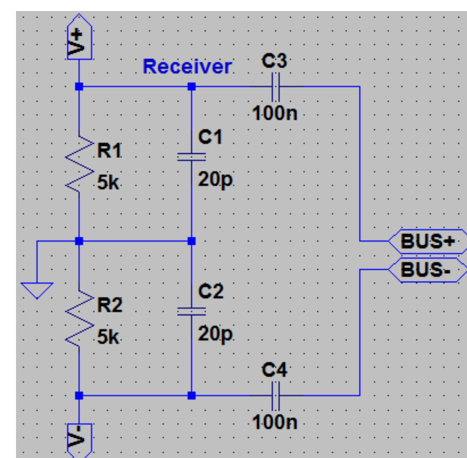
Methodology, Part 1: Spice Circuit

- Use LTSpice XVII to simulate an 8-node system, with 25 meter total cable length
- One transmitter always located at N1, on left side of bus



- Nodes modeled as:
  - 10 kΩ resistor
  - 10 pF capacitor
- Transmitter has 50 Ω output impedance
- No echo cancellation!



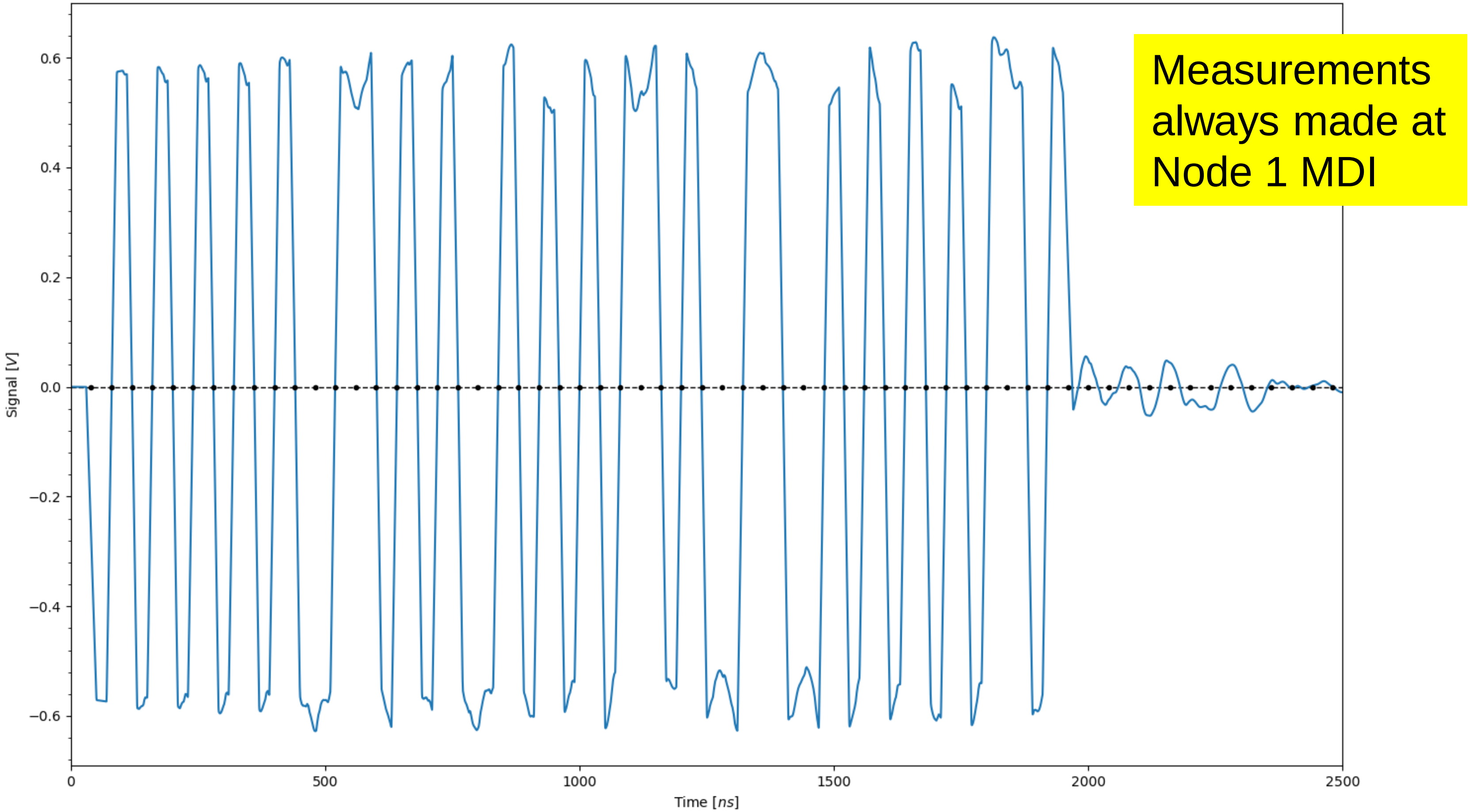


Methodology, Part 2: Configurations

- Three node configurations are used:
  - **Equal:** Node spacing fixed to 3.57 m
  - **Approximately Equal:** Node spacing obtained from 1-D Dirichlet distribution (α=2)
  - **Clumped:** TX at N1 on left side of bus, all other nodes at other end of 25 meter cable with fixed spacing (randomly chosen) between 5-100 cm
- Two configurations for second TX:
  - **No second TX** (no collision; control case)
  - **Second TX** placed in randomized location (N2 – N8)
    - Both transmitters have identical start time (perfectly in-phase)
- Two configurations for second TX bit pattern:
  - **Identical bit pattern** to first TX (except 1 bit may flipped)
  - **Random bit pattern** (no intended correlation to first TX)

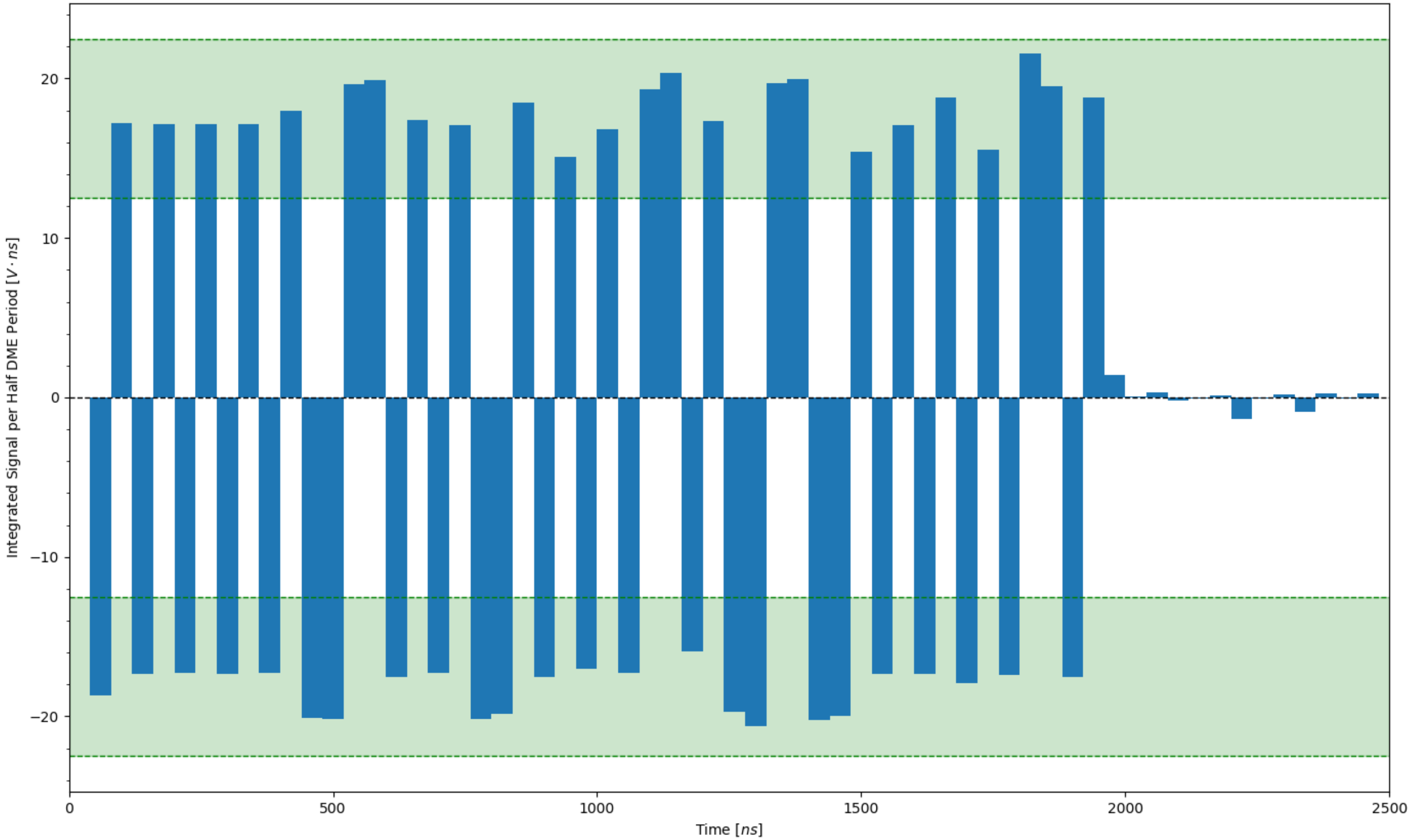
Methodology, Part 3: Raw DME Signal

- Randomly generated 24-bit signal (starts at 40 ns, 1920 ns long)
- TX at low-impedance for entire simulation window
- Half clock cycle division locations shown with black dots on x-axis



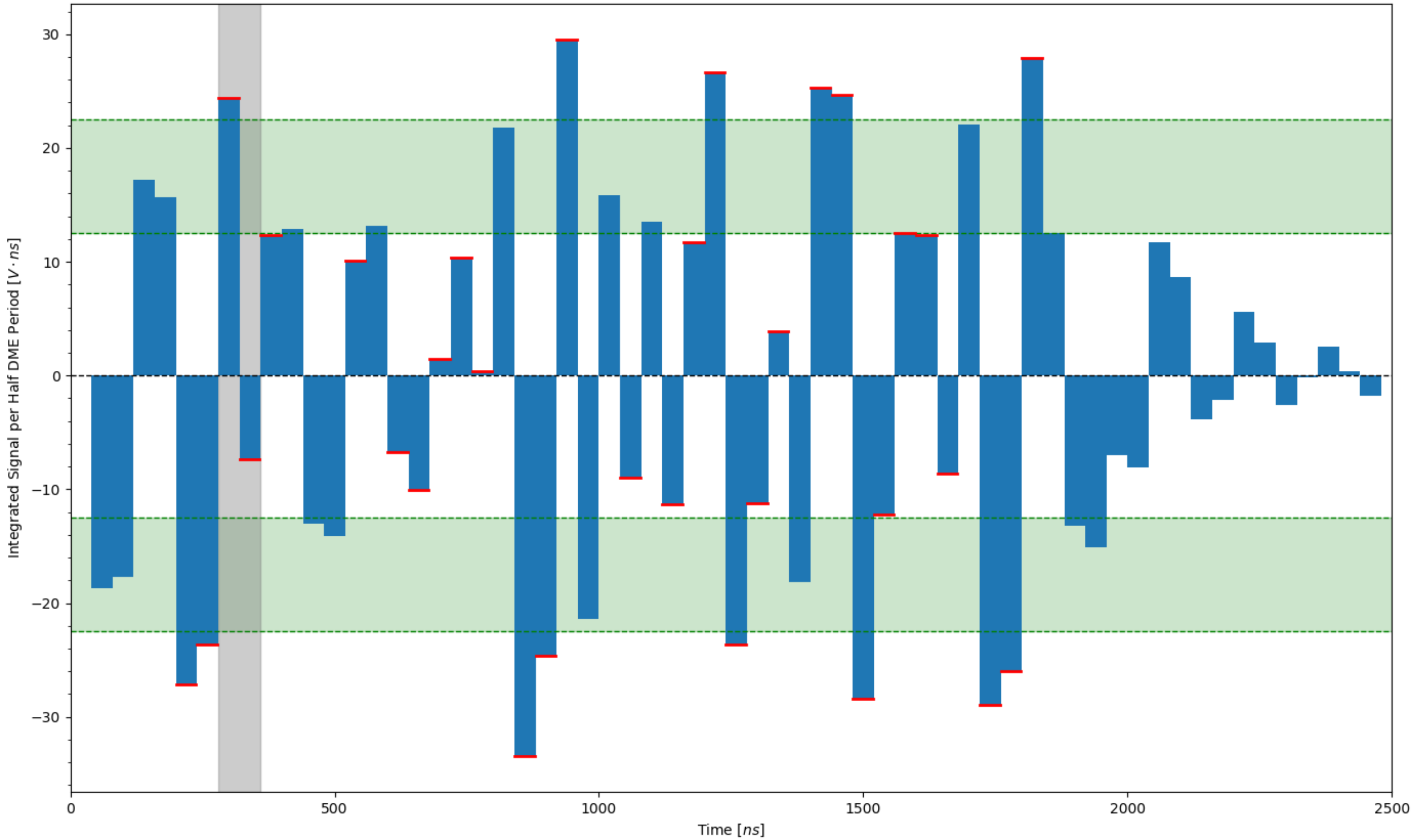
Example 1: One TX, No Collision

- 8 nodes, equal spacing, bit pattern = 0xF9BA3D
- Signal integrated each 40 ns half clock period
- Signal is found to lie within 12.5 – 22.5 V·ns bands, indicating no collision



Example 2: Collision

- 8 nodes, appox. equal spacing, second TX at N6 position
- Signal = same as 1st TX, except bit 3 is flipped (shaded gray band)
- Red-capped bars indicate excursions outside of 12.5 – 22.5 V·ns bands



Test Results

Second TX (if present) uses same bit pattern*

- Total trials: 4981
- Trials with second TX: 4332
- Trials w/o second TX: 649
- Failed detections: 0
- False positives: 16
- Error rate: 0.32%

Second TX (if present) uses random bit pattern

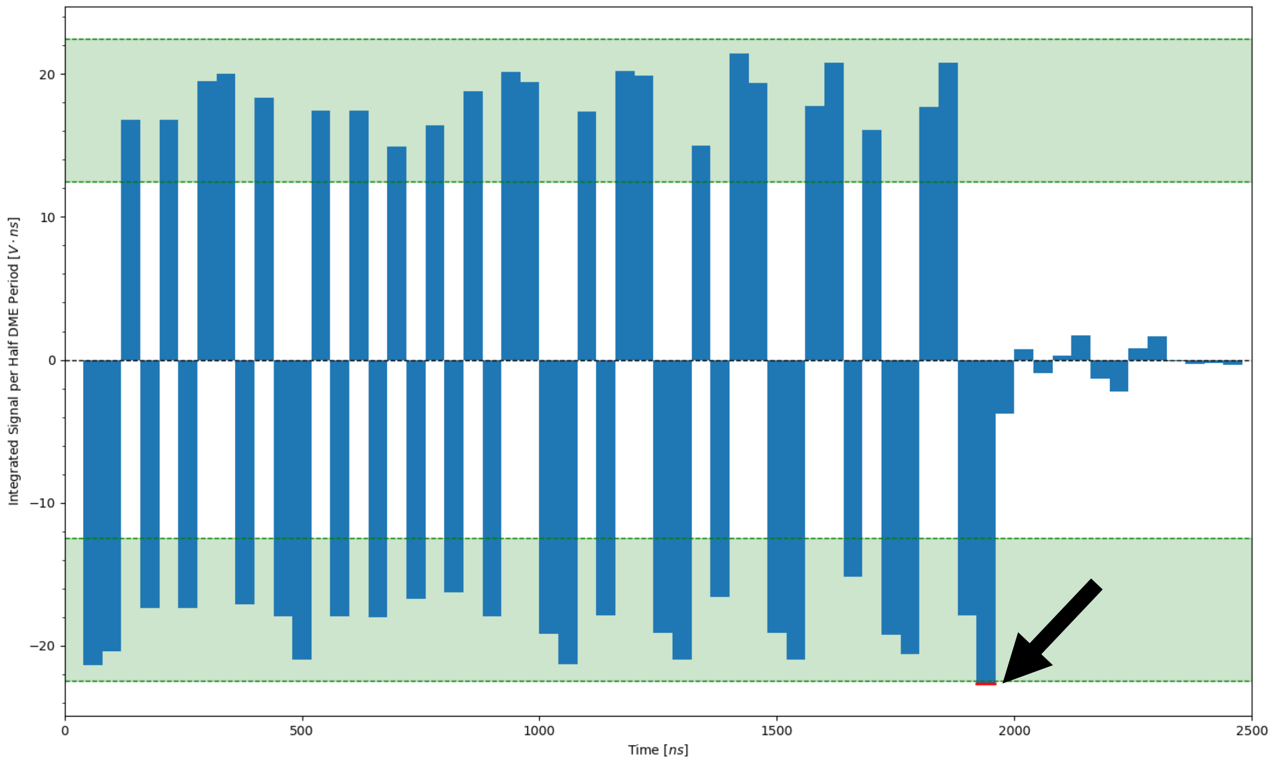
- Total trials: 5262
- Trials with second TX: 4587
- Trials w/o second TX: 675
- Failed detections: 0
- False positives: 19
- Error rate: 0.36%

Method achieves **100% detection** of collisions!

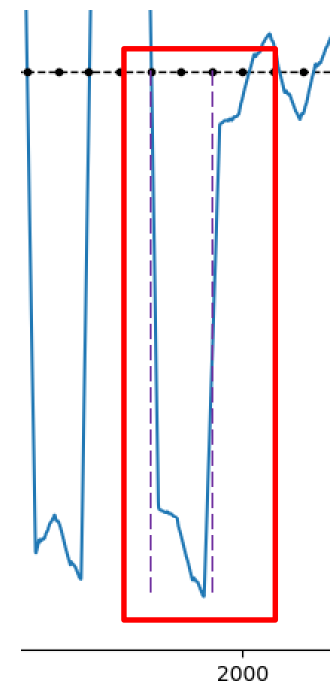
*Same bit pattern, with possibly 1 bit flipped. Location of flipped bit chosen randomly.

False Positives

- Only occurred for one bus topology: clumped
  - All (except one outlier) occurred on last bit, which was always a DME 0
  - Always just a little too high -- integrated a little too much
  - Due to transition to driving 0 V?



Raw Waveform



Required Time To Detect A Collision?

Table 147-6 prescribes a response within 25.6 µs – 256 bit times at MAC

Table 147–6—10BASE-T1S delay constraints

Event	Minimum value	Maximum value	Unit of measure	Input timing reference	Output timing reference
COL input to CRS asserted	0	25.6	µs	Start of corrupted transmitted signal at the MDI	Rising edge of CRS
COL input to CRS deasserted	0	3.2	µs	End of transmission at the MDI	Falling edge of CRS

Probably we should respond within the jamSize (32 bits)

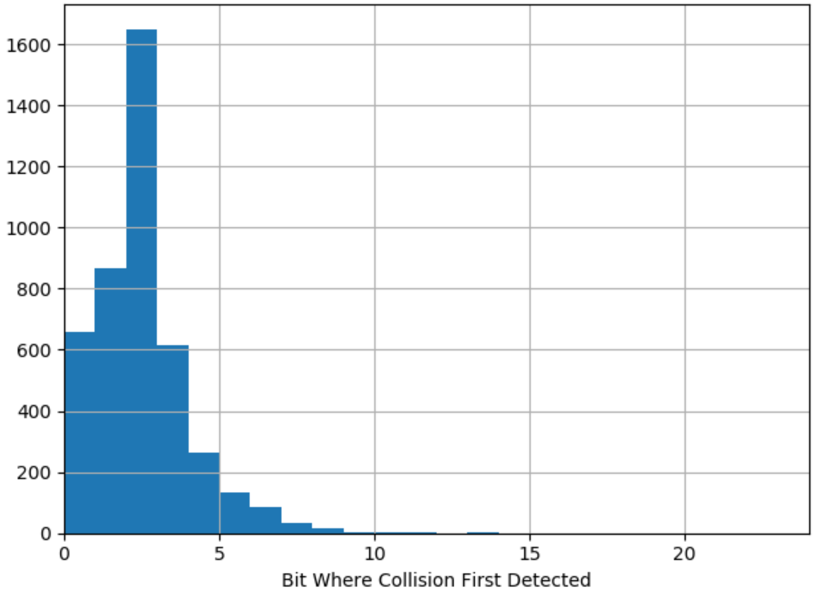
Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	1 Gb/s	2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s	10 Gb/s
jamSize	32 bits	32 bits	not applicable	not applicable

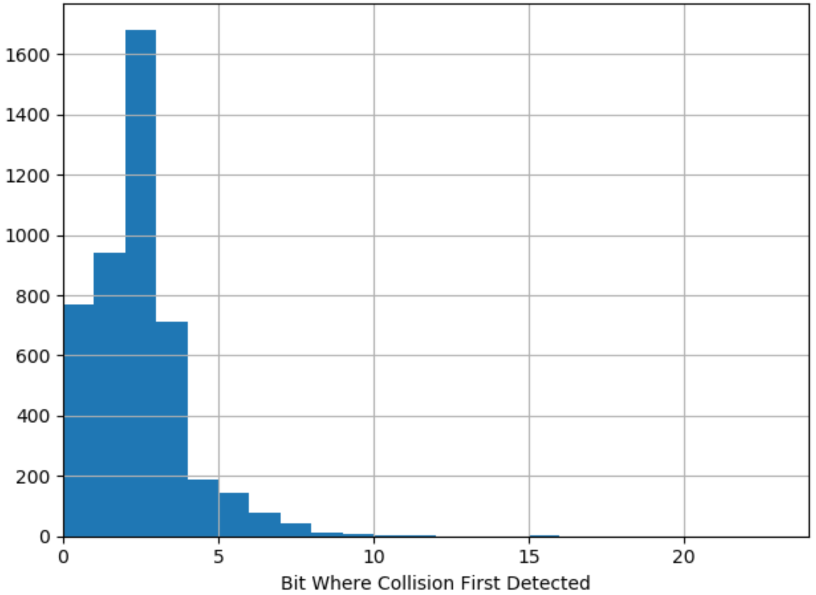
Timing Results

- Track the first bit with an integral outside the 12.5 – 22.5 V·ns bands
- Collision always detected within DME 16 bits (12.8 bit times at MAC)
- In most cases, detection within the first 5 DME bits

Second TX (if present) uses same bit pattern*



Second TX (if present) uses random bit pattern



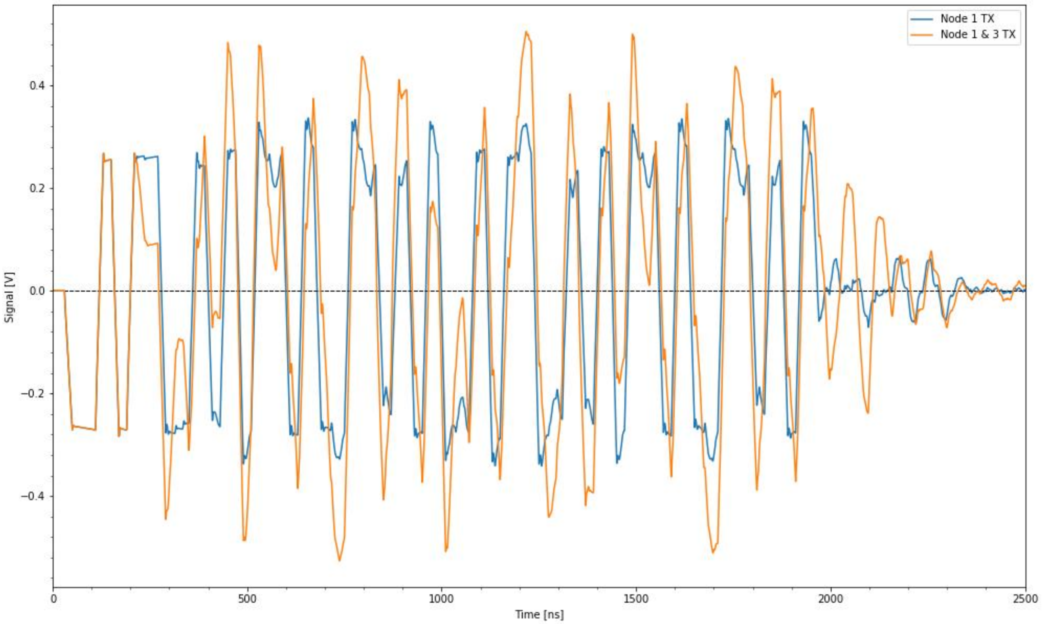
*Same bit pattern, with possibly 1 bit flipped

Alternative Methods

- Couldn't the same thing be accomplished by using the waveform amplitude instead of the integrated signal?
  - Yes, probably.
  - Probably would need to sample the signal multiple times in one 40 ns period.
  - Integration can be done with a simple analog integrator.

This plot shows a comparison between the MDI signal at Node 1 with:

- Only Node 1 transmitting (blue)
- Node 1 and Node 3 transmitting (orange)



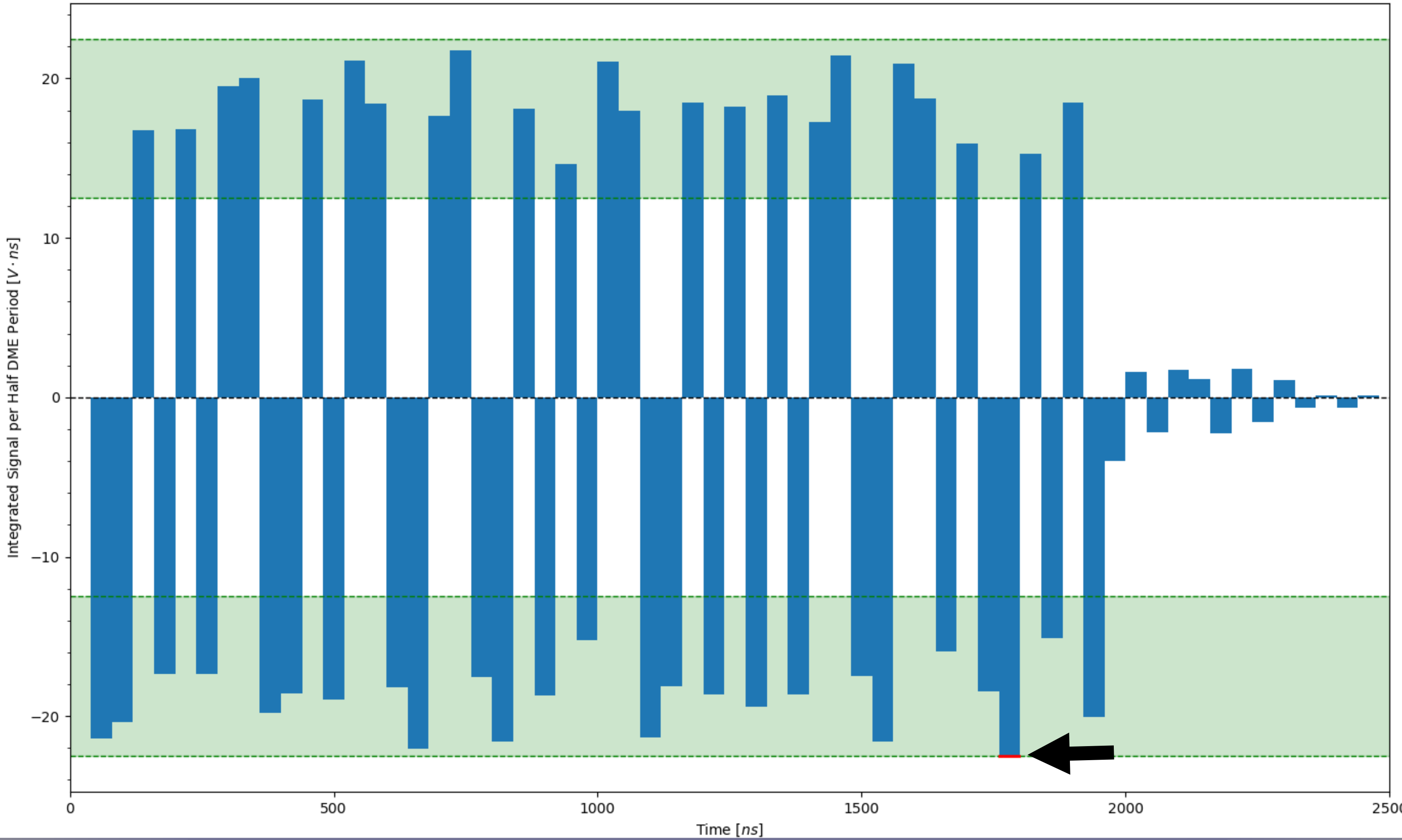
Conclusions

- We have demonstrated a viable collision detection mechanism for a mixing segment
  - Echo cancellation was not used
  - Integral bands naively selected *a priori*
  - No optimization performed
  - 100% collision detection
- Few false positives for clumped topology
  - May be due to specifics of simulation setup
  - Optimization likely to eliminate the problem
- Collisions detected promptly
  - Within 16 clock cycles/DME bits

Thank you!

Outlier False Positive

- Only 1 in 10000 simulation showed a false positive not on the last bit
- Clumped spacing, nodes spaced 5.2 cm apart

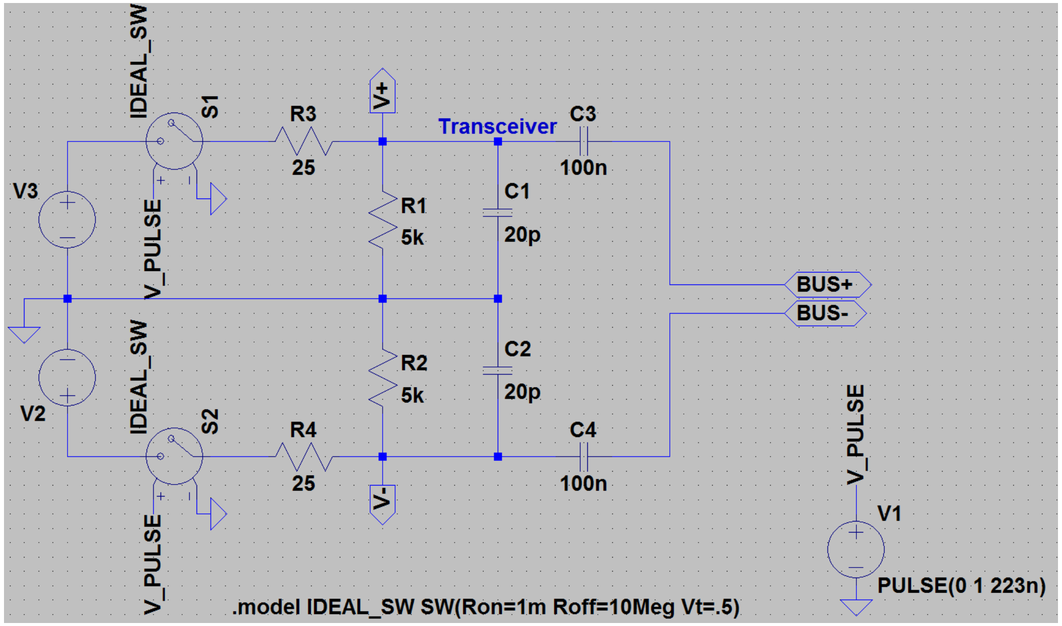


Appendix: Non-Overlapping TX Collision

- Extended study to investigate what happens when the second transmitter starts later than the first TX

LTSpice model of second transmitter

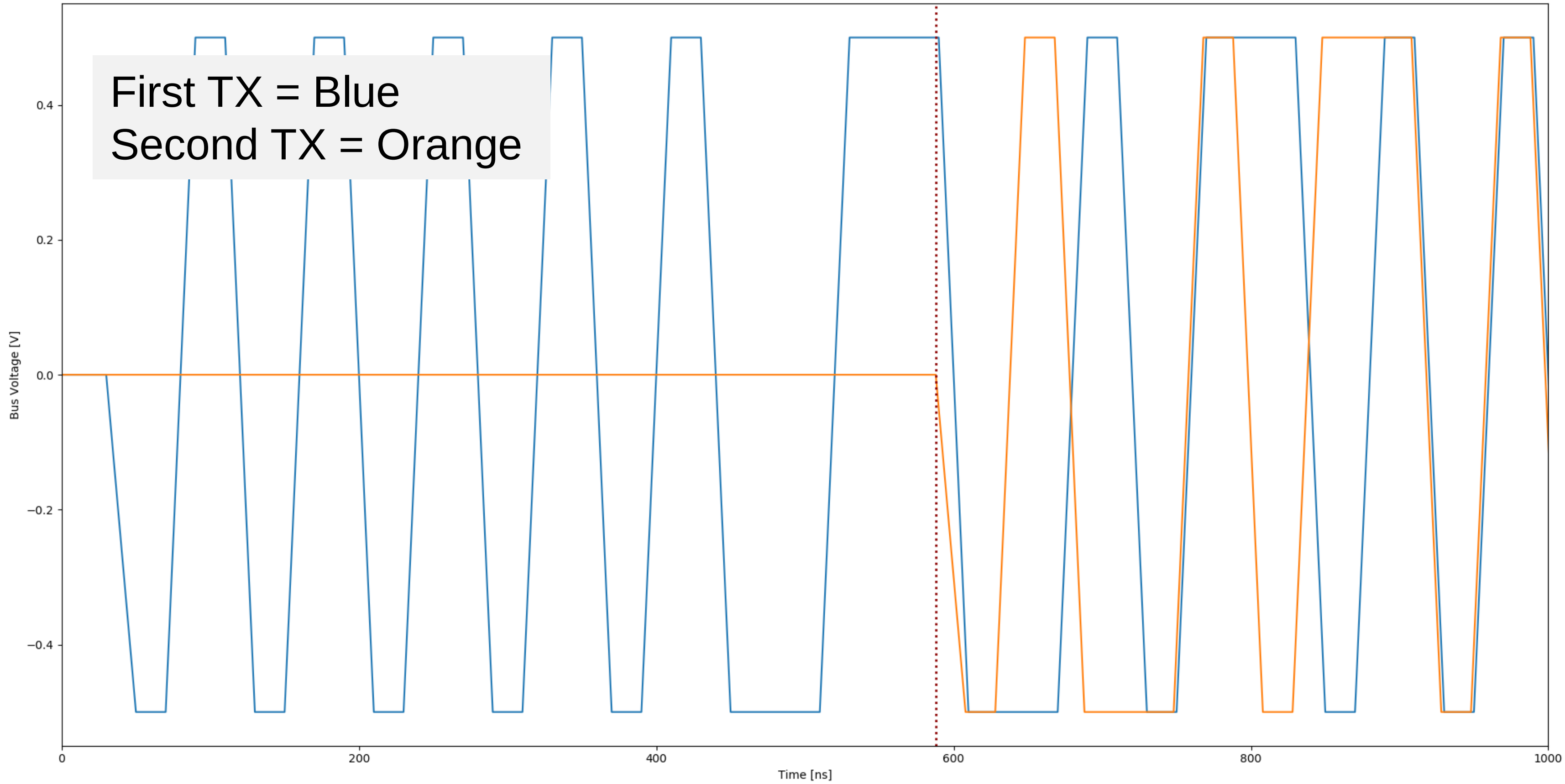
- Initially high impedance (10 kΩ)
- Ideal switches connect voltage sources, TX becomes low impedance
- Timing of V_PULSE randomized.



- Second TX waveform delayed by random amount
- Extended simulation to 48 bits to capture overlap

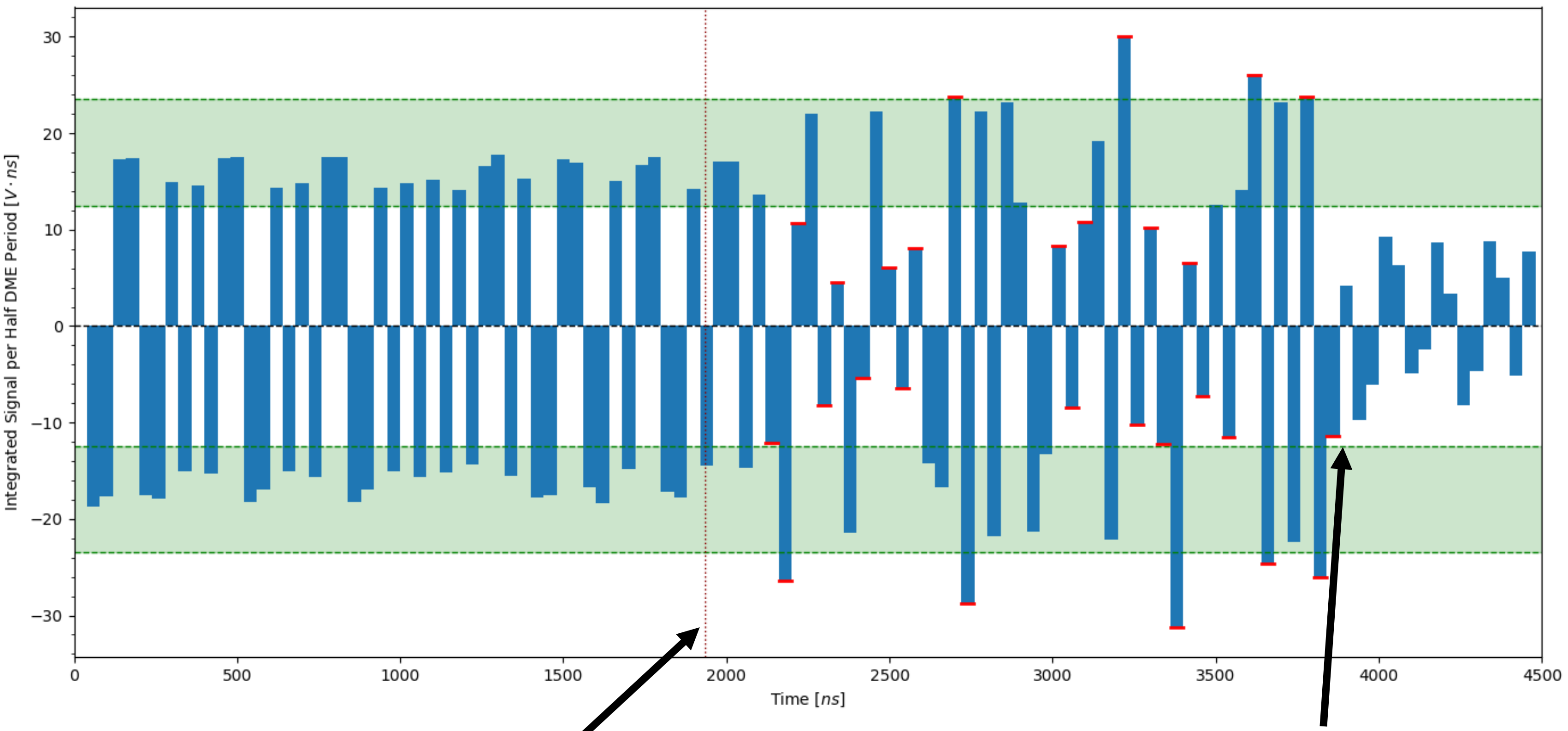
Example: Non-Overlapping Waveforms

- Second TX waveform is offset by a random amount from the first (here, 588 ns)
  - In this example, the waveforms happen to align fairly closely
- Second TX is allowed to start anywhere in the first 24 bits



Example: Non-Overlapping 2nd TX

Second TX bit pattern is random (uncorrelated) compared to first TX



Vertical dotted line indicates second TX start time

Program stops looking for out-of-range bits when 1st TX stops transmitting

Non-Overlapping 2nd TX Test Results

Integrated Signal Acceptance Magnitude:

12.5 – 23.0 V·ns

- Total trials: 5509
- With Second TX: 4810
- W/O Second TX: 699
- Failed detections: 0
- Detection, no 2nd TX: 185
- Detection before 2nd TX active: 306
- Error rate: 8.9%

Integrated Signal Acceptance Magnitude:

12.5 – 23.5 V·ns

- Total trials: 1000
- With Second TX: 886
- W/O Second TX: 114
- Failed detections: 0
- Detection, no 2nd TX: 4
- Detection before 2nd TX active: 0
- Error rate - 0.4%

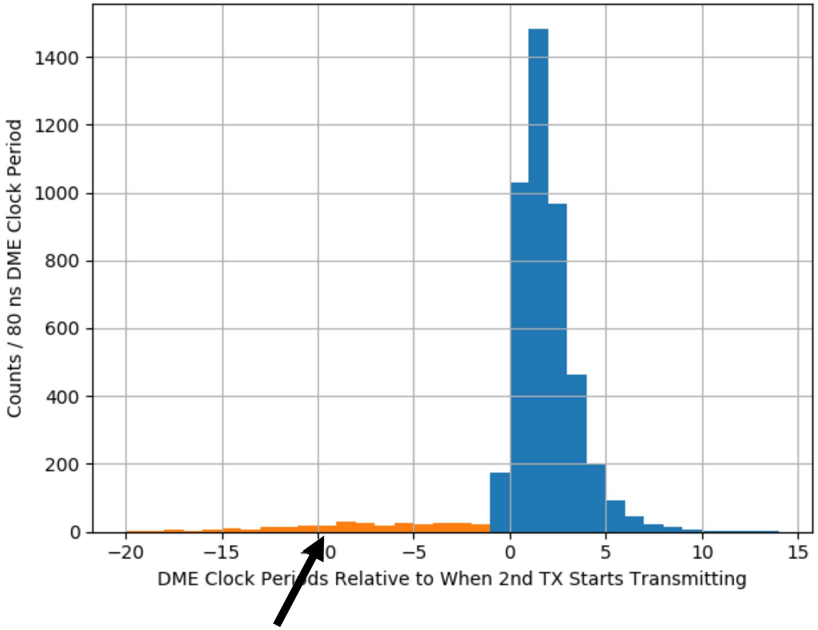
- Adjusted integrated signal acceptance bands to decrease error rate
- False positives again due to “clumped” configuration (difficult for signal integrity)

Method achieves **100% detection** of collisions!

Non-Overlapping 2nd TX Test Results

Integrated Signal Acceptance Magnitude:

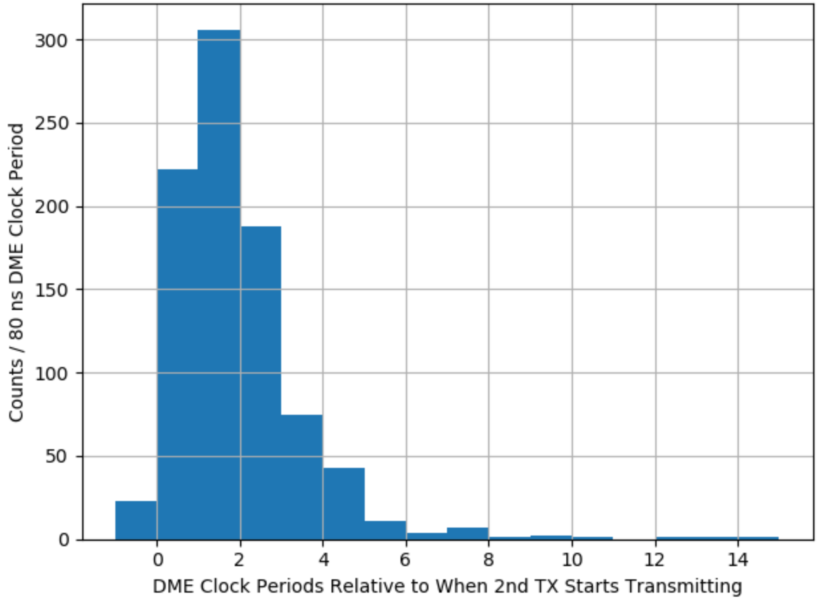
12.5 – 23.0 V·ns



Orange results are detections before 2nd TX started transmitting (false positives)

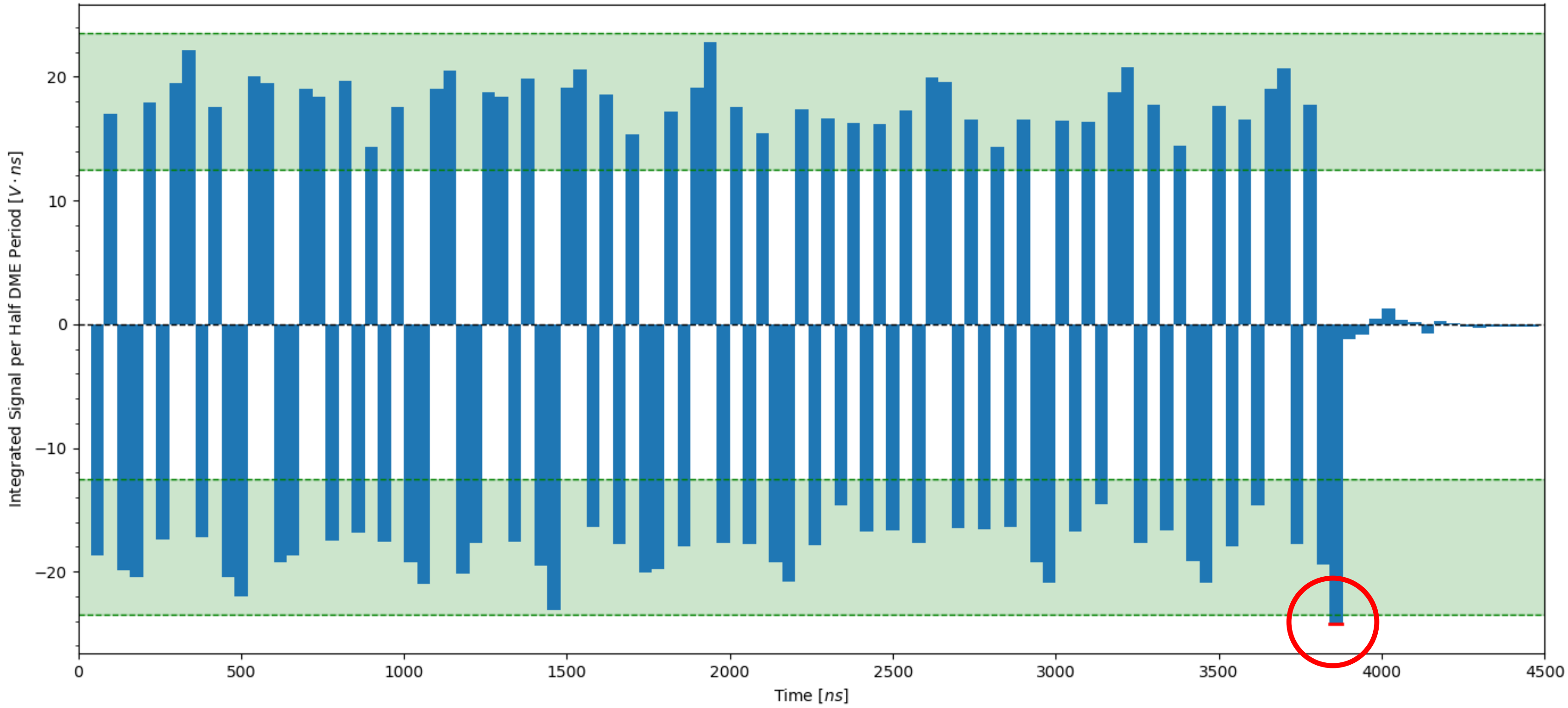
Integrated Signal Acceptance Magnitude:

12.5 – 23.5 V·ns



Data falling in -1 bit bin are okay; indicates 2nd TX started in the middle of the bit, and the bin number was rounded down

Non-Overlapping 2nd TX False Positives



- False positives are always in “clumped” case
- For increased 12.5 – 23.5 V·ns band, all four false positives looked identical: too much signal in last half bit of DME zero
- Partially due to mistake in program that generates DME waveform
  - Incorrect rise/fall times when transitioning to high-Z