Preliminary Study of Noise Effects on Multi-Gigabit Automotive PHY Designs

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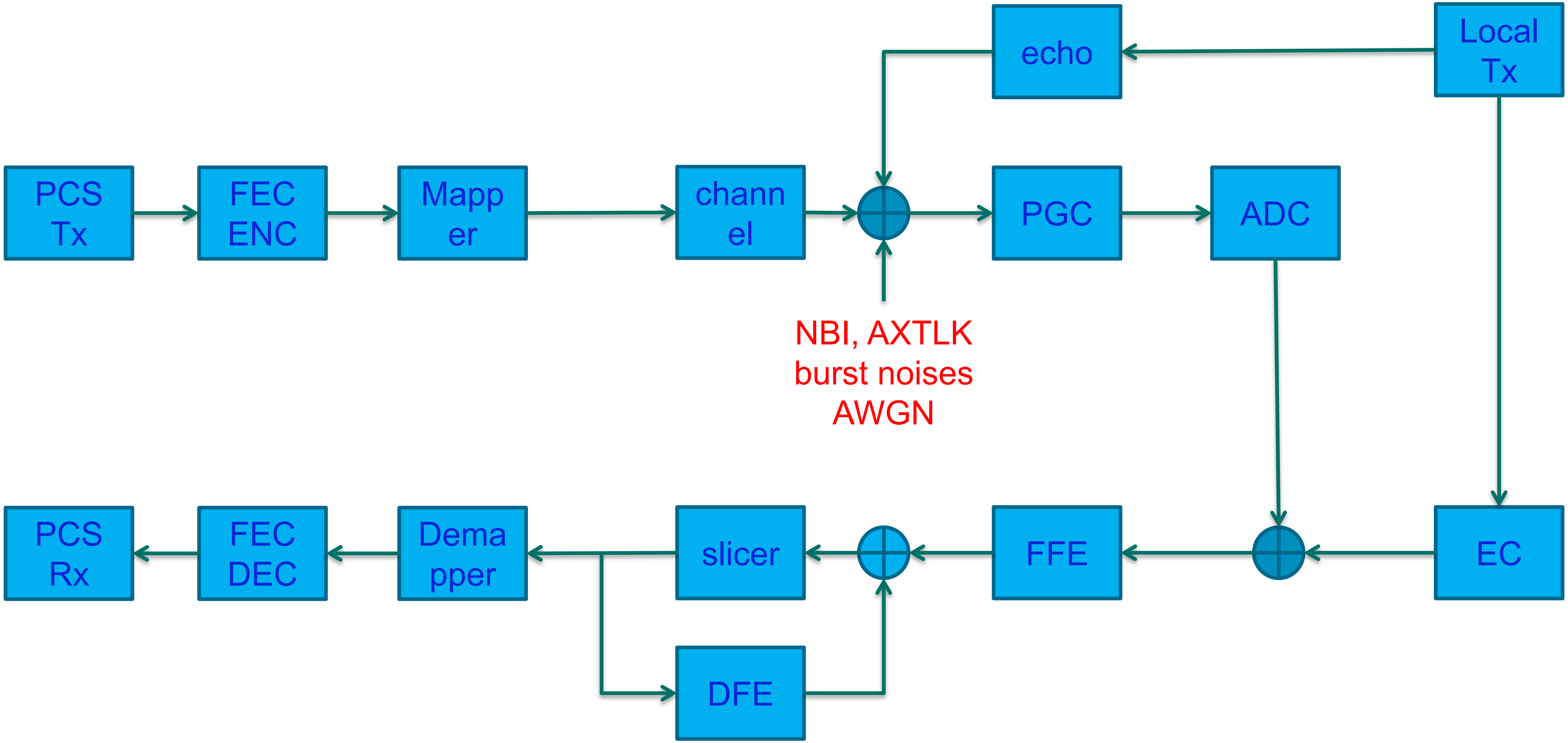
Automotive Noises at PHY Receiver

- Burst noises
  - Fast transients: model exists for 1000BASE-T1 UTP, need model for mGig Auto PHY
  - Slow transients: not an issue for 1000BASE-T1
- Narrow band interferences (NBI)
  - Frequencies and amplitudes are both time varying
- Alien crosstalk
- Wide band AWGN type noises
- Vibrations
  - Not an issue for 1000BASE-T1. How about mGig Auto PHY?
- Other noises?
- In this contribution, we mainly consider burst noises and NBI.

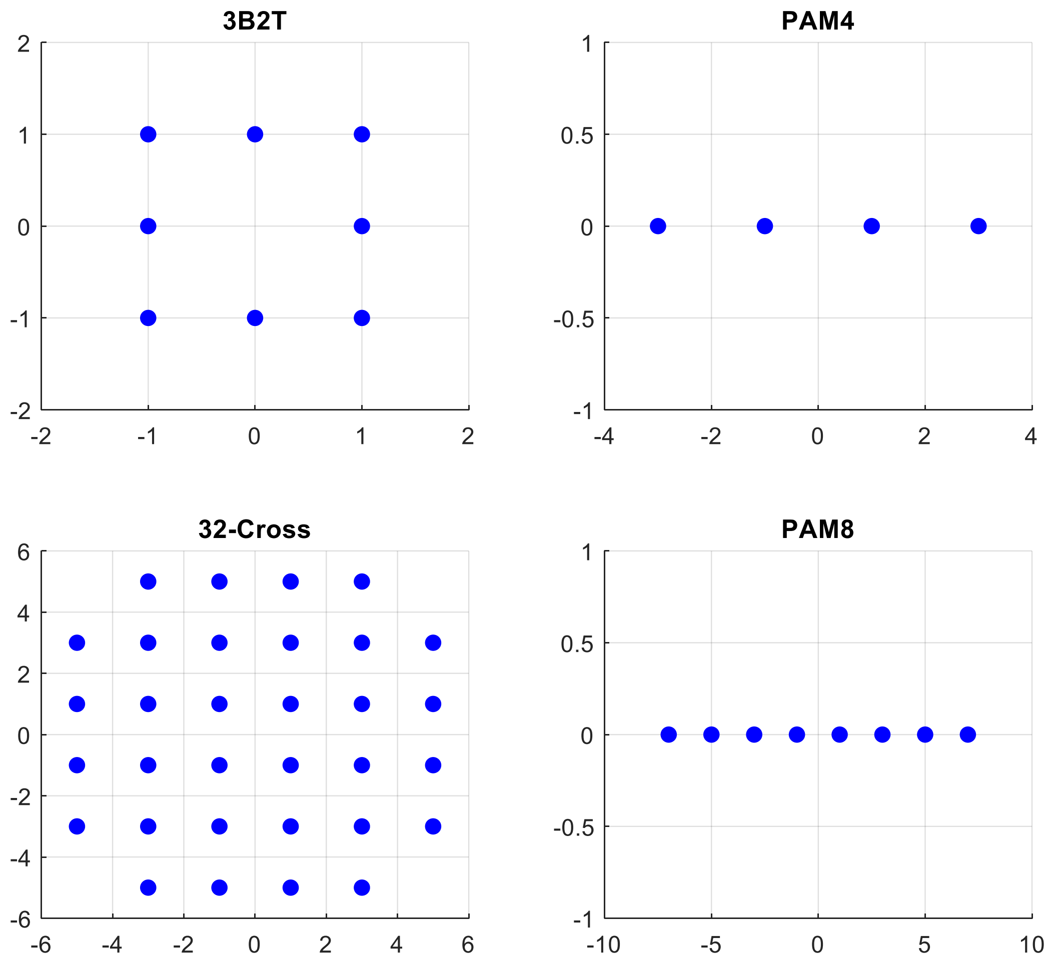
PHY Top Level Model



Impairment Mitigation at PHY Receiver

- AFE common mode rejection
- Echo cancellation
- Feed-forward (FFE) and decision feedback equalizers (DFE)
  - Compensate channel inter-symbol-interferences (ISI)
  - Stationary noise suppression
  - NBI and other time-varying noise suppressions
  - Track channel variations (e.g. due to temperature)
    - The last two requires adaptive DFE or equivalent to achieve optimal performance
  - DFE may suffer from error propagations. This becomes more severe with denser constellations and narrower channel bandwidth.
- FEC
  - Correct burst and random errors

Constellations Considered



Constellation	bits / baud	Symbol rate Mbaud
3B2T	1.5	7500
PAM4	2	5625
32-Cross	2.5	4500
PAM8	3	3750

- Maintain same 12.5% FEC + framing overhead, as in 1000BASE-T1
- For SNR margin analysis, see “souvignier_3ch_01_0518.pdf”.

SIMULATED NBI IMMUNITY VS. CONSTELLATION CHOICES

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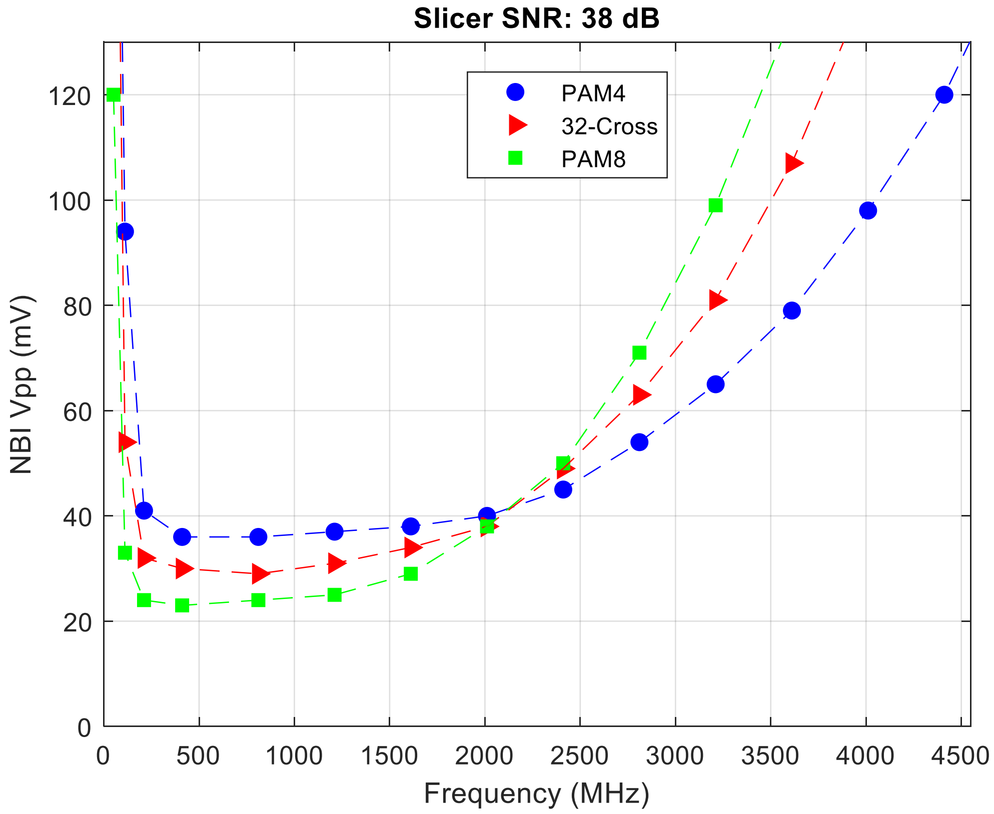
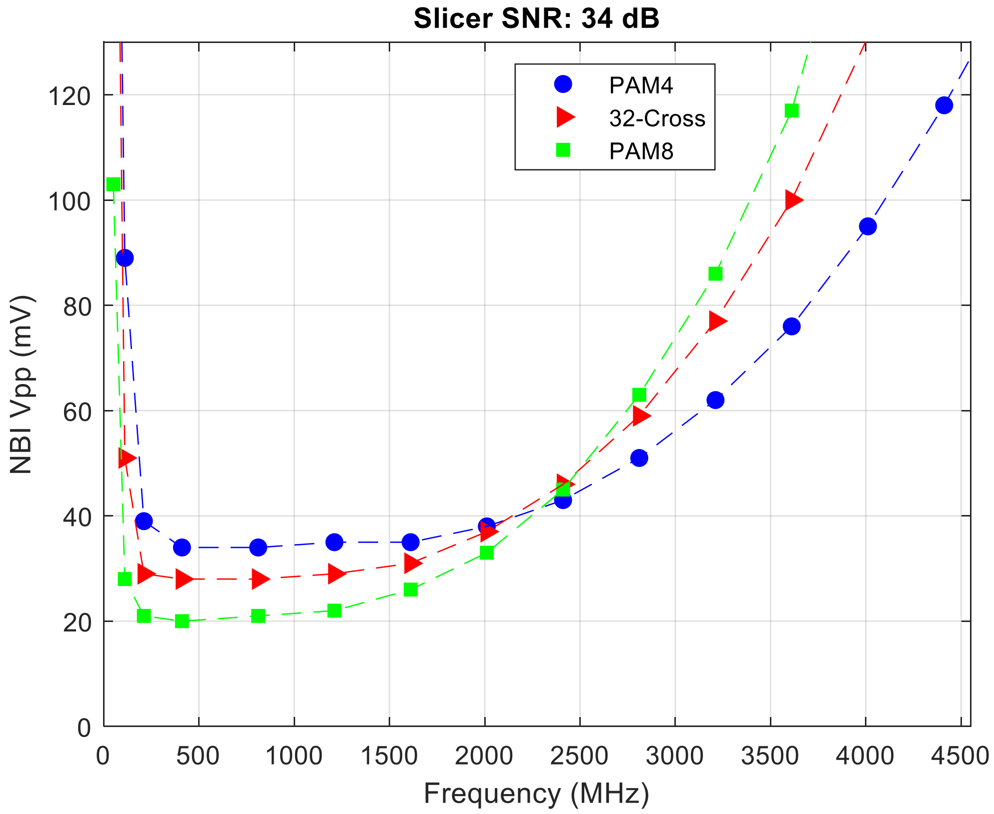
NBI Simulation Setup

- Based on channel insertion loss specified in P8023ch_D0p2p2 Equation 150-1.
- For each constellation, normalize Tx level to 3 dBm.
- Apply receiver HPF and LPF based on constellation choices.
- Calculate optimal FFE and DFE without NBI, then freeze both.
- Sweep NBI frequency
  - At each frequency look for levels exceeding decision boundaries.
  - Repeated the experiment with four different slicer SNR values

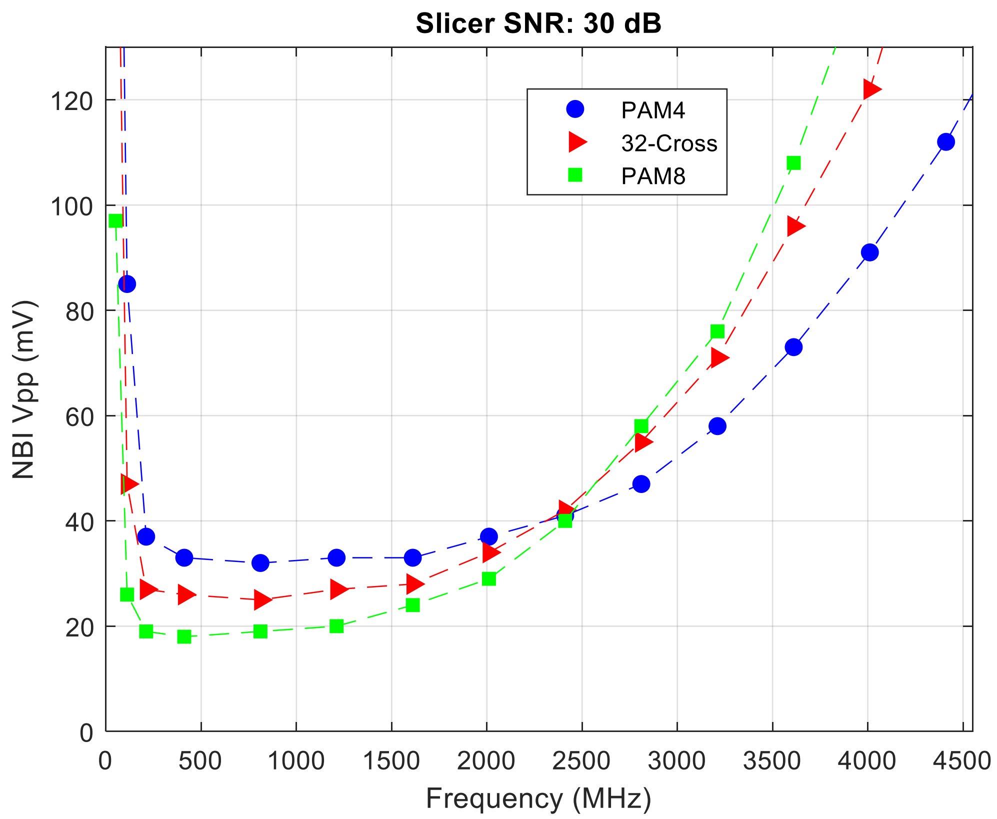
NBI Immunity Simulation Results

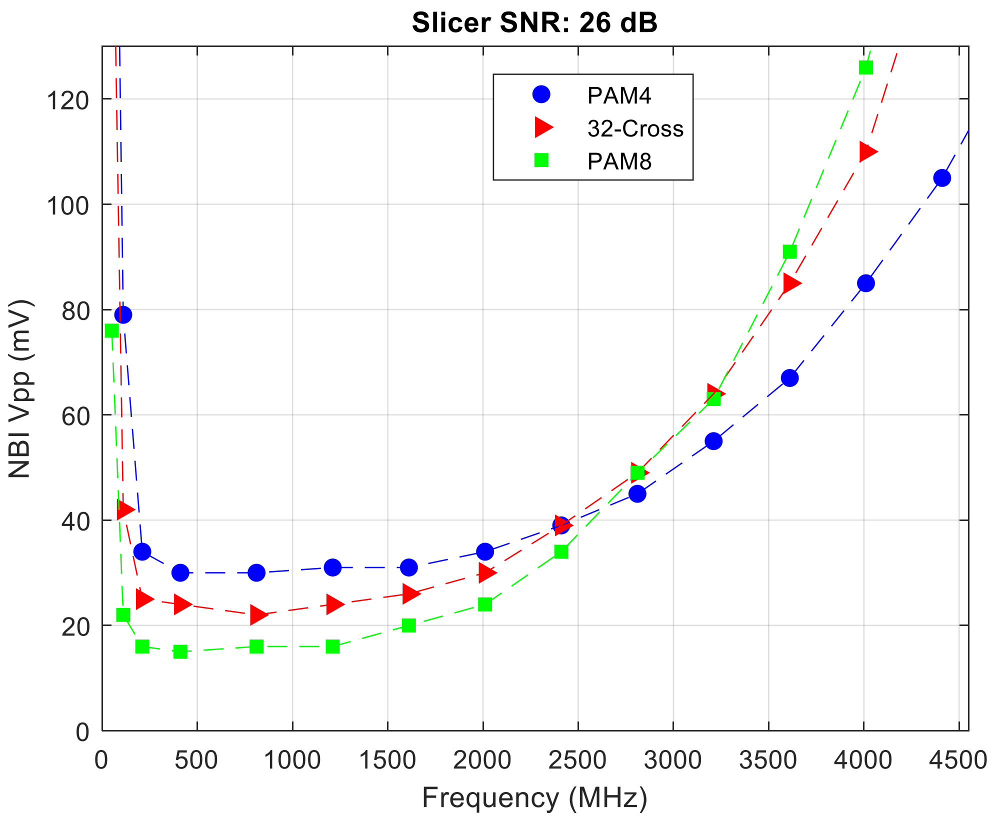




- At lower frequencies, NBI immunity increased by ~2.5dB each from PAM8 to 32-Cross to PAM4
- At higher frequencies, denser constellations have superior immunity due to lower bandwidth and analog low pass filtering

NBI Immunity Simulation Results, continued





- As the slicer SNR decreases (before adding NBI), the NBI immunity decreases as well.

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FEC CONSIDERATIONS

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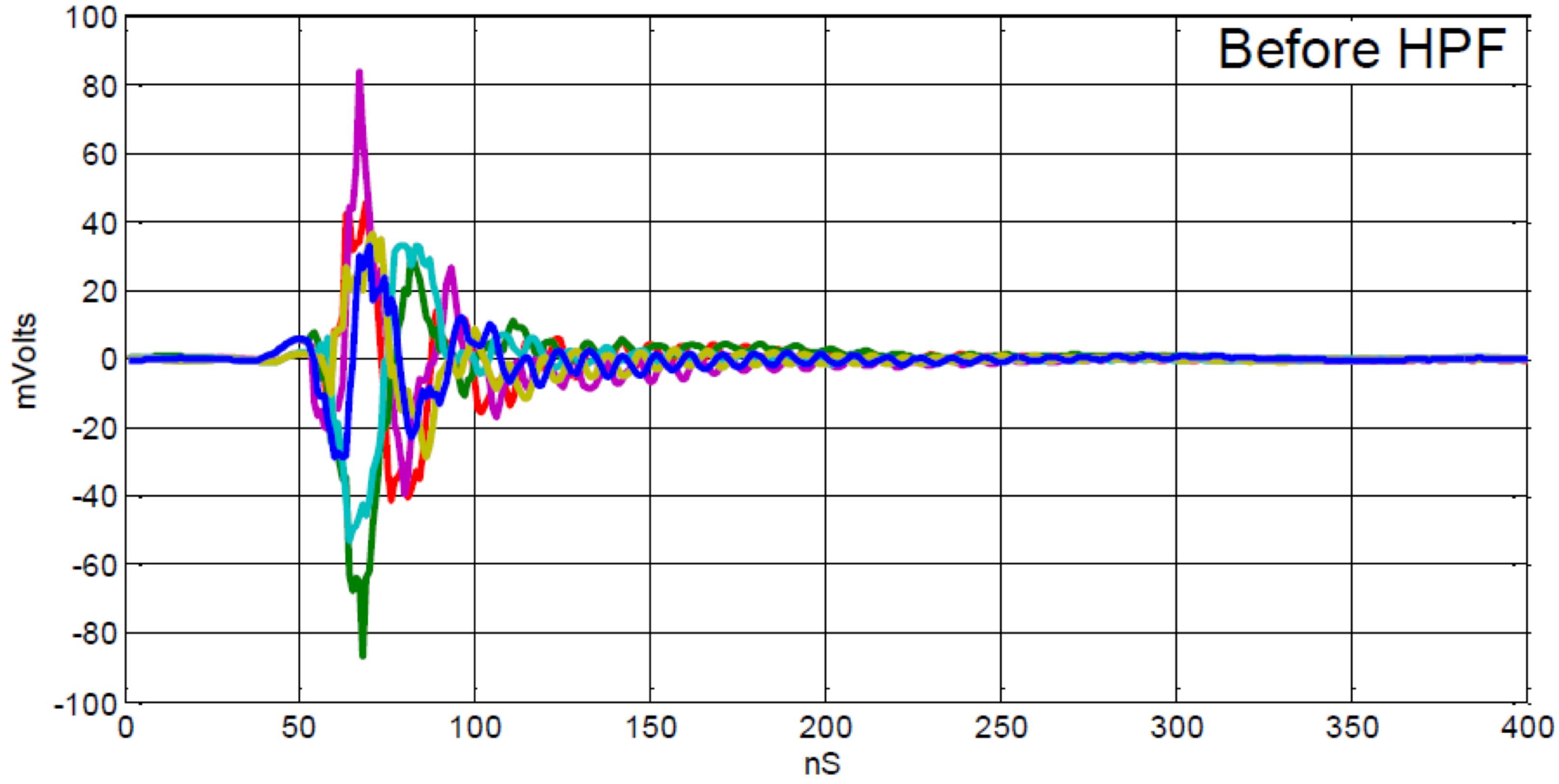
Assumed Burst Noise Model



- From 1000BASE-T1:
  - http://www.ieee802.org/3/bp/public/jan14/Chini_Tazebay_3bp_01a_0114.pdf
  - Based on ISO 7637-3 specification.
  - Each burst duration is 50nsec.
- Assume same 50nsec burst length for mGig Auto PHY.

FEC Considerations

- For 1000BASE-T1, RS FEC (N=450, K=406, m=9) was selected.
  - Code rate = 0.9022, FEC redundancy = 0.0978
  - Frame duration = 3600 ns
  - Intrinsic latency = 3952 ns
  - Max burst correction = 176 ns
    - The 176 ns burst protection covers 50 ns input burst noise + DFE error propagation + random noise protection
- For 10GBASE-T1, consider RS FEC with m=10, 11, and 12 bits/symbol.
  - Assume 50nsec input burst noises
  - Need to protect against DFE error propagation
  - Keep FEC code rate ~= 0.9
  - Keep FEC frame duration and intrinsic delay <= 1000BASE-T1 case

10GBASE-T1 RS FEC Options m=10

burst duration nsec	50.00

1000BASE-T1

Constellation	bits / baud	Symbol rate Mbaud	min # bits protected	RS m	RS N	RS K	RS N-K	FEC frame nsec	Correction nsec	FEC latency nsec	FEC redundancy
3B2T	1.5	750	57	9	450	406	44	3600.00	176.00	3952.00	0.0978

10GBASE-T1 examples

RS 10 bits / symbol

Constellation	bits / baud	Symbol rate Mbaud	min # bits protected	RS m	RS N	RS K	RS N-K	FEC frame nsec	Correction nsec	FEC latency nsec	FEC redundancy
3B2T	1.5	7500	563	10	1023	910	113	909.33	50.67	1009.78	0.1105
PAM4	2	5625	563	10	1023	910	113	909.33	50.67	1009.78	0.1105
32-Cross	2.5	4500	563	10	1023	910	113	909.33	50.67	1009.78	0.1105
PAM8	3	3750	563	10	1023	910	113	909.33	50.67	1009.78	0.1105

- By design, for a given input burst length, the number of minimum number of protected bits is independent of the PAM constellation size.
- With m=10, maximum RS code length is 1023.
- The burst error protection capability is only 50.67 ns, probably insufficient against DFE error propagation.

10GBASE-T1 RS FEC Options m=11

RS 11 bits / symbol											
Constellation	bits / baud	Symbol rate Mbaud	min # bits protected	RS m	RS N	RS K	RS N-K	FEC frame nsec	Correction nsec	FEC latency nsec	FEC redundancy
3B2T	1.5	7500	563	11	1800	1600	200	1760.00	97.78	1955.56	0.1111
PAM4	2	5625	563	11	1800	1600	200	1760.00	97.78	1955.56	0.1111
32-Cross	2.5	4500	563	11	1800	1600	200	1760.00	97.78	1955.56	0.1111
PAM8	3	3750	563	11	1800	1600	200	1760.00	97.78	1955.56	0.1111

Constellation	bits / baud	Symbol rate Mbaud	min # bits protected	RS m	RS N	RS K	RS N-K	FEC frame nsec	Correction nsec	FEC latency nsec	FEC redundancy
3B2T	1.5	7500	563	11	2000	1800	200	1955.56	97.78	2151.11	0.1000
PAM4	2	5625	563	11	2000	1800	200	1955.56	97.78	2151.11	0.1000
32-Cross	2.5	4500	563	11	2000	1800	200	1955.56	97.78	2151.11	0.1000
PAM8	3	3750	563	11	2000	1800	200	1955.56	97.78	2151.11	0.1000

- With m=11, the burst error protection capability is close to 100 ns.
- Example RS FEC (2000, 1800, 11)
  - Each FEC frame consists of 22000 bits, with 19800 data symbol bits and 2200 parity symbol bits
  - FEC frame duration = 1.96us and intrinsic latency = 2.15us.

10GBASE-T1 RS FEC Options m=12

RS 12 bits / symbol

Constellation	bits / baud	Symbol rate Mbaud	min # bits protected	RS m	RS N	RS K	RS N-K	FEC frame nsec	Correction nsec	FEC latency nsec	FEC redundancy
3B2T	1.5	7500	563	12	1800	1600	200	1920.00	106.67	2133.33	0.1111
PAM4	2	5625	563	12	1800	1600	200	1920.00	106.67	2133.33	0.1111
32-Cross	2.5	4500	563	12	1800	1600	200	1920.00	106.67	2133.33	0.1111
PAM8	3	3750	563	12	1800	1600	200	1920.00	106.67	2133.33	0.1111

Constellation	bits / baud	Symbol rate Mbaud	min # bits protected	RS m	RS N	RS K	RS N-K	FEC frame nsec	Correction nsec	FEC latency nsec	FEC redundancy
3B2T	1.5	7500	563	12	2000	1800	200	2133.33	106.67	2346.67	0.1000
PAM4	2	5625	563	12	2000	1800	200	2133.33	106.67	2346.67	0.1000
32-Cross	2.5	4500	563	12	2000	1800	200	2133.33	106.67	2346.67	0.1000
PAM8	3	3750	563	12	2000	1800	200	2133.33	106.67	2346.67	0.1000

Constellation	bits / baud	Symbol rate Mbaud	min # bits protected	RS m	RS N	RS K	RS N-K	FEC frame nsec	Correction nsec	FEC latency nsec	FEC redundancy
3B2T	1.5	7500	563	12	2700	2400	300	2880.00	160.00	3200.00	0.1111
PAM4	2	5625	563	12	2700	2400	300	2880.00	160.00	3200.00	0.1111
32-Cross	2.5	4500	563	12	2700	2400	300	2880.00	160.00	3200.00	0.1111
PAM8	3	3750	563	12	2700	2400	300	2880.00	160.00	3200.00	0.1111

- With m=12, the burst error protection capability can be >= 160ns.
- FEC frame duration <= 2.88us and intrinsic latency <= 3.2us.

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Summary

- NBI immunity simulations and potential FEC choices are presented for PAM4, 32-CROSS, and PAM8 constellations.
- Due to time-varying nature of channel and noise environment, the receiver requires adaptive DFE or equivalent to achieve optimal performance.
- Dense constellations such as DSQ128 or PAM16 may suffer from NBI and excessive DFE error propagations.
- Sparse constellations such as PAM2 or 3B2T requires bandwidth beyond 3GHz and increased receiver implementation cost.
- Good FEC options exists for all constellations under considerations.
- Analysis from “souvignier_3ch_01_0518.pdf” shows the SNR margin sweet spot for constellation size is either 2, 2.5, or 3 bits/symbol.
- NBI immunity
  - Lower frequencies: 2 bits/symbol > 2.5 bits/symbol > 3 bits/symbol
  - Higher frequencies: 2 bits/symbol < 2.5 bits/symbol < 3 bits/symbol
- Based on the existing channel model, we recommend to focus on constellations with 2, 2.5, or 3 bits/symbol for mGig Auto PHY.
- We also recommend to focus on RS FEC with m>=11.