

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162C SC 162C.1 P 302 L 3 # I-1

Lusted, Kent Intel Corporation

Comment Type TR Comment Status X

For D2.2 comment resolution, there was contribution for an improved MDI connector mapping that was not accepted by the comment resolution group (CRG). see [https://www.ieee802.org/3/ck/public/21\\_09/ghiasi\\_3ck\\_01\\_0921.pdf](https://www.ieee802.org/3/ck/public/21_09/ghiasi_3ck_01_0921.pdf) One key feedback point on the contribution from the CRG was that the Ground pins should remain in the specification.

QSFP-DD800: For the TX2n/TX2p pair, note that GND pin #1 is closest to TX2n and GND pin #4 is closest to TX2p. Also, GND pin #4 is closest to TX4n and GND pin #7 is closest to TX4p.

For the OSFP TX2n/TX2p pair, note that GND pin #1 is closest to TX2p and GND pin #4 is closest to TX2n. Also, GND pin #4 goes with TX4p and GND pin #7 goes with TX4n.

The issue now comes from having both the OSFP and QSFP-DD800 pins in the same table.

For the QSFP-DD800 column, GND pin #1 is the physical pin next to SL1n (TX2n in the connector spec) and GND pin #4 is the physical pin next to SL1p (TX2p). However, in the OSFP column, the physical GND pin next to SL1n (TX2n) is pin #4, not pin #1 as shown above, and the physical GND pin next to SL1p (TX2p) is pin #1, not #4. Then the table becomes very messy on subsequent rows because the GND pin number can be one of two values in the OSFP case; for example, GND pin #1 is next to SL1p (TX2p) but GND pin #7 is next to SL3n (TX4n).

The GND pins are useful information, keep them in the table(s)

*SuggestedRemedy*

Replace Table 162C-3 with three tables:  
QSFP/QSFP-DD800 table  
OSFP table  
SFP/SFP-DD/DSFP table

see accompanying presentation.

Proposed Response Response Status O

Cl 80 SC 80.1.3 P 76 L 41 # I-2

Marris, Arthur Cadence Design Systems, Inc.

Comment Type E Comment Status X

Add:  
"Clause 167 for 100GBASE-VR1 and 100GBASE-SR1"

on line 42 for the case of single lane datapath as added by 802.3db

*SuggestedRemedy*

Add: "Clause 167 for 100GBASE-VR1 and 100GBASE-SR1" on line 42 showing appropriate changes from the text in 802.3db

Proposed Response Response Status O

Cl 45 SC 45.2.7.13.1 P 64 L 48 # I-3

Marris, Arthur Cadence Design Systems, Inc.

Comment Type T Comment Status X

Bit 7.49.6 needs its own subclause

*SuggestedRemedy*

Insert new subclause "45.2.7.13.A RS-FEC-Int negotiated (7.49.6)" and make it contain the this text currently in 45.2.7.13.1:

"When the Auto-Negotiation process has completed as indicated by the AN complete bit (7.1.5), bit 7.49.6 indicates that Forward Error Correction codeword-interleaved (RS-FEC-Int) operation as defined in Clause 161 has been negotiated. This bit is set only if RS-FEC-Int operation has been negotiated for a 100GBASE-P PHY supporting negotiation of RS-FEC-Int operation."

Proposed Response Response Status O

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Cl 161 SC 161.5.2.6.2 P 137 L 6 # I-4

Marris, Arthur Cadence Design Systems, Inc.

Comment Type T Comment Status X

It would help understanding to point to where tx\_scrambled is defined

SuggestedRemedy

Change:

"Let the set of vectors tx\_scrambled\_i<256:0> represent consecutive values of tx\_scrambled<256:0>."

To:

"Let the set of vectors tx\_scrambled\_i<256:0> represent consecutive values of the transcoder output tx\_scrambled<256:0> (see 161.5.2.5 for a definition of the transcoder)."

Proposed Response Response Status O

Cl 30 SC 30.5.1.1.16 P 36 L 39 # I-5

Marris, Arthur Cadence Design Systems, Inc.

Comment Type E Comment Status X

Reconcile the last paragraph of 30.5.1.1.16 with the text in the revision standard.

SuggestedRemedy

Make it so the last paragraph of 30.5.1.1.16 is identical to the revision standard so it reads:

"If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC enable bit or to the RS-FEC enable bit in the appropriate FEC control register based upon the PHY type and the FEC operating mode (see 45.2.10.3, 45.2.1.108, and 45.2.1.116).;"

Proposed Response Response Status O

Cl 161 SC 161.6.2 P 146 L 53 # I-6

Marris, Arthur Cadence Design Systems, Inc.

Comment Type E Comment Status X

Some of the cross references point to the wrong subclauses in Clause 91.

SuggestedRemedy

- On page 146 line 49 change 91.6.1 to 91.6.2
- On page 146 line 53 change 91.6.4 to 91.6.9
- On page 147 line 2 change 91.6.5 to 91.6.10
- On page 147 line 7 change 91.6.7 to 91.6.14
- On page 147 line 11 change 91.6.8 to 91.6.15
- On page 147 line 15 change 91.6.9 to 91.6.16
- On page 147 line 20 change 91.6.10 to 91.6.17
- On page 147 line 23 change 91.6.11 to 91.6.18
- On page 147 line 28 change 91.6.12 to 91.6.19
- On page 147 line 32 change 91.6.2b to 91.6.4
- On page 147 line 35 change 91.6.2c to 91.6.5
- On page 147 line 39 change 91.6.2d to 91.6.6
- On page 147 line 43 change 91.6.2e to 91.6.7
- On page 148 line 3 change 91.6.13 to 91.6.20
- On page 148 line 7 change 91.6.14 to 91.6.21
- On page 148 line 11 change 91.6.15 to 91.6.22
- On page 148 line 16 change 91.6.16 to 91.6.23
- On page 148 line 19 change 91.6.17 to 91.6.24

Proposed Response Response Status O



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Cl 161 SC 161.5.2.6.2 P 137 L 36 # I-11

Nicholl, Shawn

Xilinx

Comment Type E Comment Status X

In Figure 161-3 tx\_scrambled is inserted into an area of 2x10 bits. However, tx\_scrambled is 257 bits wide. This causes confusion. The diagram should be clarified.

SuggestedRemedy

- P802.3/D3.0 (i.e. 802.3dc) Figure 119-5 and Figure 119-7 are very similar to Figure 161-3 and are the basis for the following proposed changes to Figure 161-3:
- Remove the arrow from the diagram
  - Replace "FEC codeword A" with "from FEC codeword A"
  - Replace "FEC codeword B" with "from FEC codeword B"
  - Add shading to the final cell/column of the table (i.e. for the rows pertaining to FEC lane 0-3). The shading should be different colour from the 5-bit pad shading.
  - Add superscript text "B A" into the newly shaded area for FEC lanes 1 and 3
  - Add superscript text "A B" into the newly shaded area for FEC lanes 2
  - Replace "tx\_scrambled" with "Resumption of 257-bit blocks" or "Resumption of 257-bit tx\_scrambled blocks"
    - If "Resumption of 257-bit tx\_scrambled blocks" is chosen, then propose to make similar text change to Figure 119-5 and Figure 119-7 through maintenance of P802.3/D3.0 (i.e. 802.3dc)
      - Beside the new text, add an "=" (equal symbol) and a rectangle that is shaded the same colour as the newly shared area
      - Note that this diagram is also consistent with latest P802.3/D3.0 (i.e. 802.3dc) Figure 91-4 and ideally will remain consistent with Figure 91-4

Proposed Response Response Status O

Cl 161 SC 161.5.2.6.2 P 137 L 44 # I-12

Nicholl, Shawn

Xilinx

Comment Type E Comment Status X

In Figure 161-4 tx\_scrambled is mentioned in several places -- for an area of 35x257-bit and also in an area of 40x257-bit. However, tx\_scrambled is 257 bits wide.

SuggestedRemedy

- Propose to make the following change(s) to Figure 161-4:
- Replace (in two places) "am\_txmapped 5x257-bit blocks" with "am\_txmapped (5x257 bits)"
  - Replace (in two places) "tx\_scrambled 35x257-bit blocks" with "35x257-bit tx\_scrambled blocks"
  - Replace "tx\_scrambled 40x257-bit blocks" with "40x257-bit tx\_scrambled blocks"
  - Note that this diagram is consistent with latest P802.3/D3.0 (i.e. 802.3dc) Figure 119-6 and Figure 119-8 and ideally will remain consistent with Figure 119-6 and Figure 119-8

Proposed Response Response Status O

Cl 161 SC 161.5.2.6.2 P 137 L 50 # I-13

Nicholl, Shawn

Xilinx

Comment Type ER Comment Status X

Figure 161-4 has the wrong caption.

SuggestedRemedy

- Propose to replace the Figure 161-4 caption with:
- Figure 161-4 Alignment marker insertion period

Proposed Response Response Status O

Cl 161 SC 161.5.2.6.2 P 137 L 54 # I-14

Nicholl, Shawn

Xilinx

Comment Type E Comment Status X

In order to enhance readability and help readers to mentally connect together sections that are called by reference, the draft should include some detail about how tx\_scrambled\_am<10279:0> is consumed.

SuggestedRemedy

- Propose to add a new final paragraph at the end of 161.5.2.6.2 with the following text:
- the contents of tx\_scrambled\_am<10279:0> are an input to the Pre-FEC distribution (see 161.5.2.7 for the definition of the Pre-FEC distribution)

Proposed Response Response Status O

Cl 161 SC 161.5.4.2.1 P 142 L 46 # I-15

Nicholl, Shawn

Xilinx

Comment Type E Comment Status X

Recently, P802.3/D2.3 (i.e. 802.3dc) introduced fec\_lane\_mapping<x> to the list of variables in 91.5.4.2.1. It seems appropriate to similarly update CL161.

SuggestedRemedy

Propose to insert fec\_lane\_mapping<x> after fec\_lane.

- For fec\_lane\_mapping<x> definition propose to use: "Identical to the definition of fec\_lane in 91.5.4.2.1 except that 161.6.8 defines the FEC lane mapping."
- Note that this sub-section number may be changed by a related comment against the draft.

Proposed Response Response Status O

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Cl 161 SC 161.6 P 146 L 19 # I-16

Nicholl, Shawn

Xilinx

Comment Type ER Comment Status X

The latest P802.3/D3.0 (i.e. 802.3dc) Table 91-3 lists rows sorted by "Register/bit number" it seems appropriate for P802.3ck Table 161-2 to do the same.

*SuggestedRemedy*

Summary of proposed changes to P802.3ck CL161:

- move "1.201.3" higher in the table (i.e. after 1.201.2)
- move "1.201.4" higher in the table (i.e. after the new location of 1.201.3)
- move "1.207 to 1.209" higher in the table (i.e. after 1.206)

Proposed Response Response Status O

Cl 161 SC 161.6 P 146 L 49 # I-17

Nicholl, Shawn

Xilinx

Comment Type ER Comment Status X

In the sub-sections of 161.6, a number of cross-references to sections of CL91 of the latest P802.3/D3.0 (i.e. 802.3dc) are incorrect. There are also some ordering issues with the sub-sections of 161.6.

*SuggestedRemedy*

Summary of proposed changes to P802.3ck CL161:

- pg. 146, line 49, 161.6.1 FEC\_bypass\_indication\_enable: change "91.6.1" to "91.6.2"
- pg. 146, line 50, move the existing 161.6.10 FEC\_degraded\_SER\_enable sub-clause after 161.6.1 FEC\_bypass\_indication\_enable sub-clause to retain consistency with the order of entries in Table 161-1 ; update the FEC\_degraded\_SER\_enable section to contain the text "Identical to the definition in 91.6.4, except the reference becomes 161.5.3.3.2."
- pg. 146, line 50, move the existing 161.6.14 100G\_RS\_FEC\_Int\_enable after the new location of FEC\_degraded\_SER\_enable to retain consistency with the order of entries in Table 161-1
- pg. 146, line 50, move the existing 161.6.11 FEC\_degraded\_SER\_activate\_threshold sub-clause after the new location of 100G\_RS\_FEC\_Int\_enable sub-clause to retain consistency with the order of entries in Table 161-1; update the FEC\_degraded\_SER\_activate\_threshold section to contain the text "Identical to the definition in 91.6.5, except the reference becomes 161.5.3.3.2."
- pg. 146, line 50, move the existing 161.6.12 FEC\_degraded\_SER\_deactivate\_threshold sub-clause after the new location of FEC\_degraded\_SER\_activate\_threshold sub-clause ; update the FEC\_degraded\_SER\_deactivate\_threshold section to contain the text "Identical to the definition in 91.6.6, except the reference becomes 161.5.3.3.2."
- pg. 146, line 50, move the existing 161.6.13 FEC\_degraded\_SER\_interval sub-clause after the new location of FEC\_degraded\_SER\_deactivate\_threshold sub-clause ; update the FEC\_degraded\_SER\_interval section to contain the text "Identical to the definition in 91.6.6, except the reference becomes 161.5.3.3.2."
- pg. 146, line 53, 161.6.2 FEC\_bypass\_indication\_ability: change "91.6.4" to "91.6.9"
- pg. 147, line 3, 161.6.3 hi\_ser: change "91.6.5" to "91.6.10"
- pg. 146, line 5, move the existing 161.6.20 FEC\_degraded\_SER\_ability sub-clause after 161.6.3 hi\_ser sub-clause to retain consistency with the order of entries in Table 161-2 ; update the FEC\_degraded\_SER\_ability section to contain the text "Identical to the definition in 91.6.11, except the reference becomes 161.5.3.3.2."
- pg. 146, line 5, move the existing 161.6.21 FEC\_degraded\_SER sub-clause after the new location of FEC\_degraded\_SER\_ability sub-clause ; update the FEC\_degraded\_SER section to contain the text "Identical to the definition in 91.6.12, except the reference becomes 161.5.3.3.2."
- pg. 147, line 7, 161.6.4 amps\_lock<x>: change "91.6.7" to "91.6.14"
- pg. 147, line 11, 161.6.5 fec\_align\_status: change "91.6.8" to "91.6.15"
- pg. 147, line 15, 161.6.6 FEC\_corrected\_cw\_counter: change "91.6.9" to "91.6.16"
- pg. 147, line 18, 161.6.7 FEC\_corrected\_cw\_counter: change "91.6.10" to "91.6.17"
- pg. 147, line 23, 161.6.8 FEC\_lane\_mapping<x>: change "91.6.11" to "91.6.18"
- pg. 147, line 24, move the existing 161.6.22 FEC\_cw\_counter sub-clause after FEC\_lane\_mapping<x> sub-clause to retain consistency with the order of entries in Table 161-2

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- pg. 147, line 27, 161.6.9 FEC\_symbol\_error\_counter\_i: change "91.6.12" to "91.6.19"
- pg. 147, line 28, move the existing 161.6.23 FEC\_codeword\_error\_bin\_i sub-clause after FEC\_symbol\_error\_counter\_i sub-clause to retain consistency with the order of entries in Table 161-2
- pg. 148, line 3, 161.6.15 align\_status: change "91.6.13" to "91.6.20"
- pg. 148, line 7, 161.6.16 BIP\_error\_counter\_i: change "91.6.14" to "91.6.21"
- pg. 148, line 11, 161.6.17 lane\_mapping<x>: change "91.6.15" to "91.6.22"
- pg. 148, line 15, 161.6.18 block\_lock<x>: change "91.6.16" to "91.6.23"
- pg. 148, line 19, 161.6.19 am\_lock<x>: change "91.6.17" to "91.6.24"

Proposed Response      Response Status

Cl 0      SC 0      P 0      L 0      # I-18

Brown, Matthew      Huawei Technologies Canada

Comment Type E      Comment Status X

Keep this draft in line with the new revision (802.3dc) and any amendments that precede 802.3ck.

SuggestedRemedy

Align the next draft with the latest versions of the new revision (802.3df) and any preceding amendments.

Proposed Response      Response Status

Cl 80      SC 80.1.5      P 80      L 14      # I-19

Brown, Matthew      Huawei Technologies Canada

Comment Type T      Comment Status X

100GAUI-1 C2C and C2M are listed in Table 80-5 as optional for 100GBASE-VR1 and 100GBASE-SR1, but the sublayer table in Clause 167 does not list these.

SuggestedRemedy

Import Clause 167 and Table 167-1, adding 100GBASE-1 C2C and C2M.

Proposed Response      Response Status

Cl 162      SC 162.9.4.1      P 174      L 4      # I-20

Brown, Matthew      Huawei Technologies Canada

Comment Type T      Comment Status X

This paragraph provides the nominal value for the UI. This is not provided in 162 for KR, in 120F for C2C, or in 120G for C2M. It is not necessary to specify this number since it is easily determined by the nominal signaling rate. To be consistent with other similar PMD/AUI clauses this sentence should be removed.

SuggestedRemedy

Remove the following sentence: "This translates to a nominal unit interval of approximately 18.8235 ps."

Proposed Response      Response Status

Cl 163      SC 163.9.2.7      P 207      L 10      # I-21

Brown, Matthew      Huawei Technologies Canada

Comment Type T      Comment Status X

This table incorrectly points to Table 163-11 for the SCMR value.

SuggestedRemedy

Change "Table 163-11" to "Table 163-5".

Proposed Response      Response Status

Cl 162      SC 162.11.2      P 182      L 6      # I-22

Brown, Matthew      Huawei Technologies Canada

Comment Type T      Comment Status X

The specified for ILDD says the value "should be greater than or equal" to Equation 162-17, but Equation 162-17 is an inequality. Change the wording to the form used in 120G.4.1.

SuggestedRemedy

Change: "The measured differential-mode to differential-mode insertion loss of a cable assembly shall be greater than or equal to the minimum cable assembly differential-mode to differential-mode insertion loss given in Equation (162-17) and illustrated in Figure 162-7."

To: "The channel differential-mode to differential-mode insertion loss shall meet Equation (162-17), which is illustrated in Figure 162-7."

In Equation 162-17 change ILddmin to ILdd.

Change the description of ILddmin (now ILdd) to "is the cable assembly differential-mode to differential-mode insertion loss in dB".

Proposed Response      Response Status

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CI 163 SC 163.10.2 P 214 L 16 # I-23  
 Brown, Matthew Huawei Technologies Canada  
 Comment Type T Comment Status X  
 The sentence specifying insertion loss refers to a maximum value, but the equation is an inequality. Reword the specify to be of the for used in 120G.4.1.  
 SuggestedRemedy  
 Change: "The maximum recommended differential-mode to differential-mode insertion loss of the channel is given by Equation (163-6)."  
 To: "The channel differential-mode to differential-mode insertion loss should meet Equation (163-6)."  
 Proposed Response Response Status O

CI 120F SC 120F.4.2 P 248 L 20 # I-24  
 Brown, Matthew Huawei Technologies Canada  
 Comment Type T Comment Status X  
 The sentence specifying insertion loss refers to a maximum value, but the equation is an inequality. Reword the specify to be of the for used in 120G.4.1.  
 SuggestedRemedy  
 Change: "The channel differential-mode to differential-mode insertion loss should be equal to or less than Equation (120F-2)."  
 To: "The channel differential-mode to differential-mode insertion loss should meet Equation (120F-2)."  
 Proposed Response Response Status O

CI 120F SC 120F.4.2 P 248 L 26 # I-25  
 Brown, Matthew Huawei Technologies Canada  
 Comment Type E Comment Status X  
 To be consistent with other similar specifications in this draft the units should be in the variable definition not the equation.  
 SuggestedRemedy  
 In Equation 120F-2, delete "(dB)"  
 Change the definition of ILdd to "is the channel differential-mode to differential-mode insertion loss in dB"  
 Proposed Response Response Status O

CI 120G SC 120G.3.1.5 P 260 L 19 # I-26  
 Brown, Matthew Huawei Technologies Canada  
 Comment Type T Comment Status X  
 Figure 120G-6 includes a VNA at the input to the measurement receiver, yet there are nor measurements defined that require a VNA.  
 SuggestedRemedy  
 Change "VNA or scope" to "Scope".  
 Proposed Response Response Status O

CI 120G SC 120G.3.3.5.1 P 266 L 6 # I-27  
 Brown, Matthew Huawei Technologies Canada  
 Comment Type T Comment Status X  
 The BUJ generation method is based on that specified in 120E.3.4.1.1. Since the BUJ pattern signaling rate doubles compared to that in 120E.3.4.1.1, the corner frequency frequency limits for the BUJ jitter filter should be scaled the same to give the same jitter distribution.  
 SuggestedRemedy  
 Change: "The low-pass filter has 20 dB/decade rolloff with a -3 dB corner frequency between 150 MHz and 300 MHz."  
 To: "The low-pass filter has 20 dB/decade rolloff with a -3 dB corner frequency between 600 MHz and 1.2 GHz."  
 Proposed Response Response Status O

CI 120G SC 120G.3.3.5.1 P 266 L 40 # I-28  
 Brown, Matthew Huawei Technologies Canada  
 Comment Type T Comment Status X  
 Figure 120G-9 includes a VNA (vector network analyzer) at the output of the pattern generator, yet there are measurements defined that require a VNA.  
 SuggestedRemedy  
 Delete the VNA box and the switch that connects to it.  
 Proposed Response Response Status O

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Cl 120G SC 120G.3.4 P 269 L 12 # I-29

Brown, Matthew Huawei Technologies Canada

Comment Type E Comment Status X

Table 120G-9 is titled "Module input characteristics" thus it is obvious that all specifications in this table relate to the module input. To match the other specifications in this table the word "input" should be removed from the parameter "Differential pk-pk input voltage tolerance (min)"

SuggestedRemedy

Change " "Differential pk-pk voltage tolerance (min)"  
To "Differential pk-pk voltage tolerance (min)"

Proposed Response Response Status O

Cl 120G SC 120G.3.4.3.1 P 270 L 44 # I-30

Brown, Matthew Huawei Technologies Canada

Comment Type T Comment Status X

Figure 120G-10 includes a VNA at the output of the frequency-dependent attenuator, but there are no measurements defined that require the use of a VNA.

SuggestedRemedy

Delete the VNA box and the associated switch.

Proposed Response Response Status O

Cl 120G SC 120G.3.4.3.2 P 271 L 25 # I-31

Brown, Matthew Huawei Technologies Canada

Comment Type T Comment Status X

The span over which the scattering parameters is ambiguous, but is intended to be from the pattern generator output to TP1a. Also, the description of ILdd for Equation 120G-3 and the title of Figure 120G-11 are incorrect.

SuggestedRemedy

On page 271 line 25, change "the scattering parameters approximate" to "the scattering parameters from the pattern generator output to TP1a approximate".  
For equation 120G-3 change the definition of ILdd(f) to "is the target high-loss differential-mode to differential-mode insertion loss in dB"  
Change the title of Figure 120G-11 to "Module stressed input target high-loss differential-mode to differential-mode insertion loss"

Proposed Response Response Status O

Cl 120G SC 120G.3.4.3.2 P 271 L 28 # I-32

Brown, Matthew Huawei Technologies Canada

Comment Type T Comment Status X

The explanation for the 18.2 dB is not complete. 16 dB is to account for a worst case host PCB channel. The remaining 2.2 dB accounts for only a portion of the expected package insertion loss. The intent is that the remaining 2.2 dB plus the expected effective insertion loss of the pattern generator would account for the expected package loss.

SuggestedRemedy

Change: "The resulting insertion loss from the output of the pattern generator to TP1a is 18.2 dB at 26.56 GHz, representing 16 dB channel loss with an additional allowance for host transmitter package loss."  
To: "The resulting insertion loss from the output of the pattern generator to TP1a is 18.2 dB at 26.56 GHz, representing 16 dB channel loss with an additional 2.2 dB which in addition to the effective insertion loss of the pattern generator output accounts for host transmitter package loss."

Proposed Response Response Status O

Cl 161 SC 161.5.4.2.2 P 143 L 6 # I-33

Rannow, R K IEEE member / Self Employed

Comment Type T Comment Status X

Multiple instances of the term "both", and both = and. This appears verbose and perhaps ambiguous.

Confusing statement:

If current\_pcs1 and first\_pcs1 both found a match and indicate the same PCS lane number, amp\_match is set to true. Otherwise, amp\_match is set to false.

SuggestedRemedy

Review and remove the term "both".

Suggested modification:

If current\_pcs1 and first\_pcs1 match and indicate the same PCS lane number, amp\_match is set to true. Otherwise, amp\_match is set to false.

Proposed Response Response Status O

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Cl 163 SC 163.9.2.7 P 207 L 11 # I-34  
 Wu, Mau-Lin MediaTek Inc.  
 Comment Type **TR** Comment Status **X**  
 The specification for SCMR (min) is defined in Table 163-5, instead of Table 163-11.  
*SuggestedRemedy*  
 Change Table 163-11 to Table 163-5. Correct the hyperlink as well.  
 Proposed Response Response Status

Cl 1 SC 1.3 P 32 L 12 # I-37  
 Ran, Adeo Cisco Systems, Inc.  
 Comment Type **E** Comment Status **X**  
 The references for QSFP-DD and for SFP-DD don't have periods at the end, unlike other references.  
*SuggestedRemedy*  
 Add final periods for these two references.  
 Proposed Response Response Status

Cl 154 SC 154.1 P 133 L 0 # I-35  
 Ran, Adeo Cisco Systems, Inc.  
 Comment Type **T** Comment Status **X**  
 Clause 154 (recently added to 802.3dc) defines the 100GBASE-ZR PHY, which may use the 100GAUI-1 C2C/C2M interfaces, in addition to the 100GAUI-2 and other interfaces currently listed.  
*SuggestedRemedy*  
 Add Clause 154 and 154.1 to the draft.  
 Amend Table 154-1 to include 100GAUI-1 C2C and 100GAUI-1 C2M, both optional.  
 Proposed Response Response Status

Cl 1 SC 1.4 P 32 L 51 # I-38  
 Ran, Adeo Cisco Systems, Inc.  
 Comment Type **E** Comment Status **X**  
 For consistency, URLs should be formatted in blue and underlined.  
*SuggestedRemedy*  
 Apply URL format in four URL instances on this page.  
 Proposed Response Response Status

Cl 167 SC 167.1 P 225 L 0 # I-36  
 Ran, Adeo Cisco Systems, Inc.  
 Comment Type **T** Comment Status **X**  
 Clause 167 (part of 802.3db) defines six new PHY with optical PMDs that use 53.125 Gbd signaling. These PHYs may use the 100GAUI-1, 200GAUI-2, and 400GAUI-4 C2C/C2M interfaces, in addition to the interfaces currently listed.  
 Since 802.3db is scheduled to be published before 802.3ck, this should be an amendment of clause 167.  
*SuggestedRemedy*  
 Add Clause 167 and 167.1 to the draft.  
 Amend Table 167-1 to include 100GAUI-1 C2C and 100GAUI-1 C2M, both optional.  
 Amend Table 167-2 to include 200GAUI-2 and 400GAUI-4, each with C2C and C2M, all optional.  
 Proposed Response Response Status

Cl 30 SC 30.5.1.1.16 P 36 L 39 # I-39  
 Ran, Adeo Cisco Systems, Inc.  
 Comment Type **E** Comment Status **X**  
 The fourth paragraph of 30.5.1.1.16 has been changed by 802.3dc to the following text:  
 If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC enable bit or to the RS-FEC enable bit in the appropriate FEC control register based upon the PHY type and the FEC operating mode (see 45.2.10.3, 45.2.1.108, and 45.2.1.116).;  
 This removes the need for the changes in this paragraph in the 802.3ck draft.  
*SuggestedRemedy*  
 Remove the fourth paragraph of 30.5.1.1.16.  
 Change the editorial instruction from "Change remainder of 30.5.1.1.16 as follows" to "change the three subsequent paragraphs as follows".  
 Proposed Response Response Status

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 91 SC 91 P 89 L 5 # I-40

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

The amendment of clause 91 has subclauses under 91.5 and 91.5.2 without the full hierarchy. It is common to include the full hierarchy of each amended subclause.

SuggestedRemedy

Add headings for:  
91.5 Functions within the RS-FEC sublayer  
91.5.2 Transmit function

Proposed Response Response Status O

Cl 91 SC 91.5.3.3 P 89 L 31 # I-41

Ran, Adeo Cisco Systems, Inc.

Comment Type ER Comment Status X

The amended text in this paragraph refers to "This option", without stating what option it is... (it is the option to bypass error correction)

It would be easier for readers to understand the requirement if the option is stated explicitly.

SuggestedRemedy

Include the entire third paragraph from the base document. In 802.3dc the text is:

The Reed-Solomon decoder may provide the option to perform error detection without error correction to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC\_bypass\_correction\_ability variable (see 91.6.8). When the option is provided, it is enabled by the assertion of the FEC\_bypass\_correction\_enable variable (see 91.6.1). This option... <remainder of the text as in D3.0>

Proposed Response Response Status O

Cl 120 SC 120.5.11.2.a P 110 L 46 # I-42

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

Equation (120-1) and Figure 120-6a are placed after a large block of text and a full pattern, and seem to be out of context. The block could be broken to two paragraphs so the equation and figure are placed after their reference, and are in the right context.

SuggestedRemedy

Break the paragraph into two after "Equation(120-1)", and have the equation, note, and figure follow the first paragraph.

Proposed Response Response Status O

Cl 161 SC 161.5.2.6.1 P 136 L 5 # I-43

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

The variable x is inconsistency italicized in the text of list items a-c.

SuggestedRemedy

Make x italic wherever it denotes a lane number.

Proposed Response Response Status O

Cl 161 SC 161.5.2.6.2 P 137 L 3 # I-44

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

"x" should not be used as a multiplication symbol.

Also applies in 161.5.3.5.

SuggestedRemedy

Change to a multiplication symbol as in the last paragraph of 161.5.2.6.1, in both places.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 161 SC 161.6.10 P 147 L 30 # I-45

Ran, Adee Cisco Systems, Inc.

Comment Type ER Comment Status X

The reference for FEC\_degraded\_SER\_enable is to 91.6.2b. This was the subclause added in 802.3cd. After integration into 802.3dc, this became 91.6.4.

Similarly in 161.6.11 through 161.6.13, 161.6.20, and 161.6.21.

*SuggestedRemedy*

- In 161.6.10 change the reference to 91.6.4.
- In 161.6.11 change the reference to 91.6.5.
- In 161.6.12 change the reference to 91.6.6.
- In 161.6.13 change the reference to 91.6.7.
- In 161.6.20 change the reference to 91.6.11.
- In 161.6.21 change the reference to 91.6.12.

Proposed Response Response Status

Cl 161 SC 161.7.3 P 150 L 13 # I-46

Ran, Adee Cisco Systems, Inc.

Comment Type E Comment Status X

The "FEC degraded SER detection" option for this clause is defined in 161.5.3.3.2.

*SuggestedRemedy*

- Change the reference of item \*FDD from 91.5.3.3.1 to 161.5.3.3.2.
- Similarly change item RF12 in 161.7.4.2.

Proposed Response Response Status

Cl 162 SC 162.8.2 P 162 L 34 # I-47

Ran, Adee Cisco Systems, Inc.

Comment Type T Comment Status X

The transmit function operating modes listed are DATA and TRAINING, but with the change of the PMD control state diagram we also need a QUIET mode, as in clause 136 (in 802.3dc).

*SuggestedRemedy*

In the first paragraph change "The PMD transmit function has two operating modes, DATA and TRAINING" to "The PMD transmit function has three operating modes: DATA, TRAINING, and QUIET".

Add the following paragraph at the end of 162.8.2:

"When operating in QUIET mode the PMD transmit function shall turn off the transmitter such that the transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max) with Tx disabled in Table 162-10."

Proposed Response Response Status

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162 SC 162.8.11 P 164 L 27 # I-48

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

When we defined the addition of QUIET state to the PMD control function in 136.8.11, it had the text "This variable is always set to FALSE for 50 Gb/s per lane PHYs, otherwise it is set to TRUE". Now that this change has been implemented in 802.3dc D3.0 and clause 136 removed from 802.3ck, we lost the requirement to set it to TRUE for the PHYs in clauses 162 and 163.

The suggested remedy is to add this requirement as another exception in 162.8.11.

An alternative solution is to amend the updated 136.8.11.7.1 (as of 802.3dc D3.0), specifically the definition of use\_quiet\_in\_training, to be optional only in 50 Gb/s. This could be done as follows:

"Boolean variable that is TRUE if the PMD control function (see Figure 136-7) can enter the QUIET state. The value of this variable is implementation dependent for 50 Gb/s per lane PHYs, and TRUE for all other PHYs"

And amend the PICS of clause 136 accordingly.

*SuggestedRemedy*

Add exception to the list in 162.8.11:

h) The value of use\_quiet\_in\_training (see 136.8.11.7.1) is TRUE.

Add a corresponding PICS item in 163.13.4.2.

Proposed Response Response Status O

Cl 162 SC 162.9.3 P 166 L 9 # I-49

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The 50 Ohm termination on each conductor is specified only for DC common mode measurement. I cannot find a requirement that differential signal measurement is also done with similar terminations.

It is important to specify the termination of each conductor separately, to avoid reflections from the test equipment, and to ensure the expected common mode termination (the scope cannot be isolated from signal ground).

*SuggestedRemedy*

Change "using a test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth" to "using a test system with 50 Ohm termination on each conductor of the differential pair, and a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth".

Proposed Response Response Status O

Cl 162 SC 162.9.3 P 166 L 34 # I-50

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

"peak" in Rpeak should be a subscript.

*SuggestedRemedy*

Format per comment.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162 SC 162.9.3.1.2 P 169 L 8 # I-51

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

"The linear fit pulse peak ratio shall be greater than 0.397" - but there is no definition of that parameter.

163.9.2.5 has a related parameter "Difference linear fit pulse peak ratio" calculated using a procedure in 163A.3.2.1, where Equation (163A-9) defines  $R_{peak}(meas)$ . A similar calculation should be used here, but for this clause there is only a measured parameter without a reference parameter, so it can't point to 163A.

SuggestedRemedy

Insert a paragraph after the first paragraph of 162.9.3.1.2:

"The linear fit pulse peak ratio  $R_{peak}$  is defined as the ratio between the maximum value of  $p(k)$  and the steady-state voltage  $v_f$ ."

{where  $_$  indicates subscript}

Proposed Response Response Status O

Cl 162 SC 162.9.3.1.5 P 170 L 23 # I-52

Ran, Adeo Cisco Systems, Inc.

Comment Type T Comment Status X

'A coefficient may be set to zero by asserting a coefficient request of "no equalization" for that coefficient' - but  $c(0)$  will be set to 1 this way.

The requirements to set to zero are only for  $c(-3)$ ,  $c(-2)$ ,  $c(-1)$  and  $c(1)$ .

SuggestedRemedy

Change the quoted sentence to:

'Any of the coefficients  $c(-3)$ ,  $c(-2)$ ,  $c(-1)$ , or  $c(1)$  may be set to zero by asserting a coefficient request of "no equalization" for that coefficient'.

Proposed Response Response Status O

Cl 162 SC 162.9.3.3 P 170 L 31 # I-53

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The definition of SNDR refers back to 120D which does not state what the Tx equalization should be in this measurement. Based on a previous specification in clause 92, it may be understood that the limit in Table 162-10 applies to any valid equalization setting.

Since transmitters typically have noise sources that are independent of equalization, and applying equalization reduces the pulse peak, it is expected that increasing the "strength" of Tx equalization would degrade the measured SNDR. We can assume equalization settings with  $c(0)$  close to 0.5, which would reduce the measured pulse peak by 5-6 dB; this makes the SNDR spec more difficult than it seems.

A related concern is that the noise injected in the receiver ITT is also after Tx equalization (like realistic transmitters), and it is calibrated by measuring SNDR and using the results as  $TX\_SNR$ . However,  $TX\_SNR$  in COM represents a white noise source  $before$  the Tx equalization, since it should have the same spectrum as the victim signal.

There seems to be a mismatch between the effect of  $TX\_SNR$  in COM and the effect of SNDR in real links.

This may also affect SNDR and/or  $SNR\_TX$  in clause 163 and annex 120F, although the receiver test signal is calibrated differently.

SuggestedRemedy

The definition of SNDR and/or the calculation of the effect of  $SNR\_Tx$  in COM may need to be changed.

A detailed presentation is planned.

Proposed Response Response Status O

Cl 162 SC 162.9.4.3.3 P 175 L 39 # I-54

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

Item e in the list is very difficult to understand, and the referenced equations have some parameters defined in Annex 93A which may be unclear. Also, the value of  $f_{hp}$  in equation 162-11 is not provided anywhere.

The phrasing should be improved to enable implementing this procedure.

SuggestedRemedy

A presentation proposing a rewrite is planned.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162 SC 162.11 P 181 L 11 # I-55

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The text says "For 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4, the lanes are AC-coupled. The AC-coupling shall be within the cable assembly". It can be questioned which contacts are AC-coupled in the cable. Figure 162-2 shows signal shields and link shield in addition to the differential pairs, and there is no distinction, so can the shields also be AC-coupled? Are they even required to be connected on both ends?

My understanding is that in practice the shields are DC-coupled and provide a ground connection between both ends. This has importance in preventing the ground voltage from bouncing at either end and creating unexpected common-mode differences between Tx and Rx pairs (because common-mode voltage is referenced to ground).

This should be stated explicitly. The suggested remedy is to add it to 162.11 which seems to be a convenient place, but other places or phrasing are possible. It may be required to add some specifications to the MDI as well.

SuggestedRemedy

Insert a paragraph after the one starting with the quoted text (lines 11-16) with the following text:

"The signal shield and link shield are connected to the corresponding contacts in the MDI plug connectors on both ends of the cable assembly".

Proposed Response Response Status O

Cl 162 SC 162.11.2 P 182 L 12 # I-56

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The text specifying the minimum insertion loss and equation 162-17 are inconsistent: The text says the ILDD shall be lower than the limit defined by the equation, but the equation has "ILDD\_min(f) >="; this reads as if the limit is anywhere below the line defined by the equation, so the limit is not defined.

The suggested remedy is a minimal change. Alternatively, the definition can be changed to state that ILDD "shall meet the equation" and have the equation in terms of ILDD instead of ILDDmin, as done in other similar cases.

SuggestedRemedy

In equation 162-17, change ">=" to "=".

Proposed Response Response Status O

Cl 162 SC 162.11.5 P 184 L 33 # I-57

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

Equation 162-19 lets the difference between ILcd and ILdd be 10 dB up to half of (an old Nyquist frequency) and then linearly lower at higher frequencies. This does not make sense physically, and open the door to poor cables. The Tx output common mode noise problem is exacerbated by strong conversion from common mode to differential signal.

Note that COM does not cover the conversion loss term, so we should strive to make it negligible, rather than allowing it to be large.

At low frequencies we expect low ILdd and high ILcd, and the difference is much larger than 10 dB. Even at high frequencies up to 40 GHz, channels submitted to 802.3ck do not exceed 10 dB. We should not allow less than 10 dB difference across the upper half of the spectrum.

Based on samples of submitted channels and some measured channels it is suggested to tighten this specification to be 24 dB at the lowest frequency, linear slope to 10 dB at Nyquist/2, and constant 10 dB at maximum frequency.

This also holds for the specification in clause 163 (channel construction may be different but the arguments above still hold and the effect on the link budget is the same).

A presentation of some contributed data compared to the proposed limit is planned. Any contradictory data would be welcome.

SuggestedRemedy

Change equation 162-19 limit to be  
 $24 - 13.56/f * 14 \mid 0.05 \leq f \leq 13.56$   
 $10 \mid 13.56 \leq f \leq 40$

Change Figure 162-9 accordingly.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162 SC 162.11.7.1 P 187 L 43 # I-58

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

"The scattering parameters for a PCB transmission line are calculated using the method defined in 93A.1.2.3 using Equation (93A-13), Equation (93A-14) and the parameter values given in Table 162-20"

93A.1.2.3 (in the base document) includes equations 93A-13 and 93A-14, so there is no need to include these references in addition, with repetitive "using".

(If they are to be retained, a serial comma should be inserted after Equation (93A-14))

SuggestedRemedy

Change the quoted sentence to "The scattering parameters for a PCB transmission line are calculated using the method defined in 93A.1.2.3 with the parameter values given in Table 162-20".

Proposed Response Response Status O

Cl 162 SC 162.11.7.2 P 189 L 35 # I-59

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

The sentence "Annex 162C specifies the MDIs for 100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4." seems unnecessary and out of place here (subclause title is "Signal and crosstalk paths used in calculation of COM").

The same sentence appears in the next subclause 162.12, MDI specifications, where it makes more sense, so it may be an unintended leftover.

SuggestedRemedy

Consider deleting this sentence.

Proposed Response Response Status O

Cl 162 SC 162.14.3 P 192 L 32 # I-60

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

In item FEC100, "RS(544,514)" is larger than surrounding text. Other items that include large text (different text) are CA2, CA5, CA6.

SuggestedRemedy

Make text size match the surrounding text.

Proposed Response Response Status O

Cl 163 SC 163.8.1 P 202 L 5 # I-61

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The link block diagram does not show a ground connection, and there is no requirement anywhere in clause 163 that the PMDs on both ends of the link have a common ground connection.

If there is no common ground, or ground connection is poor, the Tx common-mode specifications may become meaningless, because the common-mode voltage on each device is defined with different grounds.

SuggestedRemedy

Add a ground connection between the PMDs to the diagram.

Add a sentence below the diagram stating that the specifications in this clause only apply to systems with shared ground between the two PMDs.

Proposed Response Response Status O

Cl 163 SC 163.9.2.7 P 207 L 7 # I-62

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

In "p(k)", p and k should be italicized, as in line 18 and in 162.9.3.1.1.

SuggestedRemedy

Apply formatting per comment.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 163 SC 163.9.2.7 P 207 L 10 # I-63

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The peak-to-peak common-mode noise measured can be significantly increased by mismatched cabling in the test setup or routing in the test fixture. A difference of 1 mm between single-ended path translates to ~25% of a UI. This would cause significant conversion of the differential signal to CM signal and degradation the SCMR. This common-mode signal would be correlated to the data pattern, but so far we have not separated the CM specification to correlated and uncorrelated components.

Also, there are no conversion loss specifications for test fixture (even if we had, they would be difficult to measure). Poorly designed test fixtures may cause a good device to fail the test even in a well-calibrated test setup. This may make SCMR seem difficult to meet.

It may be possible to calibrate the measurement for differences between cables, mitigating some of the problem. But we may not want to provide an open ticket to full deskew of the single-ended signals, because it can "correct" problems in the DUT as well as in the test system.

As a minimum remedy to this problem, it is suggested to add a note informing the reader that good matching of the test fixture and calibration of the test setup is recommended.

Alternatively, the CM measurement could be separated to correlated and uncorrelated, and SCMR calculated only for the uncorrelated component. This would be preferable if there is consensus for this path.

*SuggestedRemedy*

Add an informative NOTE at the end of this subclause:

NOTE—SCMR measurement may be sensitive to mismatches between the single-ended paths in the test fixture and the test setup. Careful design and calibration of the test system is recommended.

Proposed Response Response Status O

Cl 163 SC 163.9.2.7 P 207 L 11 # I-64

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

Incorrect cross-reference to Table 163-11 - SCMR (min) is specified in Table 163-5.

Also, this subclause is also referred to by Table 120F-1 and maybe others in the future. To separate definition from required limit, the "shall" statement should be placed at the end of the subclause, as done in 163.9.2.6.

*SuggestedRemedy*

In the sentence "The signal to AC common-mode noise ratio shall meet the specification for SCMR (min) in Table 163-11", change Table 163-11 to Table 163-5.

Move this sentence to the end of the subclause, after equation 163-2 and its variable list.

Proposed Response Response Status O

Cl 163 SC 163.10.6 P 217 L 41 # I-65

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The specification of ILdc-ILdd in equation 163-9 and Figure 163-9 is identical to the specification of ILcd - ILdd in equation 163-8 and Figure 163-8, and also identical to the one in equation 162-19 and Figure 162-9.

It makes sense physically and from link budget purposes to have identical specifications for these parameters. It makes less sense to have duplicated equations and figures. It just confuses the reader.

*SuggestedRemedy*

Replace equations 163-8 and 163-9 with references to equation 162-19.

Replace figure 163-8 and figure 163-9 with references to figure 162-9.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 120F SC 120F.1 P 238 L 2 # I-66

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The link block diagram does not show a ground connection, and there is no requirement anywhere in annex 120F that the devices on both ends of the link have a common ground connection.

If there is no common ground, or ground connection is poor, the Tx common-mode specifications may become meaningless, because the common-mode voltage on each device is defined with different grounds.

If a ground connection is added in this figure, it should also be noted that each arrow represents a differential pair, or alternatively draw two lines in each direction, as done in Figure 163-2.

*SuggestedRemedy*

Add an additional line in each direction to represent a differential pair, and add a ground connection between the devices to the diagram.

Change the paragraph on P237 L40-42, inserting a sentence about the ground connection, as follows:

"The 100GAUI-1, 200GAUI-2, or 400GAUI-4 C2C bidirectional link is described in terms of a C2C transmitter, a C2C channel, and a C2C receiver, which have a shared ground connection. Figure 120F-2 depicts a typical C2C application."

Proposed Response Response Status

Cl 120G SC 120G.1 P 256 L 16 # I-67

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The link block diagram does not show a ground connection, and there is no requirement anywhere in annex 120G that the devices on both ends of the link have a common ground connection.

If there is no common ground, or ground connection is poor, the output common-mode specifications and input common-mod tolerance may become meaningless, because the common-mode voltage on each device is defined with different grounds.

If a ground connection is added in this figure, it should also be noted that each arrow represents a differential pair, or alternatively draw two lines in each direction, as done in Figure 163-2.

*SuggestedRemedy*

Add an additional line in each direction to represent a differential pair, and add a ground connection between the devices to the diagram.

Change the first sentence in the paragraph on P256 L7-14, inserting a sentence about the ground connection, as follows:

"The C2M link is described in terms of a host C2M component, a C2M channel with associated differential-mode to differential-mode insertion loss (ILdd), and a module C2M component, which have a shared ground connection."

Proposed Response Response Status

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

CI 120G SC 120G.3.2.2 P 262 L 3 # I-68

Ran, Adee Cisco Systems, Inc.

Comment Type TR Comment Status X

The test configuration shown in Figure 120G-7 is unclear about the source of the pattern used to drive the module output during the test.

In practice, three possibilities are likely to be considered by a test engineer:

1. The module can be fed an externally-generated compliant signal to its optical receiver. This would represent a real-life use case; but it makes a complicated test setup, and the pattern may contain occasional errors from the optical receiver, which will interfere with sampling scope operation (unless the BER on the optical segment is low enough).
2. The module can be fed a minimally compliant signal to its electrical input (e.g. the stressed input tolerance signal, 120G.3.4.3) its optical output looped back through an optical patch cord. This would approximate a real-life use case, without requiring optical test signal calibration. But this method is ruled out by the requirement to have asynchronous co- and counter-propagating signals.
3. The module can generate the test pattern internally, and be feed asynchronous electrical counter-propagating signals to its input. But this would not represent a real-life use case, since the pattern uses an internal clock likely with very low jitter compared to the clock recovered from an optical signal.

Option 3 is not prohibited anywhere in the text; if it is allowed, modules may pass their tests but have degraded output in the field, due to excessive jitter from using a recovered clock. The host input tolerance requirements are equal to the module output requirement, and do not account for such degradation, so a system with compliant components may fail.

The suggested remedy is to clarify that the requirements hold for any compliant optical signal input to the module, and note that using internally generated test pattern does not create a representative signal; the test engineer will have to sort it out.

Alternatively, we could remove the requirement for asynchronous counter- and co-propagating signals, to enable testing with optical loopback, which would be easier to conduct. If that is done, it should be required to use optical loopback (through the PMD) rather than internal electrical loopback (which would still not be representative, since it would involve only one clock regeneration); and in addition, the electrical signal should be a stressed input signal.

*SuggestedRemedy*

In 120G.3.2, change "The module output shall meet the specifications given in Table 120G-3" to "The module output shall meet the specifications given in Table 120G-3 for any compliant optical input signal".

In 120G.3.2.2, add a NOTE after Figure 120G-7:

NOTE—Driving the module output using an internally generated pattern might not create output signals representative of full-link operation, and may result in false pass results. It is recommended to use feed the module with an optical signal modulated by the test pattern.

Proposed Response Response Status O

CI 120G SC 120G.3.4.3.2 P 271 L 4 # I-69

Ran, Adee Cisco Systems, Inc.

Comment Type T Comment Status X

In module stressed input calibration, the transition time should be defined with no Tx equalization in the pattern generator, as in the host stressed input calibration, 120G.3.3.5.2.

*SuggestedRemedy*

Change from  
 "The pattern generator is set to generate a PRBS13Q pattern (see 120.5.11.2.1) with transition time (see 120G.3.1.4) at the output of the pattern generator as specified in Table 120G-10"  
 To  
 "The pattern generator is set to generate a PRBS13Q pattern (see 120.5.11.2.1). The transition time (see 120G.3.1.4) measured at the output of the pattern generator when configured to "no equalization" is as specified in Table 120G-10".

Proposed Response Response Status O

CI 120G SC 120G.3.4.3.2 P 271 L 24 # I-70

Ran, Adee Cisco Systems, Inc.

Comment Type TR Comment Status X

"For the high-loss signal calibration, the frequency-dependent attenuator is configured such that the scattering parameters approximate those for a PCB transmission line calculated from Equation (93A-13) and Equation (93A-14) using  $z_p = 464$  mm in length and the relevant parameter values given in Table 162-20"

The intent is that the scattering parameters \_from the pattern generator output to TP1a\_ approximate the PCB transmission line (not just the FDA), otherwise the test channel would have excessive loss. This is not clear from the current text.

*SuggestedRemedy*

Insert "from the pattern generator output to TP1a" after "the scattering parameters".

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 120G SC 120G.3.4.3.2 P 271 L 31 # I-71

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The text in list item g has been changed from D2.2 to D2.3 in a way that makes it possibly confusing to readers, as shown in comment #31 against D2.3.

The intent is to limit the space of reference receiver configurations to those with  $gDC + gDC2 \leq 10.5$  dB. The other configurations are not expected to be checked or optimized for VEC by setting the PG equalization, and the VEC that can be achieved with other configurations is irrelevant; analytically, a signal created by PG equalization optimized for a high gDC setting will be over-equalized with a lower gDC setting.

The text should be rephrased to clarify this. The suggested remedy is based on the wording in D2.2 .

SuggestedRemedy

Change from  
 "Eye height and VEC are measured at TP1a as described in 120G.5.2 with the exception for the high-loss case that the reference receiver CTLE setting that minimizes VEC has  $gDC + gDC2$  less than or equal to  $-10.5$  dB"  
 to  
 "Eye height and VEC are measured at TP1a as described in 120G.5.2. For the high-loss case, an exception is made that the reference receiver CTLE is limited to settings where  $gDC + gDC2$  is less than or equal to  $-10.5$  dB".

Proposed Response Response Status O

Cl 163A SC 163A.3.1.1 P 317 L 49 # I-72

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

In expressions that include italics, parentheses and numbers should be set in upright font. This line includes some instances, and there are many others.

SuggestedRemedy

Format per comment, apply throughout the document.

Proposed Response Response Status O

Cl 163A SC 163A.3.2.1 P 320 L 9 # I-73

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

Equation 163A-7 is truncated from the top.

SuggestedRemedy

Fix it.

Proposed Response Response Status O

Cl 163A SC 163A.3.2.1 P 320 L 24 # I-74

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

Equation 163A-6 and Equation 163A-10 use the reference voltage terms  $v_f(\text{ref})$  and  $v_{\text{peak}}(\text{ref})$ . These are not defined here but in 163A.3.1.1. A cross-reference would help.

SuggestedRemedy

Add a paragraph at the end of this subclause: " $v_f(\text{ref})$  and  $v_{\text{peak}}(\text{ref})$  are defined in 163A.3.1.1."

Proposed Response Response Status O

Cl 45 SC 45.2.7.13.1 P 64 L 49 # I-75

Slavick, Jeff Broadcom Inc

Comment Type TR Comment Status X

Bit 6 is related to the negotiation of FEC operation and not the Port Type. So the first paragraph that begins with "When the Auto-Negotiation" should be its own sub-clause similar to 45.2.7.12.2

SuggestedRemedy

Revert the text of 45.2.7.13.1 to original baseline text.

Make the first paragraph of 45.2.7.13.1 its own new sub-clause

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 161 SC 161.5.2.6 P 134 L 46 # I-76  
 Slavick, Jeff Broadcom Inc  
 Comment Type E Comment Status X  
 With the breaking up of 161.5.2.6 into two sub-clauses the introduction paragraph could use some pointers towards which sub-clause it's referring to.  
 SuggestedRemedy  
 Add "(see 161.5.2.6.2)" after the word re-inserted on line 46  
 Add "(see 161.6.2.6.1)" at the end of the first sentence of 161.5.2.6  
 Proposed Response Response Status O

Cl 161 SC 161.5.2.6.1 P 135 L 50 # I-77  
 Slavick, Jeff Broadcom Inc  
 Comment Type E Comment Status X  
 The introduction paragraph and the first sentence of this sub-clause call this a "function"  
 SuggestedRemedy  
 Change the sub-clause title to be "Alignment marker mapping function"  
 Proposed Response Response Status O

Cl 162 SC 162.8.11 P 164 L 42 # I-78  
 Slavick, Jeff Broadcom Inc  
 Comment Type TR Comment Status X  
 In D2.2 the use\_quiet\_in\_training variable found in Cl136 is set to TRUE for non-50Gbps PHYs. In the current baseline draft use\_quiet\_in\_training being set to TRUE is implementation dependent.  
 SuggestedRemedy  
 In the list of exceptions add:  
 h) The variable use\_quiet\_in\_training is set to TRUE (see 136.8.11.7.1)  
 Proposed Response Response Status O

Cl 162 SC 162.8.2 P 162 L 35 # I-79  
 Lusted, Kent Intel Corporation  
 Comment Type TR Comment Status X  
 The IEEE P802.3dc revision project made a change to the PMD control state diagram referenced in the P802.3ck draft. The PMD transmit function now has three operating modes, DATA, TRAINING and QUIET. (see IEEE P802.3dc D3.0 Cl 136.8.2 on p5315, line 49). The 3ck text does not specify the QUIET mode nor it's use.  
 SuggestedRemedy  
 Change the first sentence of Cl 162.8.11 to include the QUIET state by changing the sentence to "The PMD transmit function has three operating modes: DATA, TRAINING, and QUIET."  
 Add a second sentence to the first paragraph in Cl 162.8.11: "Support for the QUIET operating mode is required and implementations shall set the variable use\_quiet\_in\_training (see 136.8.11.7.1) to TRUE."  
 Add a new paragraph to the end of Cl 162.8.11 that describes the QUIET mode: "When operating in QUIET mode the PMD transmit function shall turn off the transmitter such that the transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max) with Tx disabled in Table 136-11."  
 Proposed Response Response Status O

Cl 73 SC 73.6.5 P 71 L 33 # I-80  
 Lusted, Kent Intel Corporation  
 Comment Type TR Comment Status X  
 The text describing the use of bit F4 in 73.6.5 differs enough from Cl 73.6.5.a to imply that many 100G PHYs have the RS-FEC-Int capability. At this time, there are only two: 100GBASE-CR1 and 100GBASE-KR1. With the exception of 100GBASE-KP4, these are all 100GBASE-P PHY types and improved wording would make it more clear and align it with the title of 73.6.5.a.  
 SuggestedRemedy  
 Change the last sentence of the last paragraph to "F4 is used by 100GBASE-P PHYs where RS-FEC-Int (see Clause161) is an alternative to the default RS-FEC (see Clause91)."  
 Additionally, change item (e) in the list of Cl 73.6.5 to be "F4 is 100GBASE-P RS-FEC-Int requested"  
 Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 80 SC 80.1.3 P 76 L 42 # I-81  
 Lusted, Kent Intel Corporation  
 Comment Type E Comment Status X  
 there is an extra "in" at the start of the bullets for Clause 162 and Clause 163 list items.  
 SuggestedRemedy  
 in 80.1.3, list item i) change:  
 "in Clause 162 for 100GBASE-CR1" to " Clause 162 for 100GBASE-CR1" and "in  
 Clause163 for 100GBASE-KR1" to "Clause163 for 100GBASE-KR1"  
 Proposed Response Response Status O

Cl FM SC FM P 1 L 34 # I-82  
 Grow, Robert RMG Consulting  
 Comment Type E Comment Status X  
 Don't forget to update copyright year here, next page, and in the footer when producing the  
 next draft  
 SuggestedRemedy  
 Update framemaker variable and inspect front pages and footer to to assure all use the  
 vairable and if not, update.  
 Proposed Response Response Status O

Cl FM SC FM P 11 L 3 # I-83  
 Grow, Robert RMG Consulting  
 Comment Type E Comment Status X  
 Missing Amendment #.  
 SuggestedRemedy  
 Amendment 5  
 Proposed Response Response Status O

Cl FM SC FM P 11 L 17 # I-84  
 Grow, Robert RMG Consulting  
 Comment Type E Comment Status X  
 Slight differences from P802.3/D3.0 front matter.  
 SuggestedRemedy  
 Update Introduction text to match the most recent P802.3 draft.  
 Proposed Response Response Status O

Cl FM SC FM P 13 L 3 # I-85  
 Grow, Robert RMG Consulting  
 Comment Type E Comment Status X  
 No amendment numbers on descriptions of amendments 3 through 5  
 SuggestedRemedy  
 Add Amendment number as on Amendment 1 through Amendment 2.  
 Proposed Response Response Status O

Cl FM SC FM P 13 L 9 # I-86  
 Grow, Robert RMG Consulting  
 Comment Type E Comment Status X  
 PHY is the acronym for Physical Layer Device, not Physical Layer. The self description in  
 P802.3db/D2.1 deletes "(PHY)".  
 SuggestedRemedy  
 Delete "(PHY)"  
 Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

CI **FM** SC **FM** P **13** L **20** # **I-87**

Grow, Robert RMG Consulting

Comment Type **E** Comment Status **X**

While the integrity of copying self descriptions exactly is to be commended, perhaps changing 2018 to 202x on Amendment 2 could be done. Multiple comments were submitted on P802.3de/D2.1 about the 2018 date of the base standard in the self description (proposed accept). P802.3cs/D3.0 has a significantly different self description.

*SuggestedRemedy*

When producing the latest draft, check for updates to the self descriptions of Amendments 2 and 3. Update the P802.3de reference to 2018 in any case. Delete the note.

Proposed Response Response Status **O**

CI **80** SC **80.2.3** P **80** L **33** # **I-88**

Grow, Robert RMG Consulting

Comment Type **ER** Comment Status **X**

Capitalization of "forward error correction" has been made consistent in P802.3/D3.0.

*SuggestedRemedy*

A search and replace will find 8 places where capitalization needs to be corrected to lower case in subclause headings and text.

Proposed Response Response Status **O**

CI **162** SC **162.9.2** P **165** L **45** # **I-89**

Grow, Robert RMG Consulting

Comment Type **ER** Comment Status **X**

Similar misuses of "comprise" have been rewritten using "compose" in P802.3/D3.0. This text also contradicts other text where a path is composed of one or more lanes. In general in 802.3 a data path is composed of a set of signals (e.g., xMII), one or more lanes in other sublayer descriptions, etc. Here, it states that a "path corresponds to one MDI lane" yet on p. 256, l. 12 it says "Each 100GAUI-1, 200GAUI-2, and 400GAUI-4 C2M data path contains one, two, or four differential lanes." This subclause is titled signal path, yet the text uses path without qualifier. In other parts of the document "channel signal path" is used. This in general is confusing!

*SuggestedRemedy*

162.9.2 MDI connections

The MDI transmit and receive data paths are point-to-point connections. Each MDI data path is composed of one or more MDI lane(s). Each MDI lane is composed of two complementary signals, forming a balanced differential pair.

For 100GBASE-CR1, there is one differential lane in each direction for a total of two pairs, or four connections. For 200GBASE-CR2, there are two differential lanes in each direction for a total of four pairs, or eight connections. For 400GBASE-CR4, there are four differential lanes in each direction for a total of eight pairs, or sixteen connections.

Proposed Response Response Status **O**

CI **163** SC **163.11** P **218** L **37** # **I-90**

Grow, Robert RMG Consulting

Comment Type **E** Comment Status **X**

Similar misuses of "comprise" have been rewritten using "compose" in P802.3/D3.0.

*SuggestedRemedy*

"The MDI is composed of..."

Proposed Response Response Status **O**

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 120F SC 120F.1 P 237 L 43 # I-91  
 Grow, Robert RMG Consulting  
 Comment Type E Comment Status X  
 Similar misuses of "comprise" have been rewritten using "compose" in P802.3/D3.0.  
 SuggestedRemedy  
 The C2M interface is composed of independent transmit and receive data paths.  
 Proposed Response Response Status O

Cl 116 SC 116.1.3 P 96 L 34 # I-94  
 Parsons, Earl CommScope, Inc.  
 Comment Type E Comment Status X  
 802.3db modifies Table 116-2. 400GBASE-VR4 now comes before 400GBASE-SR16.  
 SuggestedRemedy  
 Replace the 400GBASE-SR16 row with 400GBASE-VR4.  
 Proposed Response Response Status O

Cl 120G SC 120G.1 P 256 L 11 # I-92  
 Grow, Robert RMG Consulting  
 Comment Type E Comment Status X  
 Similar misuses of "comprise" have been rewritten using "compose" in P802.3/D3.0.  
 SuggestedRemedy  
 The C2M interface is composed of independent transmit and receive data paths.  
 Proposed Response Response Status O

Cl 116 SC 116.1.4 P 98 L 18 # I-95  
 Parsons, Earl CommScope, Inc.  
 Comment Type T Comment Status X  
 200GBASE-VR2 and 200GBASE-SR2 should be in this table.  
 SuggestedRemedy  
 Add rows to Table 116-4 for 200GBASE-VR2 and 200GBASE-SR2. 200GBASE-VR2 should be the new top row and 200GBASE-SR2 should be between 200GBASE-SR4 and 200GBASE-DR4. Add the appropriate columns too.  
 Proposed Response Response Status O

Cl 80 SC 80.1.3 P 76 L 41 # I-93  
 Parsons, Earl CommScope, Inc.  
 Comment Type T Comment Status X  
 Include 100GBASE-SR1 and 100GBASE-VR1 from 802.3db.  
 SuggestedRemedy  
 Insert a line below the Clause 140 line in item i):  
 "-- Clause 167 for 100GBASE-VR1 and 100GBASE-SR1"  
 Proposed Response Response Status O

Cl 116 SC 116.1.4 P 99 L 18 # I-96  
 Parsons, Earl CommScope, Inc.  
 Comment Type T Comment Status X  
 400GBASE-VR4 and 400GBASE-SR4 should be in Table 116-5.  
 SuggestedRemedy  
 Add new rows and columns for 400GBASE-VR4 and 400GBASE-SR4. 400GBASE-VR4 should be the new top row. 400GBASE-SR4 should be between 400GBASE-SR8 and 400GBASE-SR4.2.  
 Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

CI 116 SC 116.2.5 P 99 L 42 # I-97

Parsons, Earl CommScope, Inc.

Comment Type T Comment Status X

Add reference to Clause 167 to these two sentences.

SuggestedRemedy

The 200GBASE-R PMDs and their corresponding media are specified in Clause 121, Clause 122, and Clause 136 through Clause 138, Clause 162, Clause 163, and Clause 167. The 400GBASE-R PMDs and their corresponding media are specified in Clause 122 through Clause 124, Clause 138, and Clause 150, Clause 162, Clause 163, and Clause 167.

Proposed Response Response Status O

CI 116 SC 116.4 P 101 L 17 # I-98

Parsons, Earl CommScope, Inc.

Comment Type E Comment Status X

802.3db added 400GBASE-VR4 to Table 116-7 above 400GBASE-SR16

SuggestedRemedy

Replace the 400GBASE-SR16 row with 400GBASE-VR4.

Proposed Response Response Status O

CI 116 SC 116.5 P 102 L 13 # I-99

Parsons, Earl CommScope, Inc.

Comment Type T Comment Status X

Add references to Clause 167.3.2 to Table 116-8 and Table 116-9 as in D2.1 of 802.3db

SuggestedRemedy

Per comment

Proposed Response Response Status O

CI 167 SC 167 P 225 L 1 # I-100

Parsons, Earl CommScope, Inc.

Comment Type T Comment Status X

Include modification to Clause 167 (from 802.3db).

SuggestedRemedy

Show modified Table 167-1 and Table 167-2 with rows for 120F--100GAUI-1 C2C and 120G--100GAUI1 C2M.

Proposed Response Response Status O

CI 163 SC 163.9.2 P 203 L 43 # I-101

Mellitz, Richard Samtec, Inc.

Comment Type TR Comment Status X

Low frequency CM will not be very dependent on a test fixture. Signal to AC common-mode noise ratio, SCMR (min), is related to the Peak Pulse and used to compensate for test fixture loss. Since the low frequency the loss is very small the tp0v compensation is not correct. As demonstrated in mellitz\_3k\_adhoc\_01\_120821 noise originating from a power supply or other low frequency sources can be detrimental.

SuggestedRemedy

Add a new line to table 163-5 called maximum low frequency AC common mode max peak to peak noise (V\_CMPP) and set to 30 mV. Create a new section for such indicating the a low pass 4th order Bessel Thomson filter with a 3 dB point of 10 MHz is to be applied to the CM measurement. Additionally in section 163.9.2.7 indicate that the a high pass 4th order Bessel Thomson filter with a 3 dB point of 10 MHz is to be applied to the AC CM measurement and set SCMR (min) to 11.8 dB. See presentation.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 120F SC 120F.3.1 P 239 L 13 # I-102

Mellitz, Richard Samtec, Inc.

Comment Type TR Comment Status X

Low frequency CM will not be very dependent on a test fixture. Signal to AC common-mode noise ratio, SCMR (min), is related to the Peak Pulse and used to compensate for test fixture loss. Since the low frequency the loss is very small the tp0v compensation is not correct. As demonstrated in mellitz\_3k\_adhoc\_01\_120821 noise originating from a power supply or other low frequency sources can be detrimental,

SuggestedRemedy

Add a new line to table 120F-1 called maximum low frequency AC common mode max peak to peak noise (V\_CMPP) and set to 30 mV. Create a new section for such indicating the a low pass 4th order Bessel Thomson filter with a 3 dB point of 10 MHz is to be applied to the CM measurement. Additionally in section 163.9.2.7 indicate that the a high pass 4th order Bessel Thomson filter with a 3 dB point of 10 MHz is to be applied to the AC CM measurement and set SCMR (min) to 10.7 dB. See presentation.

Proposed Response Response Status O

Cl 162 SC 162.9.3 P 166 L 24 # I-103

Mellitz, Richard Samtec, Inc.

Comment Type TR Comment Status X

RMS is poor indicator for CM mode noise. See CM histograms in mellitz\_3k\_adhoc\_01\_120821, mellitz\_3ck\_01a\_0721, and mellitz\_3ck\_adhoc\_01\_121620. Clause 163.9.2.7 defines a more meaningful parameter V\_CMPP as the peak-to-peak AC common-mode voltage.

SuggestedRemedy

Replace "AC common-mode RMS voltage, v\_cmi (max)" with V\_CMPP as the peak-to-peak AC common-mode voltage and set to 223 mV. See presentation.

Proposed Response Response Status O

Cl 120G SC 120G.3.1 P 258 L 13 # I-104

Mellitz, Richard Samtec, Inc.

Comment Type TR Comment Status X

RMS is poor indicator for CM mode noise. See CM histograms in mellitz\_3k\_adhoc\_01\_120821, mellitz\_3ck\_01a\_0721, and mellitz\_3ck\_adhoc\_01\_121620. Clause 163.9.2.7 defines a more meaningful parameter V\_CMPP as the peak-to-peak AC common-mode voltage.

SuggestedRemedy

Replace "AC common-mode output voltage (max, RMS)" with V\_CMPP as the peak-to-peak AC common-mode voltage and set to 213 mV but define the distribution range to be between 0.000005 to 0.999995. (1.e. 1e-5) See presentation.

Proposed Response Response Status O

Cl 120G SC 120G.3.2 P 261 L 7 # I-105

Mellitz, Richard Samtec, Inc.

Comment Type TR Comment Status X

RMS is poor indicator for CM mode noise. See CM histograms in mellitz\_3k\_adhoc\_01\_120821, mellitz\_3ck\_01a\_0721, and mellitz\_3ck\_adhoc\_01\_121620. Clause 163.9.2.7 defines a more meaningful parameter V\_CMPP as the peak-to-peak AC common-mode voltage.

SuggestedRemedy

Replace "AC common-mode output voltage (max, RMS)" with V\_CMPP as the peak-to-peak AC common-mode voltage and set to 213 mV but define the distribution range to be between 0.000005 to 0.999995. (1.e. 1e-5). See presentation

Proposed Response Response Status O

Cl 120F SC 120F.3.1 P 239 L 13 # I-106

Mellitz, Richard Samtec, Inc.

Comment Type TR Comment Status X

DER0 for 120F is 1e-5 and DER0 for 163 is 1e-4. The reference to 163.9.2.7 need a reference to adjust for DER0.

SuggestedRemedy

Add a footnote to SCMR(min) to compute V\_CMPP to with the distribution range to be between 0.000005 to 0.999995. (1.e. 1e-5).

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 120G SC 120G.3.1 P 258 L 21 # I-107

Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.

Comment Type TR Comment Status X

ESMW/EW were removed in draft 1.4 with the introduction of the +/- 50 mUI rectangular window with VEO and VEC limits not passing the task force introduced Gaussian window which in effect reduces implicit minimum receiver eye opening. With current Gaussian window for typical high loss channel EW can be as little as 120 mUI, in comparisons CL120E min ESMW=220 mU. The 120 mUI can be further degraded for lower loss channel with pathological reflections/jitter may result in EW <100 mUI. Eye width opening is as critical as VEC/VEO, without explicit EW specifications and with current Gaussian window there is significant interoperability risk.

SuggestedRemedy

An explicit ESMW>=175 mUI specifications which is available in the scope might be the simplest, other alternative would be to go back to rectangular mask with +/- 50 mUI or introduce 10 sides mask as demonstrated in [https://www.ieee802.org/3/ck/public/21\\_01/dawe\\_3ck\\_01\\_0121.pdf](https://www.ieee802.org/3/ck/public/21_01/dawe_3ck_01_0121.pdf)

Proposed Response Response Status O

Cl 120G SC 120G.3.2 P 261 L 12 # I-108

Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.

Comment Type TR Comment Status X

ESMW/EW were removed in draft 1.4 with the introduction of the +/- 50 mUI rectangular window with VEO and VEC limits not passing the task force introduced Gaussian window which in effect reduces implicit minimum receiver eye opening. With current Gaussian window for typical high loss channel EW can be as little as 120 mUI, in comparisons CL120E min farend ESMW=200 mU. The 120 mUI can be further degraded for lower loss channel with pathological reflections/jitter may result in EW <100 mUI. Eye width opening is as critical as VEC/VEO, without explicit EW specifications and with current Gaussian window there is significant interoperability risk.

SuggestedRemedy

An explicit ESMW>=150 mUI specifications which is available in the scope might be the simplest, other alternative would be to go back to rectangular mask with +/- 50 mUI or introduce 10 sides mask as demonstrated in [https://www.ieee802.org/3/ck/public/21\\_01/dawe\\_3ck\\_01\\_0121.pdf](https://www.ieee802.org/3/ck/public/21_01/dawe_3ck_01_0121.pdf)

Proposed Response Response Status O

Cl 120G SC 120G.3.2.2 P 262 L 27 # I-109

Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.

Comment Type TR Comment Status X

Fig 120G-7 shows the most trivial component in the the capacitors, why not other components such as CDR, TX/RX optics?

SuggestedRemedy

Suggest removing what is inside the module just show a box for module under test

Proposed Response Response Status O

Cl 120G SC 120G.3.2 P 260 L 6 # I-110

Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.

Comment Type TR Comment Status X

AC common mode at TP1a which include the channel is specified as 25 mV but also AC common mode for module output which doesn't include the channel specified as 25 mV. Need allocation for the channel!

SuggestedRemedy

Please reduce the AC common mode at TP4 to 20 mV RMS

Proposed Response Response Status O

Cl 120G SC 120G.3.3 P 264 L 6 # I-111

Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.

Comment Type TR Comment Status X

AC common mode at TP1a which include the channel is specified as 25 mV but also AC common mode for module output which doesn't include the channel specified as 25 mV. Need allocation for the channel!

SuggestedRemedy

Please reduce the AC common mode at TP4 to 20 mV RMS

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl **120G** SC **120G.3.3.5.1** P **265** L **50** # **I-112**  
 Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.  
 Comment Type **TR** Comment Status **X**  
 Not sure why you are referencing Table 120F-3, maybe the intention was Figure 120F-3!  
 SuggestedRemedy  
 Please change to Figure 120F-3  
 Proposed Response Response Status **O**

Cl **120G** SC **120G.3.3.5.1** P **265** L **52** # **I-113**  
 Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.  
 Comment Type **TR** Comment Status **X**  
 What is the intention of defining no equalization state, I don't see it being used!  
 SuggestedRemedy  
 This sentence is either incomplete or should be removed.  
 Proposed Response Response Status **O**

Cl **120G** SC **120G.3.3.5.1** P **266** L **27** # **I-114**  
 Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.  
 Comment Type **TR** Comment Status **X**  
 Open arrow is defiend to be for mechanical insertion, having additional open arrow on the right side of MCB indicate MCB plugs in to the scope  
 SuggestedRemedy  
 You could remove the open arrow on the MCB  
 Proposed Response Response Status **O**

Cl **120G** SC **120G.3.3.5.2** P **267** L **39** # **I-115**  
 Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.  
 Comment Type **TR** Comment Status **X**  
 ESMW/EW were removed in draft 1.4 with the introduction of the +/- 50 mUI rectangular window with VEO and VEC limits not passing the task force introduced Gaussian window which in effect reduces implicit minimum receiver eye opening. With current Gaussian window for typical high loss channel EW can be as little as 120 mUI, in comparisons CL120E min farend ESMW=200 mU. The 120 mUI can be further degraded for lower loss channel with pathological reflections/jitter may result in EW <100 mUI. Eye width opening is as critical as VEC/VEO, without explicit EW specifications and with current Gaussian window there is significant interoperability risk.

SuggestedRemedy  
 An explicit ESMW>=150 mUI specifications which is available in the scope might be the simplest, other alternative would be to go back to rectangular mask with +/- 50 mUI or introduce 10 sides mask as demonstrated in [https://www.ieee802.org/3/ck/public/21\\_01/dawe\\_3ck\\_01\\_0121.pdf](https://www.ieee802.org/3/ck/public/21_01/dawe_3ck_01_0121.pdf)  
 Proposed Response Response Status **O**

Cl **120G** SC **120G.3.4** P **269** L **19** # **I-116**  
 Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.  
 Comment Type **TR** Comment Status **X**  
 ESMW/EW were removed in draft 1.4 with the introduction of the +/- 50 mUI rectangular window with VEO and VEC limits not passing the task force introduced Gaussian window which in effect reduces implicit minimum receiver eye opening. With current Gaussian window for typical high loss channel EW can be as little as 120 mUI, in comparisons CL120E min ESMW=220 mU. The 120 mUI can be further degraded for lower loss channel with pathological reflections/jitter may result in EW <100 mUI. Eye width opening is as critical as VEC/VEO, without explicit EW specifications and with current Gaussian window there is significant interoperability risk.  
 SuggestedRemedy  
 An explicit ESMW>=175 mUI specifications which is available in the scope might be the simplest, other alternative would be to go back to rectangular mask with +/- 50 mUI or introduce 10 sides mask as demonstrated in [https://www.ieee802.org/3/ck/public/21\\_01/dawe\\_3ck\\_01\\_0121.pdf](https://www.ieee802.org/3/ck/public/21_01/dawe_3ck_01_0121.pdf)  
 Proposed Response Response Status **O**

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl **120G** SC **120G.3.4.3.1** P **270** L **38** # **I-117**  
 Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.  
 Comment Type **TR** Comment Status **X**  
 Open arrow is defiend to be for mechanical insertion, having additional open arrow on the right side of MCB incidcate MCB plugs in to the scope  
 SuggestedRemedy  
 You could remove the open arrow on the MCB  
 Proposed Response Response Status **O**

Cl **162C** SC **162C.1** P **303** L **10** # **I-120**  
 Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.  
 Comment Type **TR** Comment Status **X**  
 Table 162C-3 has number of error due to lack of pin alignment between OSFP and QSFP/QSFP-DD800  
 SuggestedRemedy  
 These need to be broken in to three tables: SFP112/SFP-DD112/DSFP, QSFP112/QSFP-DD800, and the 3rd table for OSFP. Plesae see Lusted-Ghiasi presentation.  
 Proposed Response Response Status **O**

Cl **1** SC **1.4** P **32** L **65** # **I-118**  
 Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.  
 Comment Type **T** Comment Status **X**  
 SFP-DD operates at 50G and with SFP-DD112 there is no reason to include SFP-DD  
 SuggestedRemedy  
 Please remvoe SFP-DD  
 Proposed Response Response Status **O**

Cl **162** SC **162.8.11** P **164** L **42** # **I-121**  
 Healey, Adam Broadcom Inc.  
 Comment Type **T** Comment Status **X**  
 In IEEE P802.3ck/D2.2, the definition of the variable use\_quiet\_in\_training included the statement that "this variable is always set to FALSE for 50 Gb/s per lane PHYs, otherwise it is set to TRUE." When the modifications to 136.8 were moved to the IEEE P802.3 (IEEE 802.3dc) revision project, the statement was modified to state that "the value of this variable is implementation dependent." Since there is no superseding statement in 162.8.11, the value of use\_quiet\_in\_training is implementation dependent as defined in the base document and not required to be TRUE for 100G/lane as it was in IEEE P802.3ck/D2.2.  
 SuggestedRemedy  
 If the intent is require use\_quiet\_in\_training to be TRUE for 100G/lane PHYs, then add the following item to the list: "f) The variable use\_quiet\_in\_training is set to TRUE."  
 Proposed Response Response Status **O**

Cl **162B** SC **162B.5.4** P **300** L **38** # **I-119**  
 Ghiasi, Ali Ghiasi Quantum LLC,Marvell Semiconductor, Inc.  
 Comment Type **TR** Comment Status **X**  
 I suggest TF7 under feature add single-lane  
 SuggestedRemedy  
 Single-lane, SFP112, ..  
 Proposed Response Response Status **O**

Cl **30** SC **30.5.1.1.16** P **36** L **39** # **I-122**  
 Healey, Adam Broadcom Inc.  
 Comment Type **E** Comment Status **X**  
 IEEE P802.3ck will be an amendment to the next revision of IEEE Std 802.3. The changes shown in the last paragraph of the "BEHAVIOR DEFINED AS:" section do not correspond to the text in the latest revision draft (D3.0).  
 SuggestedRemedy  
 Specify the changes relative to the text in IEEE P802.3 (IEEE 802.3dc) D3.0.  
 Proposed Response Response Status **O**

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Cl **FM** SC **FM** P **4** L **32** # **I-123**  
 Healey, Adam Broadcom Inc.  
 Comment Type **E** Comment Status **X**  
 The "Important Notices and Disclaimers Concerning IEEE Standards Documents" does not align with the latest template.  
*SuggestedRemedy*  
 Update the frontmatter to be consistent with the latest template. Note changes to the second paragraph of "Notice and Disclaimer of Liability Concerning the Use of IEEE Standards Documents", two additional paragraphs under "Patents", and other minor changes.  
 Proposed Response Response Status **O**

Cl **162** SC **162.9.4.3.3** P **176** L **23** # **I-124**  
 Calvin, John Keysight Technologies  
 Comment Type **T** Comment Status **X**  
 ADD formula (162-78) has a discriminant which under many legitimate conditions can be negative, causing the expression to fail. The accompanying Note 2 asserts "If this does not hold, a different transmitter should be used in the test setup." This TE tool provider is seeing a jump in customer complaints that the BERT they purchased for receiver testing can regularly trigger this negative discriminant condition. Something more constructive than "a different transmitter should be used" needs to be considered here.  
*SuggestedRemedy*  
 Consider the following contribution :  
[https://www.ieee802.org/3/ck/public/adhoc/apr14\\_21/hidaka\\_3ck\\_adhoc\\_01\\_041421.pdf](https://www.ieee802.org/3/ck/public/adhoc/apr14_21/hidaka_3ck_adhoc_01_041421.pdf)  
 which speaks to this exact issue. Note pages 4 and 5 outline the conditions whereby this discriminant can be negative with instrument grade test tools.  
 Note 2 in subclause 162.9.4.3.3 should be revised to say the following:  
 "The Calculation of ADD may, under certain conditions pose a negative discriminant. If this condition occurs, the recommended solution is to increase DJ to increase the ADD parameter till the discriminant is positive"  
 Proposed Response Response Status **O**

Cl **162** SC **162.5** P **157** L **17** # **I-125**  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type **E** Comment Status **X**  
 PICS entry seems missing for "shall" for the max delays listed in Table 162-4.  
*SuggestedRemedy*  
 Add a PICS entry "The sum of the transmit and the receive delay at one end of the link shall be no more than the maximum delays listed in Table 162-4" with a reference to clause 162.5.  
 Proposed Response Response Status **O**

Cl **162** SC **162.6.1** P **158** L **1** # **I-126**  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type **E** Comment Status **X**  
 PICS entry seems missing for "shall" for the skew at SP3 for 100GBASE-CR1 less than 54ns.  
*SuggestedRemedy*  
 Add a PICS entry "The Skew at SP3 for 100GBASE-CR1 shall be less than 54ns" with a reference to clause 162.6.1.  
 Proposed Response Response Status **O**

Cl **162** SC **162.6.1** P **158** L **4** # **I-127**  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type **E** Comment Status **X**  
 PICS entry seems missing for "shall" for the skew at SP4 for 100GBASE-CR1 less than 134ns.  
*SuggestedRemedy*  
 Add a PICS entry "The Skew at SP4 for 100GBASE-CR1 shall be less than 134ns" with a reference to clause 162.6.1.  
 Proposed Response Response Status **O**

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Cl 162 SC 162.6.1 P 158 L 8 # I-128  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP5 for 100GBASE-CR1 less than 145ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP5 for 100GBASE-CR1 shall be less than 145ns" with a reference to clause 162.6.1.  
 Proposed Response Response Status O

Cl 162 SC 162.6.2 P 158 L 26 # I-131  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP4 for 200GBASE-CR2 and 400GBASE-CR4 less than 134ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP4 for 200GBASE-CR2 and 400GBASE-CR4 shall be less than 134ns" with a reference to clause 162.6.2.  
 Proposed Response Response Status O

Cl 162 SC 162.6.2 P 158 L 23 # I-129  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP3 for 200GBASE-CR2 and 400GBASE-CR4 less than 54ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP3 for 200GBASE-CR2 and 400GBASE-CR4 shall be less than 54ns" with a reference to clause 162.6.2.  
 Proposed Response Response Status O

Cl 162 SC 162.6.2 P 158 L 26 # I-132  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew variation at SP4 for 200GBASE-CR2 and 400GBASE-CR4 less than 3.4ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew Variation at SP4 for 200GBASE-CR2 and 400GBASE-CR4 shall be less than 3.4ns" with a reference to clause 162.6.2.  
 Proposed Response Response Status O

Cl 162 SC 162.6.2 P 158 L 23 # I-130  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew variation at SP3 for 200GBASE-CR2 and 400GBASE-CR4 less than 600ps.  
 SuggestedRemedy  
 Add a PICS entry "The Skew Variation at SP3 for 200GBASE-CR2 and 400GBASE-CR4 shall be less than 600ps" with a reference to clause 162.6.2.  
 Proposed Response Response Status O

Cl 162 SC 162.6.2 P 158 L 30 # I-133  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP5 for 200GBASE-CR2 and 400GBASE-CR4 less than 145ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP5 for 200GBASE-CR2 and 400GBASE-CR4 shall be less than 145ns" with a reference to clause 162.6.2.  
 Proposed Response Response Status O

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Cl 162 SC 162.6.2 P 158 L 30 # I-134  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew variation at SP5 for 200GBASE-CR2 and 400GBASE-CR4 less than 3.6ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew Variation at SP5 for 200GBASE-CR2 and 400GBASE-CR4 shall be less than 3.6ns" with a reference to clause 162.6.2.  
 Proposed Response Response Status O

Cl 162 SC 162.7 P 158 L 37 # I-135  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for mapping of MDIO variables and registers.  
 SuggestedRemedy  
 Add a PICS entry "MDIO shall map MDIO variables and registers to PMD variables as shown in Table 162-5 through Table 162-7" with a reference to clause 162.7.  
 Proposed Response Response Status O

Cl 162 SC 162.9.3.1.2 P 169 L 8 # I-136  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 The minimum value of the linear fit pulse peak ratio should not be described in the body text. The text is inconsistent with Table 162-10, because the text says "greater than" but Table 162-10 implicates "greter than or equal to". 0.397 is allowed in Table 162-10 as the minimum value, but not allowed in the body text. Avoid the minimum value in the text and the text should refer to the table.  
 SuggestedRemedy  
 Change "The linear fit pulse peak ratio shall be greater than 0.397 after the transmit equalizer initial condition has been set to preset 1 (no equalization)." to "The linear fit pulse peak ratio shall meet the requirements specified in Table 162-10 after the transmit equalizer initial condition has been set to preset 1 (no equalization)."  
 Proposed Response Response Status O

Cl 162 SC 162.14.4.2 P 194 L 17 # I-137  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 Item PC6 refers to clause 136.8.11.4.1.  
 SuggestedRemedy  
 Change the reference of PC6 from 136.8.11.4.1 to 162.9.3.1.3.  
 Proposed Response Response Status O

Cl 162 SC 162.11.7 P 185 L 46 # I-138  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type T Comment Status X  
 The meaning of "any channel within the cable assembly" is not clear.  
 SuggestedRemedy  
 Change "any channel" to "any lane".  
 Proposed Response Response Status O

Cl 162 SC 162.14.4.5 P 196 L 8 # I-139  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type T Comment Status X  
 The meaning of "all channels within the cable assembly" is not clear.  
 SuggestedRemedy  
 Change "all channels" with "all lanes".  
 Proposed Response Response Status O

Cl 163 SC 163.13.4.3 P 222 L 51 # I-140  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 The border between TC9 and TC10 is thick.  
 SuggestedRemedy  
 Make the border between TC9 and TC10 same as other rows.  
 Proposed Response Response Status O

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Cl 163 SC 163.5 P 199 L 51 # I-141  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the max delays listed in Table 163-4.  
 SuggestedRemedy  
 Add a PICS entry "The sum of the transmit and receive delays at one end of the link shall be no more than the maximum delays listed in Table 163-4" with a reference to clause 163.5.  
 Proposed Response Response Status O

Cl 163 SC 163.6.1 P 201 L 25 # I-144  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP5 for 100GBASE-KR1 less than 145ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP5 for 100GBASE-KR1 shall be less than 145ns" with a reference to clause 163.6.1.  
 Proposed Response Response Status O

Cl 163 SC 163.6.1 P 201 L 18 # I-142  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP3 for 100GBASE-KR1 less than 54ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP3 for 100GBASE-KR1 shall be less than 54ns" with a reference to clause 163.6.1.  
 Proposed Response Response Status O

Cl 163 SC 163.6.2 P 201 L 40 # I-145  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP3 for 200GBASE-KR2 and 400GBASE-KR4 less than 54ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP3 for 200GBASE-KR2 and 400GBASE-KR4 shall be less than 54ns" with a reference to clause 163.6.2.  
 Proposed Response Response Status O

Cl 163 SC 163.6.1 P 201 L 21 # I-143  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP4 for 100GBASE-KR1 less than 134ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP4 for 100GBASE-KR1 shall be less than 134ns" with a reference to clause 163.6.1.  
 Proposed Response Response Status O

Cl 163 SC 163.6.2 P 201 L 40 # I-146  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew variation at SP3 for 200GBASE-KR2 and 400GBASE-KR4 less than 600ps.  
 SuggestedRemedy  
 Add a PICS entry "The Skew Variation at SP3 for 200GBASE-KR2 and 400GBASE-KR4 shall be less than 600ps" with a reference to clause 163.6.2.  
 Proposed Response Response Status O

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Cl 163 SC 163.6.2 P 201 L 43 # I-147  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP4 for 200GBASE-KR2 and 400GBASE-KR4 less than 134ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP4 for 200GBASE-KR2 and 400GBASE-KR4 shall be less than 134ns" with a reference to clause 163.6.2.  
 Proposed Response Response Status O

Cl 163 SC 163.6.2 P 201 L 46 # I-150  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew variation at SP5 for 200GBASE-KR2 and 400GBASE-KR4 less than 3.6ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew Variation at SP5 for 200GBASE-KR2 and 400GBASE-KR4 shall be less than 3.6ns" with a reference to clause 163.6.2.  
 Proposed Response Response Status O

Cl 163 SC 163.6.2 P 201 L 43 # I-148  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew variation at SP4 for 200GBASE-KR2 and 400GBASE-KR4 less than 3.4ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew Variation at SP4 for 200GBASE-KR2 and 400GBASE-KR4 shall be less than 3.4ns" with a reference to clause 163.6.2.  
 Proposed Response Response Status O

Cl 163 SC 163.13.4.3 P 222 L 49 # I-151  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 "peak" is missing.  
 SuggestedRemedy  
 Change "Difference linear fit pulse ratio" to "Difference linear fit pulse peak ratio".  
 Proposed Response Response Status O

Cl 163 SC 163.6.2 P 201 L 46 # I-149  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the skew at SP5 for 200GBASE-KR2 and 400GBASE-KR4 less than 145ns.  
 SuggestedRemedy  
 Add a PICS entry "The Skew at SP5 for 200GBASE-KR2 and 400GBASE-KR4 shall be less than 145ns" with a reference to clause 163.6.2.  
 Proposed Response Response Status O

Cl 163 SC 163.9.2.6 P 206 L 53 # I-152  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for the residual intersymbol interference ISI\_RES.  
 SuggestedRemedy  
 Add a PICS entry for residual intersymbol interference per Table 163-5 with a reference to clause 163.9.2.6.  
 Proposed Response Response Status O

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Cl 163 SC 163.9.2.7 P 207 L 9 # I-153  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "shall" for signal to AC common-mode noise ratio.  
 SuggestedRemedy  
 Add a PICS entry for signal to AC common-mode noise ratio per Table 163-5 with a reference to clause 163.9.2.7.  
 Proposed Response Response Status O

Cl 163 SC 163.9.2.7 P 207 L 10 # I-154  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 Table 163-11 does not define SCMR.  
 SuggestedRemedy  
 Change the reference to Table 163-11 with a reference to Table 163-5.  
 Proposed Response Response Status O

Cl 120G SC 120G.3.1 P 258 L 17 # I-155  
 Hidaka, Yasuo Credo Semiconductor  
 Comment Type E Comment Status X  
 PICS entry seems missing for "Steady-state voltage, v\_f (max)" in Table 120G-1.  
 SuggestedRemedy  
 Add a PICS entry for "Steady-state voltage" per Table 120G-1 with a reference to 120G.5.3.  
 Proposed Response Response Status O

Cl 162 SC 162.9.3 P 166 L 47 # I-156  
 Rysin, Alexander NVIDIA  
 Comment Type TR Comment Status X  
 J3u is strongly affected by limitations of measurement equipment. A performance metric that is less subject to measurement issues should be explored. Presentation will follow.  
 SuggestedRemedy  
 J3u max from 0.115 UI to 0.125 UI here, from 0.106 UI to 0.115 in 163 and 120F. In COM tables, change A\_dd from 0.02 to 0.0185, change Jrms from 0.1 to 0.115. Alternatively, change the measurement method.  
 Proposed Response Response Status O

Cl FM SC FM P 1 L 10 # I-157  
 Dawe, Piers J G NVIDIA  
 Comment Type E Comment Status X  
 Missing amendment number  
 SuggestedRemedy  
 Insert amendment number or a placeholder if the number is not known yet. Also on page 30 line 3. It would help if the placeholders were in the template.  
 Proposed Response Response Status O

Cl FM SC FM P 30 L 47 # I-158  
 Dawe, Piers J G NVIDIA  
 Comment Type E Comment Status X  
 As this is an amendment to 802.3dc, P802.3cn and P802.3cu have gone, and new readers need not know of them. Further, the editor's note would be more use to reviewers and editor if it listed the actual amendments that the editor has noted as running in parallel and affecting this draft, not just the concept. Also, it helps to state which amendments running in parallel are believed not to affect the draft, so the reviewer knows they have been considered. Apparently, only P802.3db affects this draft, but others might.  
 SuggestedRemedy  
 Change "(e.g., IEEE P802.3cn and IEEE P802.3cu)" to "(IEEE P802.3db; no impact is noted from IEEE P802.3dd, P802.3de, or IEEE P802.3cs)"  
 Proposed Response Response Status O

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Cl **FM** SC **FM** P **30** L **48** # **I-159**  
 Dawe, Piers J G NVIDIA  
 Comment Type **E** Comment Status **X**  
 "the same text and tables" so clashing edits to figures are OK?  
 SuggestedRemedy  
 Change to "the same portions of the draft standard".  
 Proposed Response Response Status

Cl **45** SC **45.2.1.131a** P **56** L **33** # **I-162**  
 Dawe, Piers J G NVIDIA  
 Comment Type **E** Comment Status **X**  
 Table layout  
 SuggestedRemedy  
 Make the second column wider and the third, narrower.  
 Proposed Response Response Status

Cl **45** SC **45.2.1.21** P **42** L **11** # **I-160**  
 Dawe, Piers J G NVIDIA  
 Comment Type **E** Comment Status **X**  
 P802.3db has changed this table, so the next row above is 200GBASE-VR2 ability not "Reserved".  
 SuggestedRemedy  
 Show the row above and below the rows this project adds so the context can be reviewed and some clashes spotted easily.  
 Change  
 1.23.14:9x7/x Reserved Value always 0 RO  
 to  
 1.23.9 200GBASE-VR2 ability 1 = PMA/PMD is able to perform 200GBASE-VR2 0 = PMA/PMD is not able to perform 200GBASE-VR2 RO  
 Adjust the instructions at line 3 to mention the preceding amendment(s) that affect this table (P802.3db).  
 Similarly for Table 45-27.  
 Proposed Response Response Status

Cl **91** SC **91.6.7a** P **91** L **5** # **I-163**  
 Dawe, Piers J G NVIDIA  
 Comment Type **T** Comment Status **X**  
 This paragraph seems to be written as if Clause 91 RS-FEC and Clause 161 RS-FEC-Int are in series, and 91 is bypassed when 161 is used. However, Figure 161-1 and Figure 91-1 show separate scenarios, one with Clause 91 RS-FEC and the other with Clause 161 RS-FEC-Int, but no pass-through arrangement.  
 SuggestedRemedy  
 Either show the two sublayers as in series, or describe them as alternatives.  
 Proposed Response Response Status

Cl **45** SC **45.2.1.116** P **45** L **22** # **I-161**  
 Dawe, Piers J G NVIDIA  
 Comment Type **E** Comment Status **X**  
 Misplaced "only"  
 SuggestedRemedy  
 Change "only applicable for PHYs that include multiple FEC sublayers" to "applicable only for PHYs that include multiple FEC sublayers"  
 Proposed Response Response Status

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Cl 91 SC 91.6.7a P91 L5 # I-164

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

This says "An MDIO interface or ... shall be provided to access the variable 100G\_RS\_FEC\_Enable for the RS-FEC sublayer. When the 100G\_RS\_FEC\_Enable variable is set to one, the RS-FEC sublayer performs the transmit function ... and the receive function ... . When the variable is set to zero, the ... RS-FEC sublayer is bypassed... .

So all implementations, whether they need this FEC enable/disable function or not, have to have the management variable, and they have to bypass the FEC function when the variable or bit is 0 (default). I think this breaks existing implementations twice over.

*SuggestedRemedy*

The requirement for this enable/disable switch should be tied to the first sentence "For PHYs supporting RS-FEC-Int operation". Change "An MDIO interface" to "For these PHYs, an MDIO interface". Then the text will agree with the PICS.

0 and 1 should be swapped so that the default is 0, FEC operating, which is what existing implementations do: per 45.2, "If a device supports the MDIO interface it shall respond to all possible register addresses ... The operation of an MMD shall not be affected by writes to reserved and unsupported register bits..."

Proposed Response Response Status O

Cl 91 SC 91.7.3 P92 L41 # I-165

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

There is a "major capability/option" "RS-FEC-Int is supported. 161 Used to form complete 100GBASE-CR1, or 100GBASE-KR1 PHY".

I don't see text in this clause or in 161 to justify this.

*SuggestedRemedy*

Add the text. In 161, state which PHY types use the RS-FEC-Int

Proposed Response Response Status O

Cl 161 SC 161.5.2.6.2 P137 L6 # I-166

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

What do you mean, "let"? In IEEE standards, we have shall, should, may and can. See 1.1.6.

*SuggestedRemedy*

Change "Let the set of vectors tx\_scrambled\_i<256:0> represent consecutive values of tx\_scrambled<256:0>" to "In the following, the set of vectors tx\_scrambled\_i<256:0> represent consecutive values of tx\_scrambled<256:0>", or "Consecutive values of tx\_scrambled<256:0> are represented by a set of vectors tx\_scrambled\_i<256:0>". Or use "Given" as on the previous page.

Proposed Response Response Status O

Cl 161 SC 161.5.2.6.2 P137 L7 # I-167

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

Something called "tx\_scrambled" appears without explanation. According to the text and figures 161-4 and 161-5, it is 257 bits long (but what is it?), but according to Fig 161-3 it's 2 RS symbols or 20 bits.

*SuggestedRemedy*

In 161.5.2.5, add a sentence saying that the transcoder output is tx\_scrambled which is a 257-bit block. In Figures 161-3, change "tx\_scrambled" to "Beginning of tx\_scrambled", pointing at row 0, if that is what is intended.

Proposed Response Response Status O

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Cl 162 SC 162.8.1 P 161 L 48 # I-168

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

"differential-mode to differential-mode insertion loss" is wordy and everyone understands just "insertion loss" to mean differential-mode to differential-mode if they know it's a system or component that uses differential signalling, which is made plain above. Similarly for return loss. The base document doesn't use this term, and uses "differential-mode insertion loss" only twice, in figures 128-4 and 130-4. But it does use "differential insertion loss" and "differential output return loss" many times, and unqualified "insertion loss" very many times.

SuggestedRemedy

Change "differential-mode to differential-mode" when an adjective to "differential-mode" (correct and unambiguous), "differential" (unambiguous, matches base document) or to nothing, throughout the document.

Proposed Response Response Status O

Cl 162 SC 162.8.1 P 161 L 53 # I-169

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

"The channel (see 162.11) is defined between the transmitter (TP0) and receiver (TP5) blocks to include the transmitter and receiver differential controlled impedance printed circuit board (PCB) differential-mode to differential-mode insertion loss and the cable assembly differential-mode to differential-mode insertion loss, as illustrated in Figure 162-2" - but discussing insertion loss is going off topic, it's not keeping to what the channel includes and we define other things about the channel, principally COM.

SuggestedRemedy

Change to "The channel (see 162.11) is defined between the transmitter (TP0) and receiver (TP5) blocks to include the transmitter and receiver differential controlled impedance printed circuit boards (PCBs), and the cable assembly, as illustrated in Figure 162-2."

Proposed Response Response Status O

Cl 162 SC 162.9.3 P 166 L 32 # I-170

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The draft CR loss budget wastes 3 dB in nearly every case. The relative range of host losses,  $6.875/2.3 = 3:1$ , is too small for switch layout yet not needed for NICs. The recommendation for the host traces plus BGA footprint and host connector footprint, 6.875 dB, compares very poorly with C2M's host insertion loss up to 11.9 dB, making passive copper to this draft expensive and unattractive for a switch, yet a full range of NICs can be made with only 3.75 dB. C2M already has short and long ports. Server-switch links are asymmetric in form factor (e.g. QSFP-DD to 2 x QSFP) and will get made with an asymmetric loss budget, so it would be better for the standard to regularise what will happen anyway with industry-standard registers. This change would also benefit CR switch-switch links because the low loss of the shortest ports would be recognised, so more of the ports in a switch (with higher loss) could be used for CR switch-switch links. The symmetric budget is used for some designs under way and may be useful in future for LOM, so it is kept here as "B", and the better way (A and C) added.

SuggestedRemedy

As in daw\_e\_3ck\_01a\_0721.pdf:  
 3 classes of CR ports, host loss allocations of A 9.5, B 6.875, C 3.75 dB. B is as D2.1. A connects to C, B to B or C, C to A, B or C.  
 Use 2 bits in the training control field to advertise A, B or C to the other end.  
 In Table 162-10, add limits A and C for linear fit pulse peak ratio (min). Change text in 162.9.3.1.2 to refer to the table.  
 In Table 162-14, add columns for Test 2 (high loss), A and C, with test channel insertion loss: A:  $6.875-3.75 = 3.125$  dB lower (20.5 dB to 21.5 dB), and C:  $9.5-6.875 = 2.625$  dB higher (26.25 dB to 27.25 dB). No change needed for Test 1.  
 In 162A.4, add equations for IL\_PCBmax and ILHostMax A and B and show them in Fig 162A-1 and 2. In 162A.5, add Value columns A, C in Table 162A-1 (ILChmin and ILMaxHost differ). Adjust figures 162A-3 and 4.  
 Add MDIO registers to report local and remote host ability to station management, for inventory and diagnostics.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162 SC 162.9.3 P 166 L 47 # I-171  
 Dawe, Piers J G NVIDIA  
 Comment Type **TR** Comment Status **X**  
 It appears that measured J3u looks bad for measurement reasons. We can choose a different worst jitter corner so that the measurement issues are less important.  
*SuggestedRemedy*  
 Change J3u max from 0.115 UI to 0.125 UI here, from 0.106 UI to 0.115 in Table 163-5, and from 0.118 UI to 0.128 UI in Table 120F-1. In all three COM tables, change A\_dd from 0.02 to 0.0185, change Jrms from 0.1 to 0.115. Alternatively, change the measurement method.  
 Proposed Response Response Status **O**

Cl 162 SC 162.9.3.1.2 P 169 L 1 # I-172  
 Dawe, Piers J G NVIDIA  
 Comment Type **T** Comment Status **X**  
 Table 162-10 says "Linear fit pulse peak ratio" and refers to this subclause whose title is "Steady-state voltage and linear fit pulse peak", and does not say what "pulse peak ratio" means. Nor does 162.9.3.1.1.  
*SuggestedRemedy*  
 Change the title to "Steady-state voltage and linear fit pulse peak ratio". Define linear fit pulse peak ratio.  
 Proposed Response Response Status **O**

Cl 162 SC 162.9.3.4 P 170 L 49 # I-173  
 Dawe, Piers J G NVIDIA  
 Comment Type **TR** Comment Status **X**  
 Something as vague and open-ended as "may be set lower than 4 MHz" isn't acceptable in a standard. How much lower, how close should the frequency points be? How many attempts must the tester try before he can fail a bad part?  
 Also, lowering the CRU corner frequency is not needed if PRBS9Q is used, because PRBS9Q is 16 times shorter than PRBS13Q.  
*SuggestedRemedy*  
 Change  
 The corner frequency of the clock recovery unit (CRU) may be set lower than 4 MHz. to  
 If the test pattern is PRBS13Q, the corner frequency of the clock recovery unit (CRU) is set to 4 MHz as in 120D.3.1.8.2, or 1 MHz.  
 Add informative NOTE saying that the measured even-odd jitter is expected to be the same or lower with 1 MHz than with 4 MHz.  
 Proposed Response Response Status **O**

Cl 162 SC 162.9.3.4 P 170 L 52 # I-174  
 Dawe, Piers J G NVIDIA  
 Comment Type **T** Comment Status **X**  
 This says "NOTE—If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter may not be correctly observed." If the measurement sees the wrong EOJ, the reported J3u and Jrms will be off, too.  
*SuggestedRemedy*  
 Delete "even-odd"  
 Proposed Response Response Status **O**

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162 SC 162.9.3.4 P 170 L 52 # I-175  
 Dawe, Piers J G NVIDIA  
 Comment Type E Comment Status X  
 "may not be" is troublesome. As "The word may is used to indicate a course of action permissible within the limits of the standard (may equals is permitted to)", "may not" means is not permitted to.  
 SuggestedRemedy  
 Change "may not be correctly observed" to "might be incorrectly observed".  
 Proposed Response Response Status O

Cl 162 SC 162.9.3.5 P 172 L 13 # I-176  
 Dawe, Piers J G NVIDIA  
 Comment Type T Comment Status X  
 ERL needs a parameter Delta f for the S-parameter measurement. I don't see that it is defined for ERL nor incorporated by reference from COM.  
 SuggestedRemedy  
 Add a Delta f entry to all the ERL tables. I suppose the value can be the usual 10 MHz, although for small test fixtures, a larger value might work too.  
 Proposed Response Response Status O

Cl 162 SC 162.9.3.5 P 172 L 19 # I-177  
 Dawe, Piers J G NVIDIA  
 Comment Type T Comment Status X  
 I wouldn't call this switch or option, a flag with a numerical value. I think it is a parameter, as in functional specifications, and as it is called in 93A.5.1.  
 SuggestedRemedy  
 Change flag to parameter, here and in tables 162-18 and 163-6, 163-7, 163-12 and 93A-4. Here and in tables 162-18 and 163-6, 163-7 and 163-12, change 1 to true.  
 Proposed Response Response Status O

Cl 162 SC 162.9.3.6 P 172 L 27 # I-178  
 Dawe, Piers J G NVIDIA  
 Comment Type TR Comment Status X  
 As for the mated test fixtures and the cable, this common mode return loss spec RLcc becomes useless at the frequency when the MCB loss is 2/2 dB, which is only 10 GHz. The spec should trend down with the MCB trace loss at 0.1 dB/GHz.  
 SuggestedRemedy  
 Use a frequency-dependent mask  $2 \text{ dB } 0.2 \leq f \leq 4$ ,  $1.6+0.1*f \text{ dB } 4 < f \leq 30$ ,  $8.5-0.13f$   $30 < f \leq 40$ . f is in GHz. See another comment for cable RLcc, 162.11.6.  
 Proposed Response Response Status O

Cl 162 SC 162.9.4.3.4 P 178 L 11 # I-179  
 Dawe, Piers J G NVIDIA  
 Comment Type E Comment Status X  
 Please help the reader understand the relation between the normalized NSD limits and Hhp  
 SuggestedRemedy  
 Please add the plot of Hhp, squared and normalized, to Figure 162-5, NSD(f) constraints. See example in attached file.  
 Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162 SC 162.11 P 181 L 31 # I-180

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The poor max cable loss makes CR unattractive, while all NICs and some ports on any switch have host loss budget going to waste. Enabling longer cables on a minority of links is needed.

In the remedy, each host knows the other host's loss class through the training protocol and the cable's loss class from its I2C compliance code, so no extra management features needed in the spec for the long cable class.

SuggestedRemedy

2 classes of cable, which could be called "short" (19.75 dB, as today) and "long",  $19.75+2*(6.875-3.75) - 0.5 = 19.75+6.25 - 0.5 = 25.5$  dB max (achievable cable length 3 m). Long cables connect port types C (see another comment) at both ends, short cables connect a valid combination of A, B, C.

In 162.11.2, cable assembly insertion loss, change text "less than or equal to 19.75 dB" to refer to Table 162-17 instead.

In 162.11.7.1.1, add zp = 30.7 mm for the "short" cable.

In Table 162A-1, add a column for the A-short-A scenario (ILCamax is 25.5 dB).

Illustrate in figures 162A-3 and 162A-4.

Proposed Response Response Status O

Cl 162 SC 162.11.6 P 185 L 28 # I-181

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

We need a common mode return loss spec RLcc to stop large common-mode voltages building up through multiple low-loss reflections. As we know, this common mode return loss spec RLcc becomes useless at the frequency when the MCB loss is 1.8/2 dB, which is only 8.5 GHz. The impedance the cable presents is mostly related to the connector, so it's much like the mated test fixtures' RLcc, except at the very lowest frequencies where the cable loss is very small and both connectors can be seen by the measurement. This proposal allows for that.

SuggestedRemedy

Use a frequency-dependent mask  $1.2 \text{ dB } 0.05 \leq f \leq 4$ ,  $0.76+0.11*f \text{ dB } 4 < f \leq 30$  GHz. f is in GHz. See another comment for Tx, Table 162-11, 162.9.3.6.

Proposed Response Response Status O

Cl 162 SC 162.11.7 P 187 L 3 # I-182

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

Empty cells

SuggestedRemedy

If unitless, use a long dash

Proposed Response Response Status O

Cl 162 SC 162.11.7 P 187 L 31 # I-183

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

Cable channels' reference receiver tap weights are less -ve than -0.02, and taps 13 to 40 are less than +0.025. The tap weight limits are not hard cable or channel limits, but they let cables that go outside the envelope pay a price in COM for it (see dawes\_3ck\_01a\_0921).

The normalized DFE coefficient minimum limit bbmin for taps 3 to 12 is -0.03 and for taps 13 to 40 it is -0.05 (bgmax 0.05) but the receiver is protected from bad taps 25-40 by the tail RSS limit. But the receiver is not protected so well for taps 13 to 24.

We can expect cable channels to be better for reflections than backplane channels because hosts must be designed for maximum-loss performance, and cable technology will also be adequate for maximum-loss performance. As a cable can have worse tap weights than the headline numbers for a very small COM penalty (see dawes\_3ck\_01a\_0921 slide 5), this remedy leaves margin for the cable.

SuggestedRemedy

For CR, in Table 162-19, change Normalized coefficient magnitude limit for DFE floating taps, bgmax, from 0.05 to 0.03.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

CI 120G SC 120G.3.1 P 258 L 19 # I-184

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

Eye height measurements are inaccurate, receivers can cope with much smaller eye height than this as they do for CR; VEC is much more important. C2M drivers are traditionally 900/1200 as strong as CR/KR drivers, and receiver noise is already in the measurement, and . So a small EH is acceptable.

SuggestedRemedy

Reduce the eye height by 2 dB, from 10 mV to 8 mV.

Proposed Response Response Status O

CI 120G SC 120G.3.1.1 P 258 L 39 # I-185

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The output common-mode to differential-mode return loss specs are the same as the input differential-mode to common-mode return loss specs, and are scaled versions of the ones in Annex 83E (which uses PAM2 not PAM4, so less demanding for signal integrity). While CEI-28G-VSR, CEI-56G-VSR-PAM4 and draft CEI-112G-VSR-PAM4 also have limits for inputs that are also 22 dB at low frequency, for outputs it's 25 dB at low frequency. This was done for good reason. 120E followed 83E rather than OIF. As we struggle with poor VEC and eye width and common-mode specification methodology, we should not be adopting weak mixed-mode specs without knowing a good reason. Also, the OIF specs are 15 dB at Nyquist; the ck draft has 12 following 83E and 120E, and we should consider if the specs should be tightened by 2 dB at Nyquist because each compliance board loss is about 1 dB higher at Nyquist than in 83E and 120E.

SuggestedRemedy

In Equation 120G-1, change 22 -20f/fb to 25 -26f/fb.  
If correcting for increased compliance board loss, change Equation 120G-1 from 22 -20f/fb, 15 -6f/fb to 25 -22f/fb, 19 -10f/fb,  
change Equation 120G-2 from 22 -20f/fb, 15 -6f/fb to 22 -16f/fb, 19 -10f/fb,

Proposed Response Response Status O

CI 120G SC 120G.3.1.1 P 258 L 41 # I-186

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

ERL has the high frequencies attenuated by the Tukey window function, 93A.5.1 says "See 93A.1.1 for scattering parameters measurement recommendations including frequency step, start frequency, and stop frequency", and 93A.1.1 says "It is recommended that the scattering parameters be measured with uniform frequency step no larger than Delta f from a start frequency no larger than fmin to a stop frequency of at least the signaling rate fb". But the test fixtures are defined to 50 GHz.

SuggestedRemedy

In 120G, make the frequency range consistent for ERL and mixed-mode return loss specs for product, and make the test fixtures' fmax no lower than that. For example, in equations 120G-1 and 2, change f <= 53.125 to f <= 50, and define ERL up to 50 GHz.

Proposed Response Response Status O

CI 120G SC 120G.3.2 P 261 L 11 # I-187

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

On one hand: the eye height measurement method is very inaccurate, host receivers that implement CR can cope with much smaller eye height than this, VEC is much more important. Receiver noise is already in the measurement, C2M drivers are traditionally 900/1200 as strong as CR/KR drivers, and the end-to-end loss is lower by a much larger ratio. So a small EH is acceptable.  
On the other hand: if the eye height limit is the same at near end as at far end, there is huge margin at near end and the implementer can optimise beyond far end, only limited by the NE VEC spec, while we want modules to be set up consistently, for the full range from near to far. NE and FE EH naturally differ, and the spec should reflect that. Also, host designers know their own loss and low-loss hosts (NICs) can take advantage of a naturally larger signal that cost the module nothing. This applies to both the short and long modes.

SuggestedRemedy

Change the far end eye height so that it is 2 dB below near end: if near can remain at 15 mV, far becomes 12 mV. Far end remains the one with less margin, that the implementer should tune the module for.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl **120G** SC **120G.3.2** P **261** L **11** # **I-188**

Dawe, Piers J G

NVIDIA

Comment Type **TR** Comment Status **X**

The module output eye height and VEC have to comply at both near end and far end, and depending on the cleanliness of its signal, a module can be tuned to either end or somewhere in the middle, or even somewhere outside the range. The host stressed input signal is tuned to far end, only, so the host isn't required to receive those other tuning choices. This is inconsistent and a serious flaw in the spec. Yet we would rather not have multiple host stress tests, nor require the host to receive unnecessary and sub-optimal signal tunings, so we need to make sure that modules are tuned correctly.

*SuggestedRemedy*

Tighten the equaliser limits for module output so that modules are tuned consistently across the industry. Because the channel losses in short and long mode testing are significantly different, in Table 20G-11 use separate gDC limits for short and long mode (see other comments). To discourage module implementers from mis-tuning modules so they are optimised significantly beyond the far end, in Table 120G-3, ensure that each near end VEC is 0.5 dB less (better) than its corresponding far end VEC, and the far end EHs are 2 dB less than the corresponding near end EHs. Note other comments that address what these values should be.

Proposed Response Response Status

Cl **120G** SC **120G.3.2.2.1** P **263** L **14** # **I-189**

Dawe, Piers J G

NVIDIA

Comment Type **TR** Comment Status **X**

If we include an allowance for host transmitter package loss for the host stressed input test, it would make sense to include the same allowance for far-end module output specs. As the change is to the reference host channel which is in software, it's convenient to do, rather than rely on extrapolation.

*SuggestedRemedy*

Increase the two far-end lengths by 2.2 dB (taking 16 dB to 18.2 dB, aligning with 120G.3.4.3.2). In Table 120G-11, increase bbmax(1) from 0.4 to 0.55. Reduce module output eye height by 2.2 dB.

Proposed Response Response Status

Cl **120G** SC **120G.3.3.3** P **265** L **3** # **I-190**

Dawe, Piers J G

NVIDIA

Comment Type **E** Comment Status **X**

Please make it easier for the reader to see how these limits relate to each other, as OIF does.

*SuggestedRemedy*

Please put the input RLcd limit on Figure 120G-5, refer to it from the sentence above, and delete this Figure 120G-8.

Proposed Response Response Status

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162 SC 162.9.4.3 P 265 L 31 # I-191

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

Improving the wording, bearing in mind that 802.3 is not a test spec nor does it mandate how compliance is achieved. At present, the introductory sentence gives the opposite impression because it says something "is measured". Other parameter definition/explanation/detail subclauses that aren't receiver interference tolerance, jitter tolerance or stressed input tolerance don't do this.

Improving consistency.

It seems that any of these would work but there may be a reason for choosing one that I have not seen yet:

- measurement procedure
- measurement method
- procedure
- method

*SuggestedRemedy*

Use a format similar to 162.9.3.3, Output SNDR. "The transmitter SNDR is defined by the measurement method..."

Here and in 162.9.4.4.1, change "Receiver interference tolerance is measured according to the procedure..." to "Receiver interference tolerance is defined by the measurement { procedure | method }..."

Similarly in 163 and 120F.

In 120G.3.3.5, Host stressed input tolerance, change

Host stressed input tolerance is measured according to the procedure...

to

Host stressed input tolerance is defined by the measurement { procedure | method }...

And similarly in 120G.3.4.3, Module stressed input tolerance.

For consistency, in 162.9.3.5, Transmitter effective return loss (ERL), "ERL of the transmitter at TP2 is computed using the procedure...", change "is computed using" to "is defined by" (there's more to it than calculation, an S-parameter measurement is needed too, as mentioned in 93A.5.1).

After we have said that a section is a definition rather than a requirement to test, it's OK to describe the procedure as a test as we do, so no further change is needed for this.

Proposed Response Response Status

Cl 120G SC 120G.3.3.5.1 P 265 L 50 # I-192

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

For module output, the optimum setting for the \*first\* precursor is 0.02 to 0.04, and the optimum for the \*second\* precursor is much smaller, so very weak. It would be better to make stressed signals (and real signals) consistent across the industry and simplify the tuning challenge for real modules than to try to squeeze out the last drop of tuning. We don't use smaller than 0.02 steps in COM.

The same point applies to module stressed input signal generator, but 120G.3.4.3.1 refers back to here.

*SuggestedRemedy*

For the host stressed input signal generator functional model, set the third precursor to zero. Modify "The tap coefficients are not specified with the exception that".

Proposed Response Response Status

Cl 120G SC 120G.3.3.5.1 P 265 L 50 # I-193

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

For module output, the optimum for postcursor with a module package and channel is zero. We want consistent stressed signals across the industry so we should give guidance where we can.

The same point applies to module stressed input signal generator, but 120G.3.4.3.1 refers back to here.

*SuggestedRemedy*

Say that in practice, a postcursor may be used to make the PG output like that from a module with zero postcursor. Modify "The tap coefficients are not specified with the exception that".

Proposed Response Response Status

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 120G SC 120G.3.3.5.1 P 266 L 15 # I-194

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The host stressed input signal is emulating a module so obviously it must obey the same rules. VEC and eye height must be in spec for both near end and far end. Ensuring this is part of the calibration process. See comment against page 267, line 25.

*SuggestedRemedy*

Change "short or long mode far-end test" to "short or long mode far-end calibration or long mode near-end verification"

Proposed Response Response Status O

Cl 120G SC 120G.3.3.5.2 P 267 L 15 # I-195

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The counter-propagating crosstalk signal amplitude for calibrating the host stressed input signal (which emulates a module) should be calibrated with PRBS13Q. CEI 16.3.10.3.1 is quite clear about this: "The crosstalk signal is calibrated at TP4 or TP1a using a QPRBS13-CEI pattern, then the pattern is changed to QPRBS31-CEI for the test". Here, the value of 750 mV in Table 120G-8 is the same as in Table 120G-1, Host output, which is defined for PRBS13Q (see 120G.5.1 and 120E.3.1.2). As these crosstalk signals are emulating the host, they must match. Also, it is convenient to set up both the peak-to-peak voltage and the transition time of a signal on the same pattern, and PRBS13Q allows both a transition time measurement and a cleaner peak-to-peak voltage measurement.

*SuggestedRemedy*

Move a few words:

The crosstalk signal transition time is calibrated with a PRBS13Q pattern. The crosstalk pattern is changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for crosstalk amplitude calibration and stressed signal calibration (see step g).

to:

The crosstalk signal transition time and amplitude are calibrated with a PRBS13Q pattern. [Or, The crosstalk signals are calibrated with a PRBS13Q pattern.] The crosstalk pattern is changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for stressed signal calibration (see step g).

Similarly in 120G.3.4.3.2 for module stressed input crosstalk signal calibration.

Proposed Response Response Status O

Cl 120G SC 120G.3.3.5.2 P 267 L 20 # I-196

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

It may not be feasible to obtain a pattern generator signal with the right rise time (transition time with "no equalization"), or perfect compliance boards, but that's OK if the loss board is tweaked to allow for this.

*SuggestedRemedy*

Add text: The reference host channel may be adjusted so that combination of the pattern generator output transition time (see step a), the HCB and the reference host channel has the effect of the ideal setup described here.

There is another comment for 120G.3.4.3.2.

Proposed Response Response Status O

Cl 120G SC 120G.3.3.5.2 P 267 L 21 # I-197

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The host stressed input signal is emulating a module so obviously it must obey the same rules. VEC and eye height must be in spec for both near end and far end. Ensuring this is part of the calibration process. See comment against line 25. This says "parameters in Table 120G-5 for far-end host channel type and the requested mode": but in one case, the near end needs a parameter from the table.

*SuggestedRemedy*

Change "for far-end host channel type and the requested mode" to "for host channel type and the requested module output mode".

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 120G SC 120G.3.3.5.2 P 267 L 25 # I-198

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The signal needs to be verified with the near end channel so that its eye height is at least the target and its VEC is no more than VEC (max) in the table. If it fails at NE, the signal must be adjusted to bring it into compliance. Also, the stressed input signal needs to obey the rules for differential peak-to-peak output voltage.

*SuggestedRemedy*

Change

... adjusted to minimize VEC, so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G-8.

to

... adjusted to minimize far-end VEC, so that the far-end eye height of the smallest eye matches the target value, far-end VEC is within the limits in Table 120G-8, and differential peak-to-peak output voltage, near-end VEC and eye height are within the limits in Table 120G-3.

Also (see other comments),

Include separate near-end and far-end VEC limits in Table 120G-8. As there will be more than one eye height limit for module output, there will be multiple EH targets here: it may be simpler to refer to Table 120G-3, Module output characteristics at TP4, rather than list them all again here.

Proposed Response

Response Status

Cl 120G SC 120G.3.3.5.3 P 268 L 10 # I-199

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

There's a problem with identifying which lanes are relevant. For example, if a host has QSFP-DD ports, there are 8 host lanes (per physical port), but there may be just 1, 2 or 4 lanes in each AUI. "The host electrical output is enabled on all lanes with any of the patterns above" is fine, it includes all the neighbours. While for "The host BER is the average of the BER of each of its lanes", only the lanes in the PMA (AUI) under test are relevant. "Module BER" in 120G.3.4.2.3 is even more open to misinterpretation because we are so clear how many lanes a module has. But, terminology for this has been set up: the term "interface BER" is used 19 times in the base document, and is defined in 86.8.2.1, 86.8.4.7, 86.8.4.8, 95.8.1.1 and 86A.5.3.8.1. 86A is an electrical spec. "host BER" and "module BER" are used just once each.

*SuggestedRemedy*

Change paragraph to:

The relevant BER is the interface BER, which is the average of the BER of each of the lanes in the AUI under test.

If the test is performed with PRBS31Q, the BER of a PMA lane may be calculated using the bit error counter in the PMA test pattern checker (see 120.5.11.2.2) as the number of bit errors divided by the number of received bits.

If the test is performed with scrambled idle or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, the interface BER may be calculated using the host FEC decoder error counters (see 91.6 and 119.3.1), as the number of FEC symbol errors divided by the number of received bits.

Similarly in 120G.3.4.2.3.

Proposed Response

Response Status

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

CI 120G SC 120G.3.4.3.2 P 271 L 4 # I-200

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

120G.3.3.5.2 says that "The pattern generator is set to generate a PRBS13Q pattern (see 120.5.11.2.1). The transition time (see 120G.3.1.4) measured at TP4a with the pattern generator output equalization configured for "no equalization" is as specified in Table 120G-8." This says "The pattern generator is set to generate a PRBS13Q pattern (see 120.5.11.2.1) with transition time (see 120G.3.1.4) at the output of the pattern generator as specified in Table 120G-10."

The point about neutral emphasis (so it's really rise time not transition time) applies to both. D2.2 comment 133. (The terminology problem is in the base document: generally, the parameter Tr is not a "transition time" as defined, but can be called a rise time.)

SuggestedRemedy

Change

"(see 120.5.11.2.1) with transition time (see 120G.3.1.4) at the output of the pattern generator as specified in Table 120G-10." to

"(see 120.5.11.2.1). The transition time (see 120G.3.1.4) measured at the output of the pattern generator, with the pattern generator output equalization configured for "no equalization", is as specified in Table 120G-10."

Proposed Response Response Status O

CI 120G SC 120G.3.4.3.2 P 271 L 25 # I-201

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

This formula imposes a delay spec on the frequency-dependent attenuator, which is unnecessary because it and the pattern generator are supposed to have good return loss, and typically there will be coax cables of unspecified length between them (which contribute a small part of the loss). The shape of the loss curve imposes the phase response we want.

SuggestedRemedy

Make it clear that extra or reduced delay is acceptable. One way would be to add "with an additional implementation-dependent frequency-independent delay". Or, change "such that the scattering parameters approximate" to "such that the magnitude of the scattering parameters approximate".

Proposed Response Response Status O

CI 120G SC 120G.3.4.3.2 P 271 L 25 # I-202

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The mated compliance boards should approximate Eq 162B-5, and the frequency-dependent attenuator should look like a clean PCB transmission line. The two in series will NOT look like another clean transmission line with no f^2 term because if that were attempted, the loss curve of the frequency-dependent attenuator would have to bend the wrong way. This is unrealistic and impractical. Also, L of 464 mm is wrong. See daw\_3ck\_01a\_1121.pdf

Further, Eq 162B-5 doesn't look like real mated compliance boards; see kocsis\_3ck\_01\_0719, slide 4, and another comment. See new presentation

SuggestedRemedy

Revise text and equation 120G-3 to make this clear. Show all three curves (Eq 162B-5 mated compliance boards, frequency-dependent attenuator and the combination) in Figure 120G-11.

Change its title from "Module stressed input target high-loss frequency-dependent attenuator differential-mode to differential-mode insertion loss" to "Module stressed input target differential-mode to differential-mode insertion losses"

Change L from 464 to 295.6 mm;

Replace Eq 120G-3 with two equations:

frequency-dependent attenuator  $0.981\sqrt{f} + 0.2463f$ ;

The combination is  $1.7962\sqrt{f} + 0.2463f + 0.003405f^2$ .

Proposed Response Response Status O

CI 120G SC 120G.3.4.3.2 P 271 L 30 # I-203

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

It may not be feasible to obtain a pattern generator signal with the right rise time (transition time with "no equalization"), or perfect compliance boards, but that's OK if the loss board is tweaked to allow for this.

SuggestedRemedy

Add text: The combination of the pattern generator output transition time (see step a) and the implementations of the frequency-dependent attenuator and the MCB, may be chosen together so that the combination has the effect of the ideal parts described here.

There is another comment for 120G.3.3.5.2.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 120G SC 120G.3.4.3.2 P 271 L 33 # I-204

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

We have a gDC + gDC2 max limit for the high loss module stressed input case to ensure that the module can equalise a very slow signal. Likewise, there should be max/min limits for gDC + gDC2 for the low loss case to set the contract for faster signals. In Table 120G-11, gDC+gDC2 can be -2 for TP1a and -1 for TP4 near-end. dudek\_3ck\_01\_0921 slide 5 indicates that a range of -3 to -1 dB would be suitable.

*SuggestedRemedy*

Add an exception that for the low-loss case, the reference receiver CTLE setting that minimizes VEC has gDC + gDC2 in the range -3 dB to -1 dB.  
It may be preferable to put the exceptions for both low- and high-loss cases in Table 120G-10.

Proposed Response Response Status

Cl 120G SC 120G.4.1 P 273 L 44 # I-205

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

This sentence that was deleted at D2.1/D2.2 "For correct operation, the actual differential-mode to differential-mode insertion loss could be higher or lower than that given by Equation (120G-4) due to the channel ILD, return loss, and crosstalk" is a necessary part of the story. It tells the host implementer that correct operation is his responsibility, and he needs to put more thought into it than simply meeting a recommended loss curve, and tells the module implementer that he has to cope with compliant hosts whose channels don't meet this recommendation. Without it, different readers can interpret "is expected" as anything between irrelevant and required.

An informative section saying "is expected" is a problem anyway.

There are similar sentences in 120D and 120F, without "For correct operation"

*SuggestedRemedy*

Change "The channel differential-mode to differential-mode insertion loss is expected to meet Equation (120G-4)..." to "An example region of channel differential-mode to differential-mode insertion losses is given in Equation (120G-4)..."

(It's not a good singular example channel because it has a kink in it.)

Reinstate a sentence that says what the deleted sentence was trying to say - preferably one that is better understood. e.g.

"However, channels with higher insertion loss are not excluded, and lower insertion loss may be necessary to allow for factors such as channel ILD, return loss, and crosstalk."

Make 120F.4.2 consistent.

Proposed Response Response Status

Cl 120G SC 120G.5.2 P 275 L 27 # I-206

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The limits for TP4 gDC, gDC2 should not be the same for short and long output modes. The range of losses in a module is much less than the range of losses of the four reference host channels. So, obviously, different channels will need different CTLE settings. Obviously, CTLE settings that represent signals outside what the spec makes a host capable of receiving in a particular mode, should be excluded, to make module implementers set up their product correctly.

*SuggestedRemedy*

Create separate limits for TP4 short and long output modes, so 4 sets for TP4+, in the style of TP1a. See other comments.

Proposed Response Response Status

Cl 120G SC 120G.5.2 P 275 L 28 # I-207

Dawe, Piers J G

NVIDIA

Comment Type TR Comment Status X

The maximum gDC is -2 for TP1a and -1 for TP4 near-end. As the MCB loss and HCB loss are within 0.2 dB of each other, these specs are inconsistent by 0.8 dB.

dudek\_3ck\_01\_0921 slide 5 shows that -1 is reasonable for a 12 mm package trace, and shorter traces are possible, e.g. an on-board repeater. Hosts and modules with less loss than the MCB and HCB respectively may have to receive a signal less filtered at the point of use than in the module or host output measurement.

ghiasi\_3ck\_adhoc\_01a\_042121 slide 9 says that -1 is needed for 5 dB ball to ball, 1.6 dB less than the mated compliance boards' loss.

On the other hand, things go bad rapidly with too much emphasis. It would be safer to set both at -2, which would require retuning the short setting in ghiasi\_3ck\_adhoc\_01a\_042121 with reduced output emphasis - which should be OK.

See other comments that give specific ranges for the stressed signals to ensure that inputs are tested with representative low-loss signals.

*SuggestedRemedy*

For TP4 gDC, change -1 to -2.

Proposed Response Response Status

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl **120G** SC **120G.5.2** P **275** L **34** # **I-208**

Dawe, Piers J G

NVIDIA

Comment Type **TR** Comment Status **X**

The weakest (max, least -ve) gDC + gDC2 is -2 for TP1a, -2 for TP4 near end, -3 for TP4 far end and -10.5 for module stressed input high loss. There is about 10 dB loss difference between short near end and long far end, but 1 dB difference in max gDC + gDC2 which is far too little. It looks like TP4 far end (-9 to -2 in the draft) is out of step, with a much wider range than TP4 near end. TP4 LONG far end should never use this wide range as most of the channel loss is fixed. We should not be encouraging modules to try to do a job the host receiver does better, and we want modules to be set up consistently so that the short/long mode choice means something.

Also, if we include an allowance for host transmitter package loss for the host stressed input test, it would make sense to include the same allowance for far-end module output specs.

*SuggestedRemedy*

Impose a max gDC + gDC2 limit of -5 for TP4 long far end, e.g. with gDC, gDC2 ranges in the same style as TP1a:

- Range for gDC2 = 0 -9 to -5
- Range for -1 <= gDC2 < 0 -9 to -4
- Range for -2 <= gDC2 < -1 -9 to -3
- Range for -3 <= gDC2 < -2 -9 to -2

Proposed Response Response Status

Cl **120G** SC **120G.5.2** P **275** L **34** # **I-209**

Dawe, Piers J G

NVIDIA

Comment Type **TR** Comment Status **X**

As a most of the channel for TP4 far-end is known exactly and the max loss to TP4 far end is less than to TP1a, the range of gDC, gDC2 combinations should be a subset of the TP1a ones.

*SuggestedRemedy*

For continuous time filter, DC gain for TP4 short far-end (gDC), change to sets of limits that depend on gDC2 in the same style as for TP1a. The allowed values should be subsets of those for TP1a.

See another comment for TP4 long far end.

For TP4 short far end, change from -9 to -2, to:

- Range for gDC2 = 0 -7 to -3
- Range for -1 <= gDC2 < 0 -7 to -2
- Range for -2 <= gDC2 < -1 -7 to -2
- Range for -3 <= gDC2 < -2 -7 to -2

Proposed Response Response Status

Cl **120G** SC **120G.5.2** P **276** L **21** # **I-210**

Dawe, Piers J G

NVIDIA

Comment Type **T** Comment Status **X**

This says "a minimum of 3 samples per symbol, or equivalent. Collect sufficient samples equivalent to at least 1.2 million PAM4 symbols to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10<sup>-5</sup> without extrapolation."

With a uniform-weighted histogram/mask, one needs several times 1e5 samples in the 0.1 UI window to get several hits in each tail. If samples are distributed uniformly across time, and using 10 for "several" for simplicity, we need 10 \* 1e5 / 0.1 = 10 million samples. The first sentence implies that maybe several times fewer are needed, but still, 1.2 million seems too few for a reference (accurate) measurement.

If Gaussian weighting is used (which it should not be, see another comment) then one needs many more de-weighted hits to get to a false 1e-5 in the tails.

Also, giving a number is like telling the test engineer to use an instrument with a certain precision. That's not the standard's business; we say what the outcome of an accurate, possibly idealised, measurement must be, and the test engineer balances cost, time, margin, accuracy and so on. Including choosing how many samples.

*SuggestedRemedy*

Change "equivalent to at least 1.2 million PAM4 symbols" into an example, with a higher number, or delete it.

Proposed Response Response Status

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl **120G** SC **120G.5.2** P **277** L **6** # **I-211**

Dawe, Piers J G

NVIDIA

Comment Type **TR** Comment Status **X**

This draft has a (de-)weighted rectangular eye mask spec with mask height = max(EHmin, EA/VECmax) and effective mask width ~2x0.03 to 2x0.035 UI, although it is described as a histogram 2x0.05 UI wide. This is too narrow; compare 120E with ESMW of 0.2 or 0.22 UI. It's half as wide as TDECQ with histograms extending to +/-0.07 UI.

This de-weighted histogram might have worked if there had been a guarantee that no host or module would ever produce a fast, highly jittered eye, but we don't have that guarantee. Work needs to be done to repair the hole in the spec.

See healey\_3ck\_01a\_1020 slide 6, orange dots for +/-0.025 UI which is the closest to the current draft. For VEC of 10 dB, EW can be anywhere in the range 160 to 290 mUI: an almost 2:1 range. Driver risetime is not reported; if it is always the COM default slowest-reasonable 7.5 ps, then even worse EW is possible with faster or peaked drivers. This is too much worse than 120E. As the plot shows, a wide range of eye widths are possible, so we don't need to allow the worst ones by an oversight.

De-weighting the sides of the histogram with flat top and bottom, rather than chamfering the corners, means that infringing the corners by a mile is counted the same as infringing by an inch, which is bad. Most of the weight of samples is in the middle of the eye which is a waste of measurement time; we know the corners will fail first so we should measure them, not the middle. Hence the 2-offsets approach of TDEC and healey\_3ck\_01a\_1020. The effective BER criterion of the (de-)weighted mask seems to be around 1e-4, not 1e-5 as before.

The distribution of repeated measurements is very skewed.

We need an eye mask that's more eye shaped, so that a higher proportion of the samples near the boundary are measured at full weight and contribute properly to the measurement. Eye mask measurement with a 10-sided mask has been pre-programmed into scopes for about 20 years, we should use established tools and methods where they work well.

The 10-sided mask controls the eye on the diagonal more strongly than the rectangular uniform histogram/mask because hits are collected over the time of the chamfer, rather than just in corners. The de-weighted rectangular histogram controls the eye on the diagonal more weakly than the rectangular uniform histogram/mask because hits are collected just in corners, and de-weighted.

*SuggestedRemedy*

Change from a 4-cornered weighted mask with corners at  $t = ts \pm 0.05$ ,  $V = y \pm H/2$  to a 10-cornered unweighted mask with corners at  $t = ts \pm 1/16$ ,  $ts \pm 0.05$ ,  $ts \pm 3/32$ ,  $V = y \pm H/2$ ,  $y \pm H \cdot 0.4$ ,  $y$ .  $y$  is near VCmid, VCupp or VClow (vertically floating, as in D3.0).  $H$  is  $\max(EHmin, Eye Amplitude * 10^{-(VECmax/20)})$ . Eye Amplitude is AVupp, AVmid or AVlow, as today.

This simple scalable method gives VEC results 0.5 to 1 dB more optimistic than the unweighted rectangular mask. It can remain as the EH and VEC limits are revised in the light of experience.

Proposed Response Response Status **O**

Cl **120G** SC **120G.5.2** P **277** L **6** # **I-212**

Dawe, Piers J G

NVIDIA

Comment Type **TR** Comment Status **X**

The Gaussian weighting has the effect of destroying the histogram width, allowing bad fast eyes to pass, while failing less bad slow eyes. It gives the false impression that the histogram width still applies. With a weighting standard deviation of 0.02 UI, the eye height is measured at around +/-0.035 UI rather than the +/-0.05 UI with the unweighted histogram - depending on eye shape. Compare 120E with ESMW of 0.2 or 0.22 UI, and TDECQ with histograms extending twice as wide, to +/-0.07 UI. This weighting is equivalent to relaxing the VEC spec by 1.5 to 2 dB - but it depends on the eye shape, it weakens the spec most for the worst-shaped eyes, which is bad. It applies a worse BER criterion than the 1e-5 intended.

*SuggestedRemedy*

Remove the Gaussian weighting and set the eye height and VEC limits (which need revision anyway) appropriately. ghiasi\_3ck\_01\_0721, which was not given the presentation time it deserved, says that the minimum eye height in particular needs to be reduced for TP1 and TP4 far end.

Proposed Response Response Status **O**

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162A SC 162A P 284 L 9 # I-213

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

I wondered why 162.9.3 was referring to an annex whose title seemed to be nothing to do with the subject...

The title of this annex is "TP0 and TP5 test point parameters and channel characteristics ..." yet it contains recommended transmitter and receiver characteristics, which aren't mentioned in 162A.1 Overview, "This annex provides information on..." either. I don't recognise "test point parameters" as including transmitter IC recommendations.

SuggestedRemedy

Change the title from  
TP0 and TP5 test point parameters and channel characteristics for 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4

to

Transmitter, receiver and channel recommendations at test points TP0 and TP5 for 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4

Change the first sentence from

This annex provides information on parameters associated with test points TP0 and TP5 that might not be testable in an implemented system.

to

This annex provides information on transmitter, receiver and channel parameters associated with test points TP0 and TP5 that might not be testable in an implemented system.

Proposed Response Response Status O

Cl 162A SC 162A P 284 L 15 # I-214

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

"TP0 and TP5 that might not be testable": see style guide

SuggestedRemedy

TP0 and TP5, which might not be testable

Proposed Response Response Status O

Cl 162A SC 162A.4 P 285 L 1 # I-215

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

ILPCBmin

SuggestedRemedy

ILddPCBmin

Proposed Response Response Status O

Cl 162B SC 162B.2.1 P 291 L 3 # I-216

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

Please make it easier for the reader to judge the size of these losses. Also, it's test fixture reference ... loss as in the text, not reference test fixture ... loss.

SuggestedRemedy

Please put ILddcatf on Figure 162B-1, and label the two lines (e.g. make one dashed), change figure title to "reference differential-mode to differential-mode insertion losses of test fixtures", refer to it from 162B.3, delete Figure 162B-2.

Proposed Response Response Status O

Cl 162B SC 162B.2.1 P 291 L 49 # I-217

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

fixtures

SuggestedRemedy

fixture

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162B SC 162B.4.1 P 293 L 1 # I-218

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

The reference differential-mode to differential-mode insertion loss of the mated test fixture is a scaled version of Eq 120E-3 and it doesn't align well to kocsis\_3ck\_01\_0719, slide 4. This causes a problem when constructing the lossy channel for the module stressed input test (in daw\_3ck\_01a\_1121 slide 8, the green line is straighter than the black line at low frequencies).

The new equation has the same loss at Nyquist as the existing one. See new presentation.

SuggestedRemedy

Change equation 162B-5 from:

$$|L_{ddMTFref}(f) = 0.942(0.471\sqrt{f}) + 0.1194f + 0.002f^2$$

to

$$|L_{ddMTFref}(f) = 0.8153\sqrt{f} + 0.003405f^2$$

Update Figure 162B-3, Mated test fixtures differential-mode to differential-mode insertion loss

Proposed Response Response Status O

Cl 162C SC 162C.1 P 303 L 14 # I-219

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

As these aren't proper names, according to the house style they don't get capitals (except at the beginning of a sentence, cell or similar)

SuggestedRemedy

Change "Transmitter Inverted Data Input" to "Transmitter inverted data input" and so on.

Proposed Response Response Status O

Cl 163A SC 163A P 316 L 1 # I-220

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

annex Annex ... and ...

SuggestedRemedy

annexes Annex ... and ...

Proposed Response Response Status O

Cl 163A SC 163A.3.1.3 P 319 L 24 # I-221

Dawe, Piers J G

NVIDIA

Comment Type E Comment Status X

Eq 163A-5 is part of step b, and Eq 163A-4 is part of step d, is after b.

SuggestedRemedy

Swap equations 163A-5 and 4

Proposed Response Response Status O

Cl 163B SC 163B.2 P 322 L 21 # I-222

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

Complete the example

SuggestedRemedy

As this is a Clause 163 example, there's another package length  $z_p = 12$ .

Change " $z_p = 31$  mm" to " $z_p = 12$  mm or 31 mm".

Delete the sentence "Although clauses using the TP0v methodology may require the ERL reference value to be calculated at more than one package length, only one is shown here."

In table 163B-1, add a row for package  $z_p$ . Add a column for the 12 mm case. Add a row called "Candidate effective return loss" with the two entries. Straddle the entry for "Effective return loss, ERL".

Proposed Response Response Status O

Cl 163B SC 163B.2 P 322 L 31 # I-223

Dawe, Piers J G

NVIDIA

Comment Type T Comment Status X

Figure 163B-1 doesn't match Equation 163B-1.

SuggestedRemedy

I believe the graph is right, and the right coefficients are 0, 0.235616, 0.059147.

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 162 SC 162 P 166 L 6 # I-224

Zivny, Pavel Tektronix, Inc.

Comment Type T Comment Status X

The "using a test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth." allows for large range of result change depending on the end of B-T filter compliance. This can readily be corrected by specifying the roll-off, as has been done in optical standards for years - see e.g. 140.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ).

Reasoning: experiments show that for realistic signals the sensitivity (of measurement results) to roll-off compliance becomes insignificant past about 55 GHz. Presentation available.

SuggestedRemedy

Append "using a test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth" with "compliant (to the B-T response) to at least 58 GHz, and lower or the same level as the 58 GHz response thereafter".

Proposed Response Response Status O

Cl 166 SC 166.9.3.4 P 170 L 46 # I-225

Zivny, Pavel Tektronix, Inc.

Comment Type T Comment Status X

the statement "The test pattern is either PRBS13Q or alternatively PRBS9Q. PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only one pattern is sufficient" includes PRBS9Q only as a test equipment work-around. Clarify that PRBS13Q is preferred. Reasoning: allowing either of two different patterns increases compliance uncertainty. The PRBS9Q is not needed for equipment available in 2022.

SuggestedRemedy

repalce "The test pattern is either PRBS13Q or alternatively PRBS9Q. PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only one pattern is sufficient." with

"The test pattern is PRBS13Q or alternatively PRBS9Q (deprecating). PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only PRBS13Q pattern is sufficient; in cases when that fails due to do test equipment problems the PRBS9Q might be used."

Proposed Response Response Status O

Cl 30 SC 30.5.1.1.17 P 37 L 8 # I-226

Ben-Artsi, Liav Marvell Semiconductor, Inc.

Comment Type E Comment Status X

Historically speeds were stated lowest first, this 10/1Gboa-PRX should be changed to 1/10Gbase-PRX

SuggestedRemedy

change to 1/10Gbase-PRX

Proposed Response Response Status O

Cl 30 SC 30.5.1.1.18 P 37 L 22 # I-227

Ben-Artsi, Liav Marvell Semiconductor, Inc.

Comment Type E Comment Status X

Historically speeds were stated lowest first, this 10/1Gboa-PRX should be changed to 1/10Gbase-PRX

SuggestedRemedy

Change to 1/10Gbase-PRX

Proposed Response Response Status O

Cl 45 SC 45.2.1.6 P 40 L 12 # I-228

Ben-Artsi, Liav Marvell Semiconductor, Inc.

Comment Type TR Comment Status X

How 1011111 is defined? Should be reserved.

SuggestedRemedy

Add 1011111 as reserved

Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 45 SC 45.2.1.21 P 42 L 18 # I-229  
 Ben-Artsi, Liav Marvell Semiconductor, Inc.  
 Comment Type ER Comment Status X  
 "ability 1" is "1" a typo?  
 SuggestedRemedy  
 If a typo, erase  
 Proposed Response Response Status O

Cl 162 SC 162.11 P 181 L 18 # I-232  
 Ben-Artsi, Liav Marvell Semiconductor, Inc.  
 Comment Type E Comment Status X  
 The term twinaxial cabling os used in multiple places, but never defined.  
 SuggestedRemedy  
 Suggest changing twinaxial cable to "twinaxial shielded balanced copper cable", which would explain it a bit better  
 Proposed Response Response Status O

Cl 73 SC 73.6.4 P 71 L 3 # I-230  
 Ben-Artsi, Liav Marvell Semiconductor, Inc.  
 Comment Type T Comment Status X  
 What is the reason to shorten this field? I'd rather have a 24-bit field instead. More software friendly.  
 SuggestedRemedy  
 Change to 24 bit  
 Proposed Response Response Status O

Cl 121 SC 121.1 P 115 L 19 # I-233  
 Ben-Artsi, Liav Marvell Semiconductor, Inc.  
 Comment Type E Comment Status X  
 120-F and 120G have a different format than the line above - Same applies for table 122-1 on page 116  
 SuggestedRemedy  
 aline formats between the three and write: 120F-Chp-to-chip 200GAUI-2 and 120G-Chip-to-module 200GAUI-2. Fix also table 122-1  
 Proposed Response Response Status O

Cl 116 SC 116.1.2 P 95 L 24 # I-231  
 Ben-Artsi, Liav Marvell Semiconductor, Inc.  
 Comment Type E Comment Status X  
 400GBASE-SR4.2 seems to have a nomanclature very different than all others - find one which is more aligned with all others  
 SuggestedRemedy  
 Proposed Response Response Status O

Cl 124 SC 124.1 P 118 L 19 # I-234  
 Ben-Artsi, Liav Marvell Semiconductor, Inc.  
 Comment Type E Comment Status X  
 120-F and 120G have a different format than the line above  
 SuggestedRemedy  
 aline formats between the three and write: 120F-Chp-to-chip 200GAUI-2 and 120G-Chip-to-module 200GAUI-2.  
 Proposed Response Response Status O

IEEE P802.3ck D2.3 100/200/400 Gb/s Electrical Interfaces Task Force Initial Sponsor ballot comments

Cl 135 SC 135.5.7.2 P 123 L 48 # I-235  
 Ben-Artsi, Liav Marvell Semiconductor, Inc.  
 Comment Type E Comment Status X  
 Stating the GAUI lane amounts in an increasing order makes more sense  
 SuggestedRemedy  
 Replace 100GAUI-1 and 100GAUI-2 order on lines 47 and 51  
 Proposed Response Response Status O

Cl 161 SC 161.5.2.6 P 135 L 3 # I-238  
 Ben-Artsi, Liav Marvell Semiconductor, Inc.  
 Comment Type TR Comment Status X  
 In figure 161-2 it seems that this FEC does not support EEE. If such is desired recommend amending in a similar manner as Figure 91-2 in clause 91  
 SuggestedRemedy  
 Add EEE support similar to Figure 91-2 in clause 91  
 Proposed Response Response Status O

Cl 163 SC 163.9.2.6 P 206 L 42 # I-236  
 Dudek, Michael Marvell  
 Comment Type TR Comment Status X  
 The value of Np=11 is unnecessarily low for this variant where the receiver equalizer has many more taps. Note however that this section is referenced by the C2C in 120F.3.1 where the number of DFE taps is only 6.  
 SuggestedRemedy  
 Change the value of Np from 11 to 24 here. Reference Residual ISI in table 120F-1 to a new section in 120F.3.1. This section to say "Residual Intersymbol Interference is measured with the procedure in 163.9.2.6 with the exception that Np=11  
 Proposed Response Response Status O

Cl 162 SC 162.9.3 P 166 L 45 # I-237  
 Dudek, Michael Marvell  
 Comment Type TR Comment Status X  
 With the Np=200 value used for the linear fit procedure in the SNDR measurement it is possible that the transmitter can have significant pulse distortions at times beyond the reach of the receiver DFE. These pulse distortions cannot be equalized and could increase the BER unacceptably.  
 SuggestedRemedy  
 Add a Residual Intersymbol Interference specification with value -31dB max referring to the test procedure in 163.9.2.6  
 Proposed Response Response Status O