Physical Aspects of Packages for 100GEL & PKG ad-hoc Physical Aspects Summary

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Suggested PKG Model Cases

	Length	Ball Side Discontinuity	Xtalk (Suggest using random noise)	Suggested Decision & (Priority)
PHY **(WIP)**	8-12mm	Low Pitch BGA	High	A Must have for high reflections & Xtalk (1)
Typ Switch	20mm	1mm pitch BGA	Medium	Check if covered by any of the 30mm (2)
High Lane Count Switch up to 70x70mm	30mm	1mm pitch BGA	Low	Provide an initial model to check for impact (1)
High Lane Count Switch > 70x70	30mm	LGA	Low	Discuss whether should be covered. if yes… How? If not… how to manage the impact?

- Models supplied for Case 1 & 3 and dealt with until now

PKG Trace & Design Characteristics

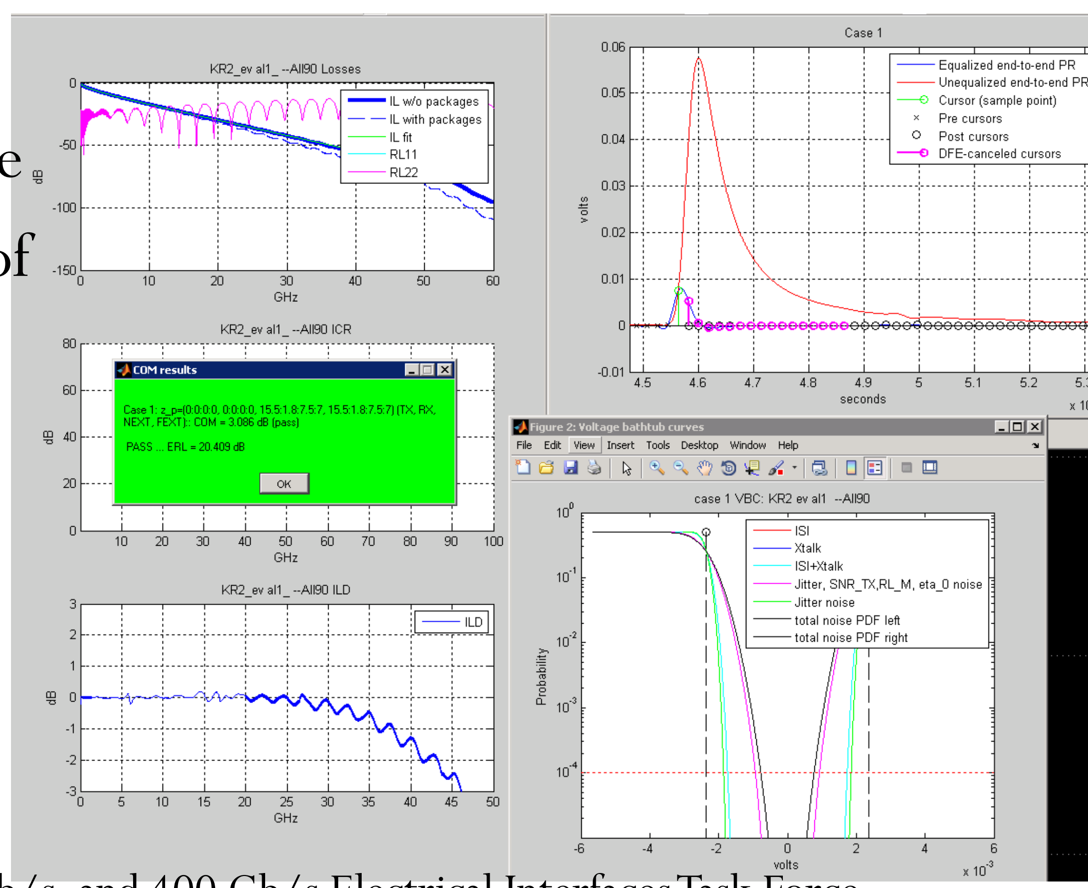
- 29 micron width for low loss
- Dielectric loss coefficient = 0.004
- Roughness processing causes R=0.1μ on the treated surface
- 90ohm nominal targeted PKG impedance
- @ long PKG traces it was assumed that dominant Xtalk can be avoided due to big package size in this case (though in some situations that may not be the case)
- Xtalk (Fext only) will be taken only in the short PKG trace case

COM Runs on Concatenated Interconnect + PKGs

- Nb=16
- Cd = 130fF / 110fF (10fF included in PKG extracted model)
- Ran with 30mm HFSS extracted PKGs on both ends
- Ball + PTH discontinuity integrated into the extracted model

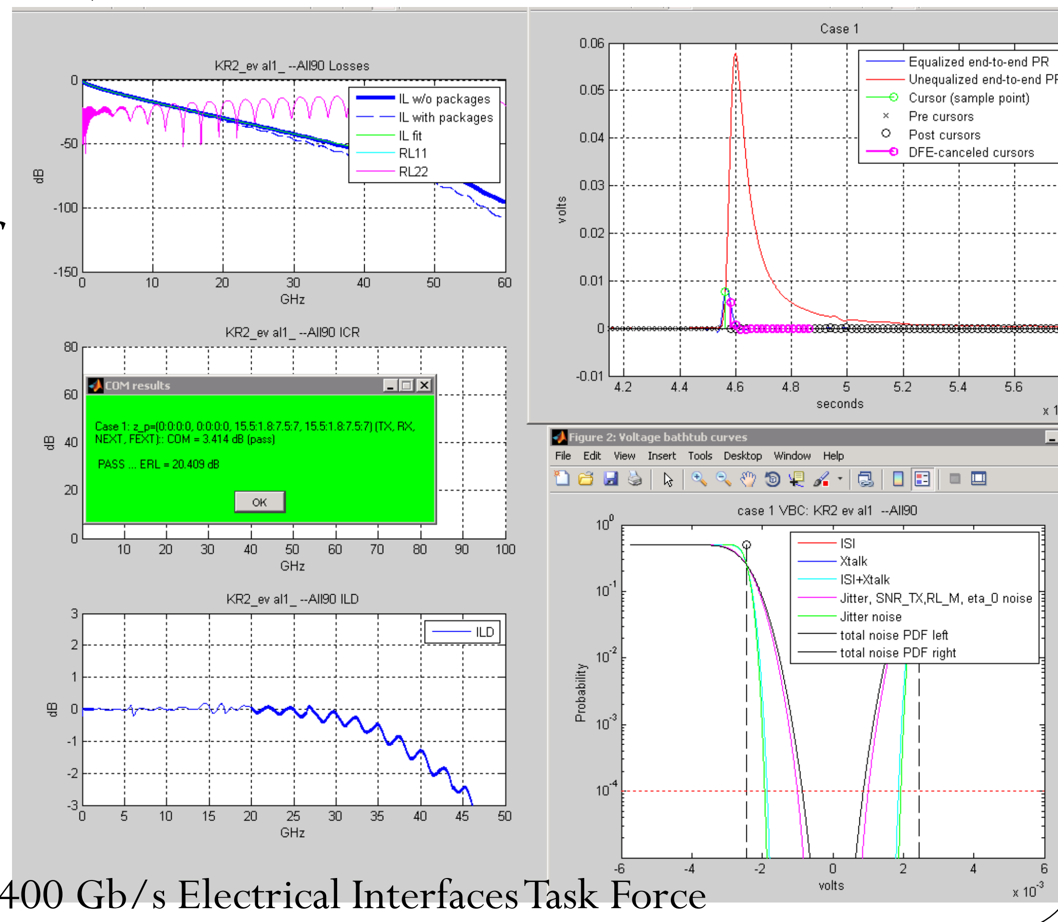
Ideal 30mm PKG

- Concatenated to 30mm packages on both sides
- ~90Ω trace
- 130fF total die capacitance
- Ball capacitance is a part of The Extracted Model
- 3.1dB COM



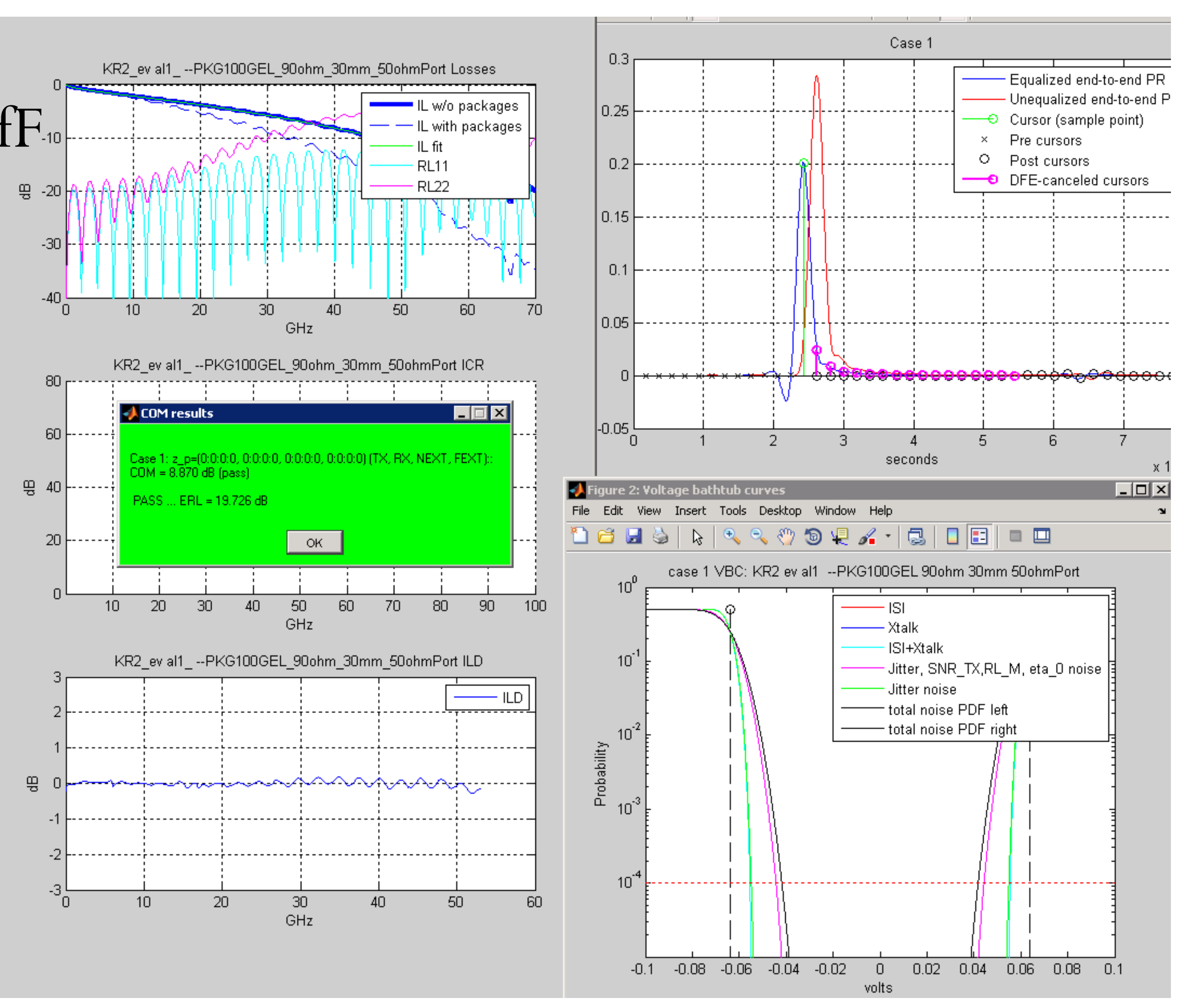
Best Design 30mm PKG

- Concatenated to 30mm packages on both sides
- ~90Ω trace (28dB@26.6GHz)
- 110fF total die capacitance (100fF-Die + 10fF-PKG)
- Ball capacitance is a part of The Extracted Model
- ~3.4dB COM



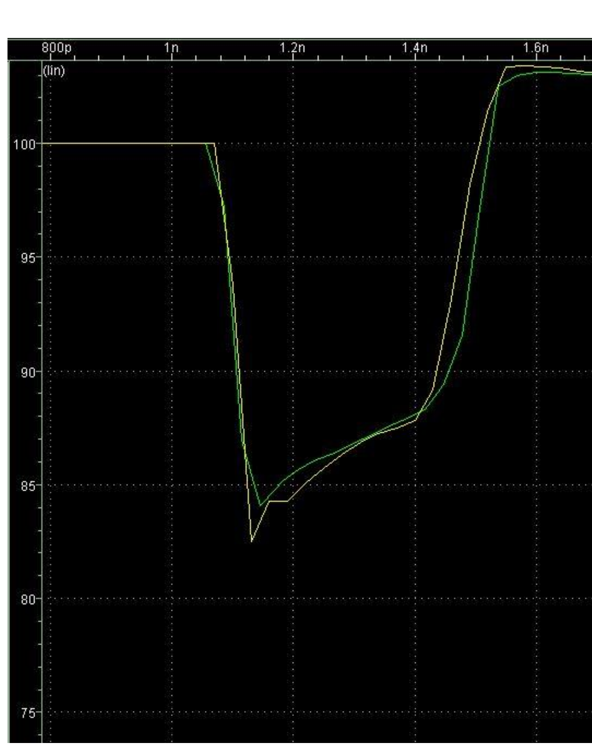
~90Ω PKG Results (Stand Alone)

- Die Side total capacitance = 110fF
- No BRD attached



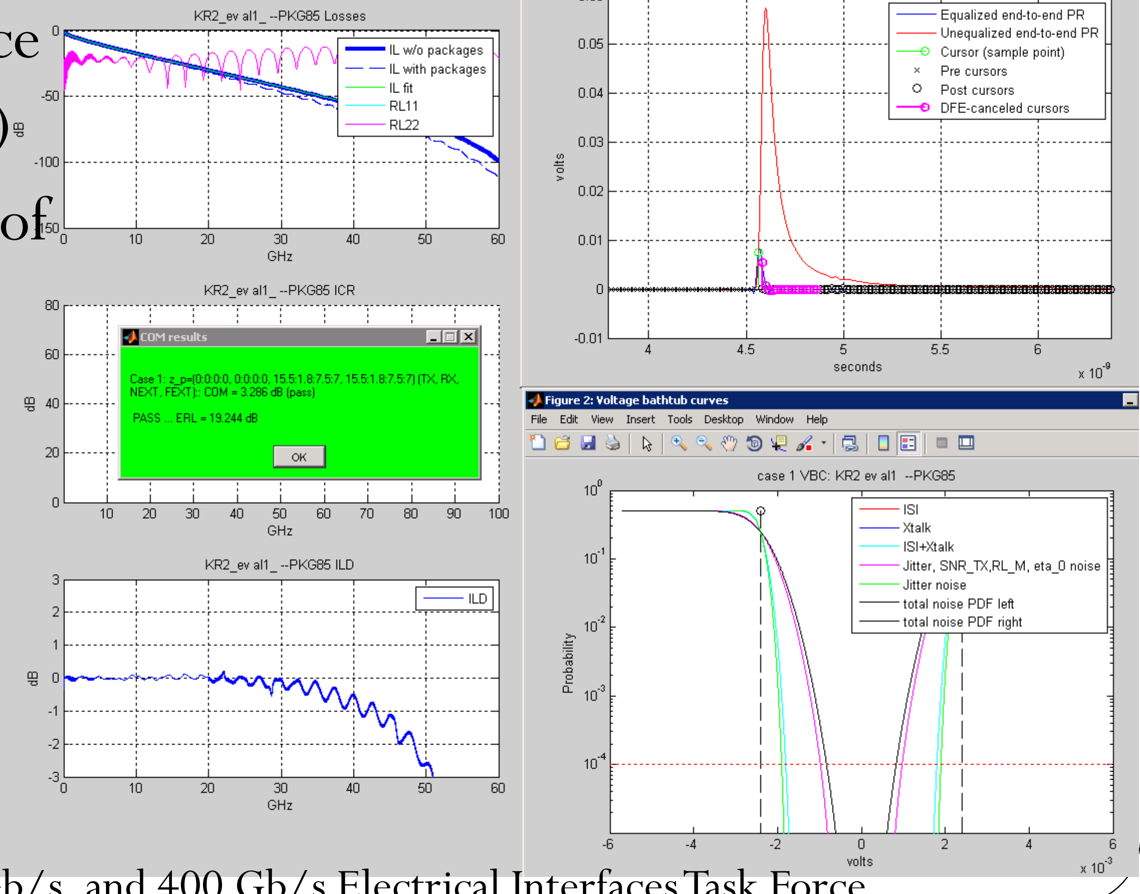
~85Ω PKG 30mm length

- Die Side total capacitance = 110fF
- No BRD Attached



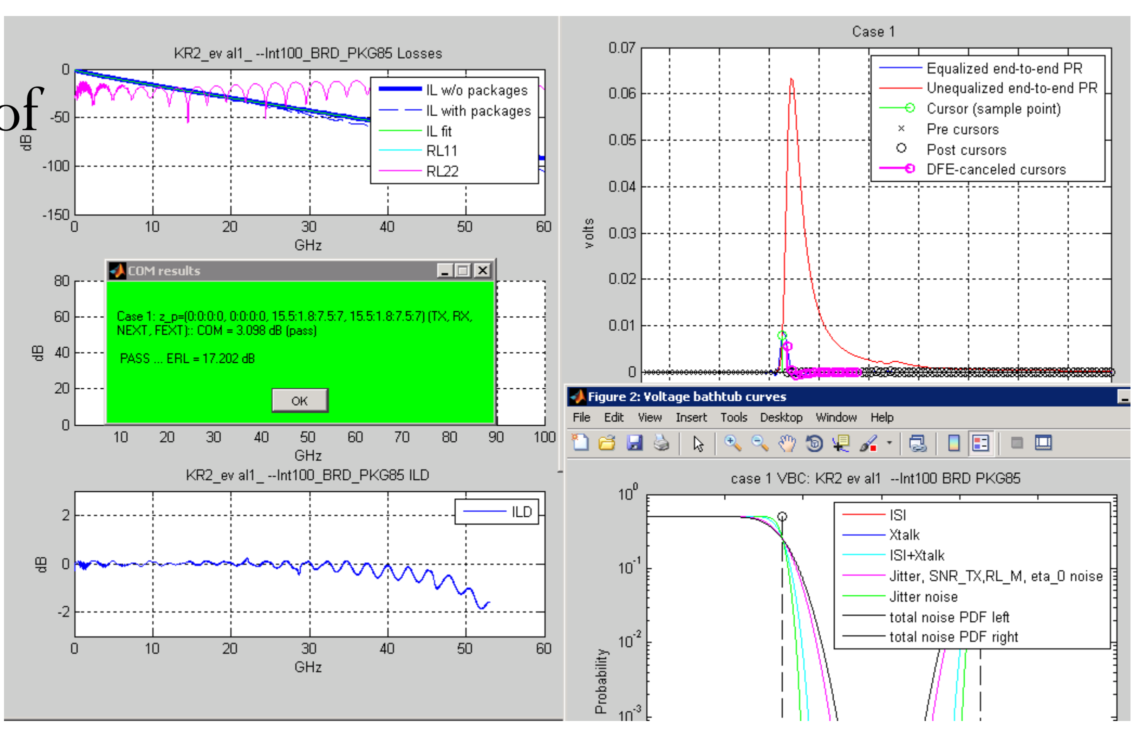
PKG85

- Concatenated to 30mm 85Ω packages on both sides
- ~90Ω trace (28dB@26.6GHz)
- 110fF total die capacitance (100fF-Die + 10fF-PKG)
- Ball capacitance is a part of The Extracted Model
- ~3.4dB COM



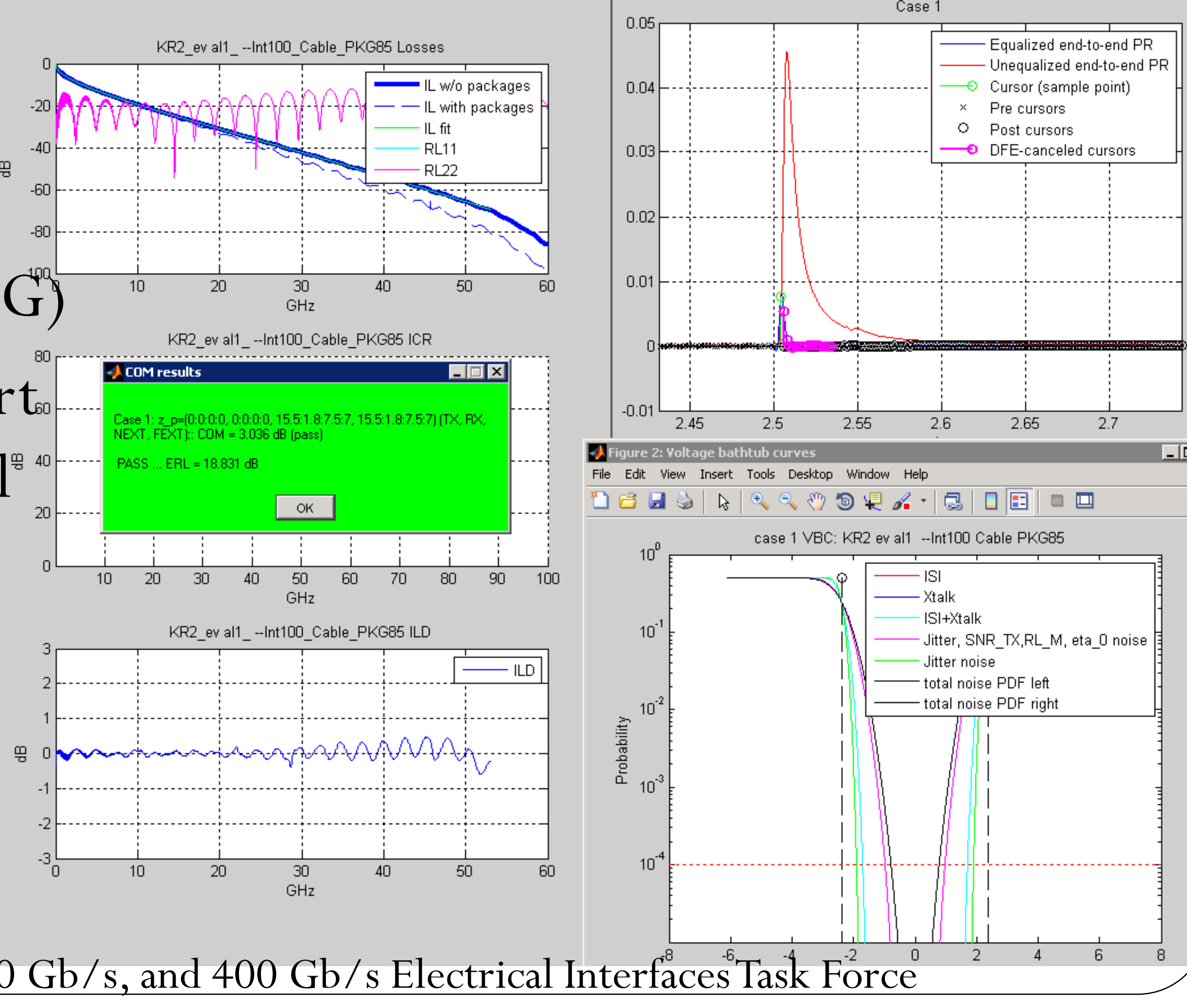
PKG85 + 100ohm MEG6 BRD

- Concatenated to 30mm 85Ω packages on both sides
- 100Ω max loss trace (MEG6 28dB@26.6GHz)
- 110fF total die capacitance (100fF-Die + 10fF-PKG)
- Ball capacitance is a part of The Extracted Model
- ~3.1dB COM



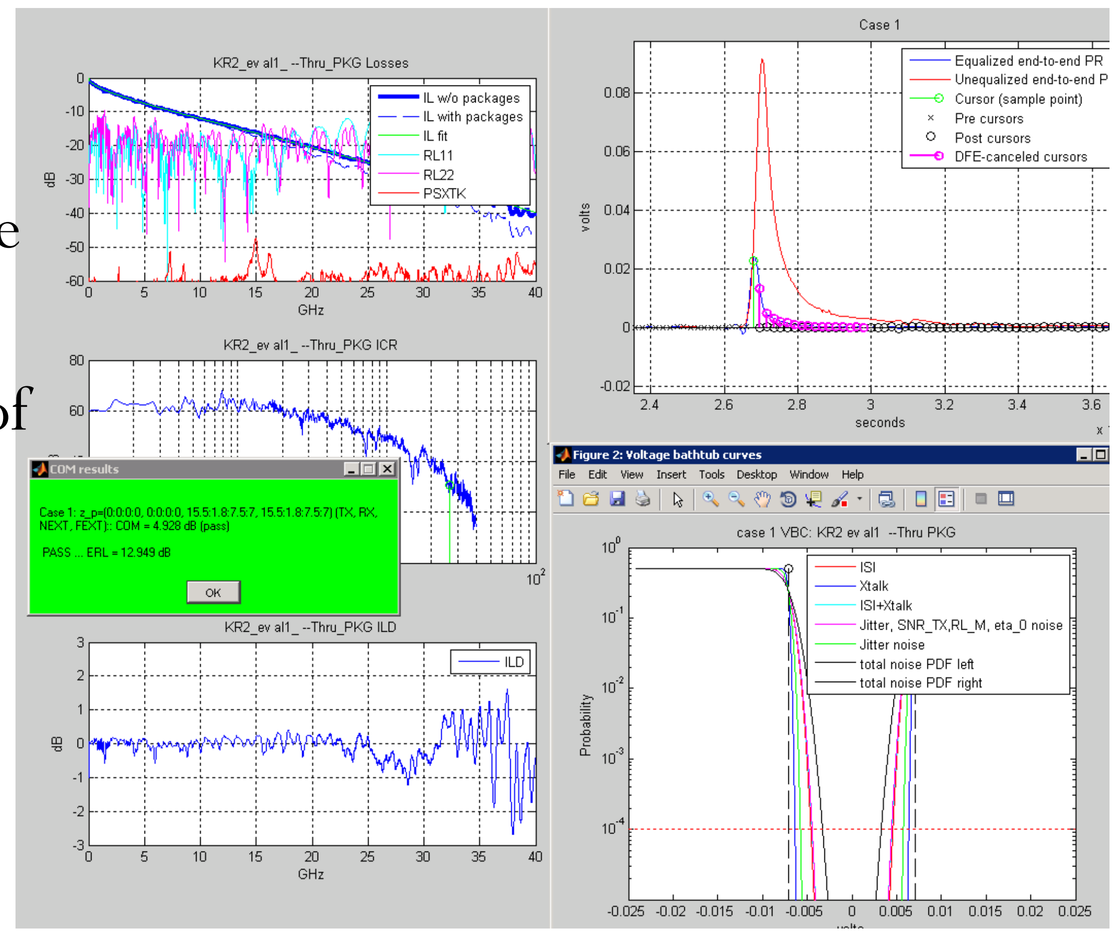
PKG85 + 100ohm Twinax Cable

- Concatenated to 30mm 85Ω packages on both sides
- 100Ω max-loss cable
- 110fF total die capacitance (100fF-Die + 10fF-PKG)
- Ball capacitance is a part of the Extracted Model
- ~3.1dB COM



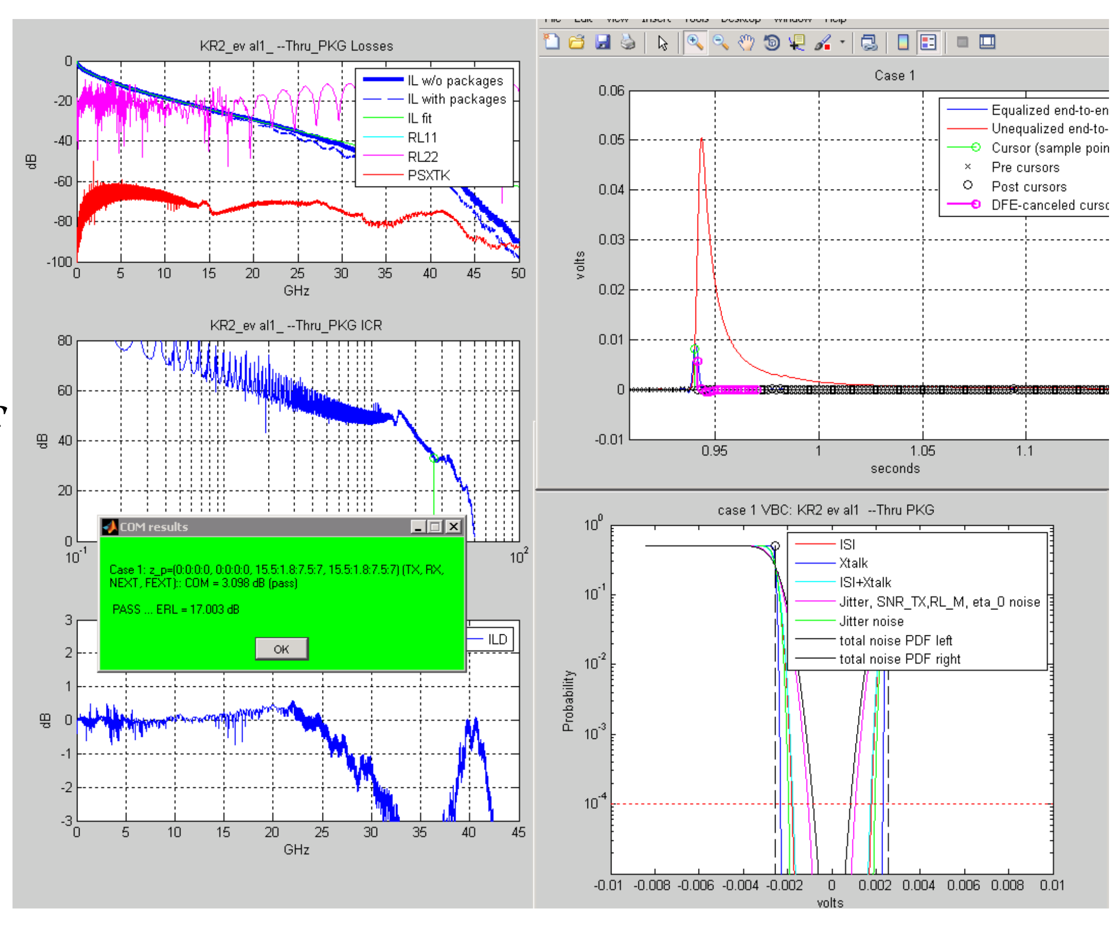
PKG85 + Lim_16dB

- Concatenated to 30mm 85Ω packages on both sides
- 16dB loss C2M channel
- 110fF total die capacitance (100fF-Die + 10fF-PKG)
- Ball capacitance is a part of The Extracted Model
- ~4.9dB COM (can therefore run with lower silicon capabilities)



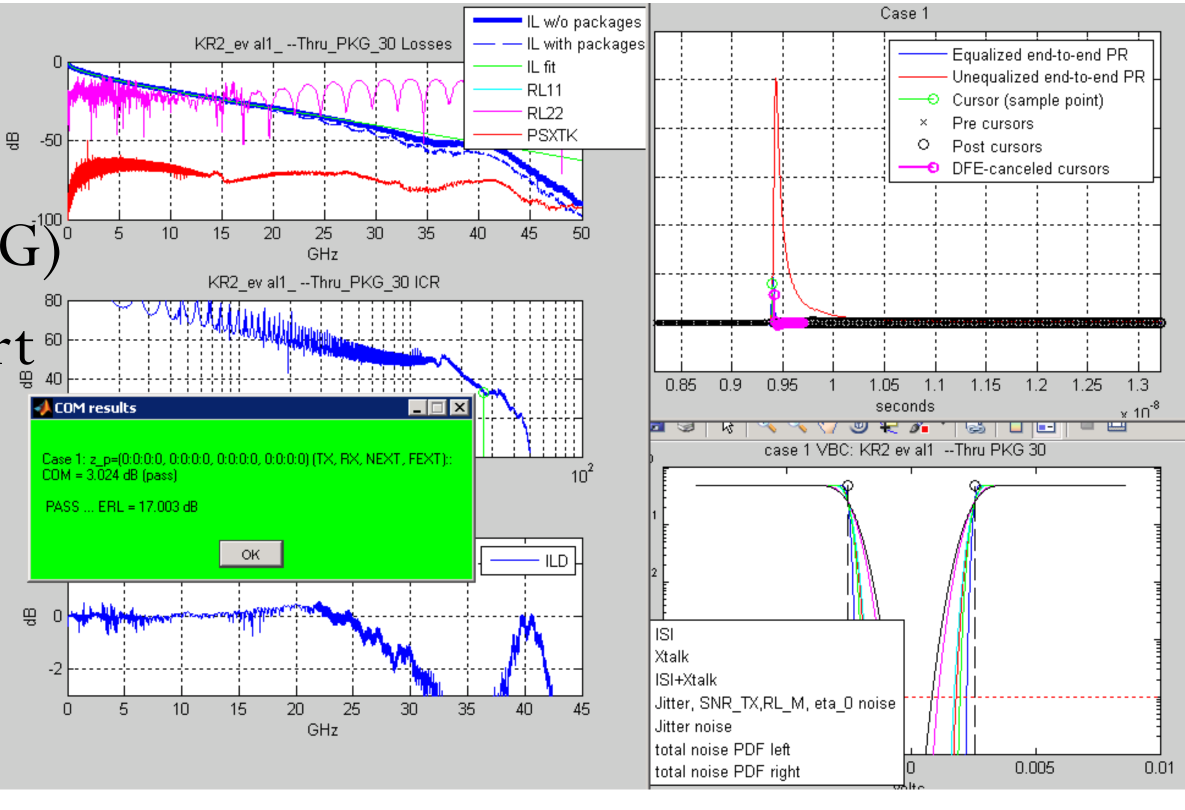
PKG85 + CaBP_BGAVia_Opt2_28dB

- Concatenated to 30mm 85Ω packages on both sides
- 100Ω max loss trace
- 110fF total die capacitance (100fF-Die + 10fF-PKG)
- Ball capacitance is a part of the extracted model
- ~3.1dB COM



PKG85 + CaBP_BGAVia_Opt2_28dB+ XTalk

- Concatenated to 30mm 85Ω packages on both sides
- Concatenated to CaBP_BGA_Opt2_28dB which includes BGA break-out via
- 110fF total die capacitance (100fF-Die + 10fF-PKG)
- Ball capacitance is a part of the extracted model
- ~3dB COM including 5Fext + 3Next



PKG85 + CaBP_BGAVia_Opt2_32dB

- Concatenated to 30mm 85Ω packages on both sides
- 100Ω max loss trace
- 110fF total die capacitance (100fF-Die + 10fF-PKG)
- Ball capacitance is a part of The Extracted Model
- ~1.3dB COM

Nominal or WorstCase?

- None… Not nominal and not worst case, rather a good design and "a bit of" manufacturing tolerance. (Can we allow a bit more tolerance? The model places us in a sweet spot… should we ask for more tolerance? Should we include Xtalk in the long PKG as well?)
- 8mm/12mm PKG model should follow the same concept as the 30mm but integrate Xtalk into both Rx and Tx sides (FEXT alone) to account for the small PKG footprint/size
- Crosstalk per PKG case suggested to be implemented as random noise with the applicable σ

Future Large 100G/lane Devices

- Not Covered by the model, but the model does not seem to have that margin @ this point
- Big packages will be one possible target implementation for 100Gbps/lane
- Need to consider the implications of a decision not to model future LGAs
- https://www.ectc.net/files/68/ECTC_2018_Luncheon_Keynote_BCOoi_Broadcom.pdf

IC Package Need	2018	2022	Challenges
Data Rate	56 Gbps	112 Gbps	• Channel Insertion Loss & Return Loss • Crosstalk • Power Integrity
Body Size	67.5mm x 67.5 mm	> 90mm x 90mm	• Package Warpage • Board Level Reliability • Socket Cost & Performance Penalty
2.5D Integration	Up to 5 dies	More/Larger dies (incl. Optical)	• Interposer Reticle Size • Assembly challenges • More Memory BW
Micro-bump Pitch	40um	<=30um	• Assembly challenges • Routing challenges
Power Dissipation	300 W	> 500 W	• Thermal Interface Material • Heatsink Solutions

ference – Luncheon Keynote Address

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Summary

- It was shown that a well designed 30mm 85Ω (90Ω with "some" manufacturing tolerance) PKG can pass the target interconnect with 3dB COM

Thank You!