

**100Gb/s KR COM**  
**- Reference Receiver (FFE / DFE)**  
**- Reference PKG**

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**IEEE802.3ck**

**November, 2018**

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- 1. Overview**
- 2. Backplane channels for simulation**
- 3. Ref\_receiver simulation (proprietary tool)**
- 4. Ref\_receiver COM simulation**
- 5. COM : PKG impedance combination effect**
- 6. COM : PKG Tx/Rx trace length combination effect**
- 7. Conclusion**

# 1. Overview

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## 1. 100G-KR COM Reference Receiver studies

- At ad hoc on 10/24/2018, "DFE-based model vs FFE-based model for Reference Rx of COM" (hidaka\_3ck\_adhoc\_01\_102418.pdf) was presented. In that, reference receiver equalizer, no FFE pre-tap and n-tap DFE reference receiver was recommended.
- A study based on this proposal was done.
- Comparison of COM reference receiver configuration (16-tap FFE with 1-tap DFE or 16-tap DFE) using proprietary tool for two (2) channels.
- Similar comparison using COM for more channels and equalizer settings.

## 2. COM PKG studies

- (1) Tx/Rx COM PKG impedance combination
- (2) Tx/Rx COM PKG trace length combination

# 1.1 reference receiver configuration

#	Tx FFE pre		Rx FFE pre		Rx FFE post		Rx DFE		PKG	result	note
	tap	step	tap	step	tap	step	tap	step			
1	3	2.5%	3	0%	16	0%	1	0%	30mm 87.5 $\Omega$ +1.8mm 92.5 $\Omega$ Cd=110fF, Cp=70fF	No significant COM difference	hidaka_3ck_adhoc_01_102418.pdf  - COM 2.52 - channel used #4, 11, 5, 7, 9, 6, 8, 10 (BP channel)
2		4%									
3		1%									
4	1	2.5%									
5	3	2.5%	0	-	16	0%	1	0%		0.55~0.96dB worse COM than with Rx FFE-pre (#1-4)	
6	3	2.5%	0	-	0	-	16	0%		No major COM difference to #5	
7	0	-	3	0%	16	0%	1	0%	27mm extracted Cd=110fF	No major difference between FFE and DFE.	- proprietary tool - channel #8,18
8					0	-	16	0%			
9	2	2.5%	3	0%	n	0%	1	0%	30/20mm* 92.5 $\Omega$ +1.8mm 92.5 $\Omega$ Cd=110fF, Cp=80fF	Depends on number of taps and PKG trace combination.	- COM 2.51 n=12/16/20/24/28 - channel #5,6,7,8,9,10,17
10					0	-	n	0%			

**This work**

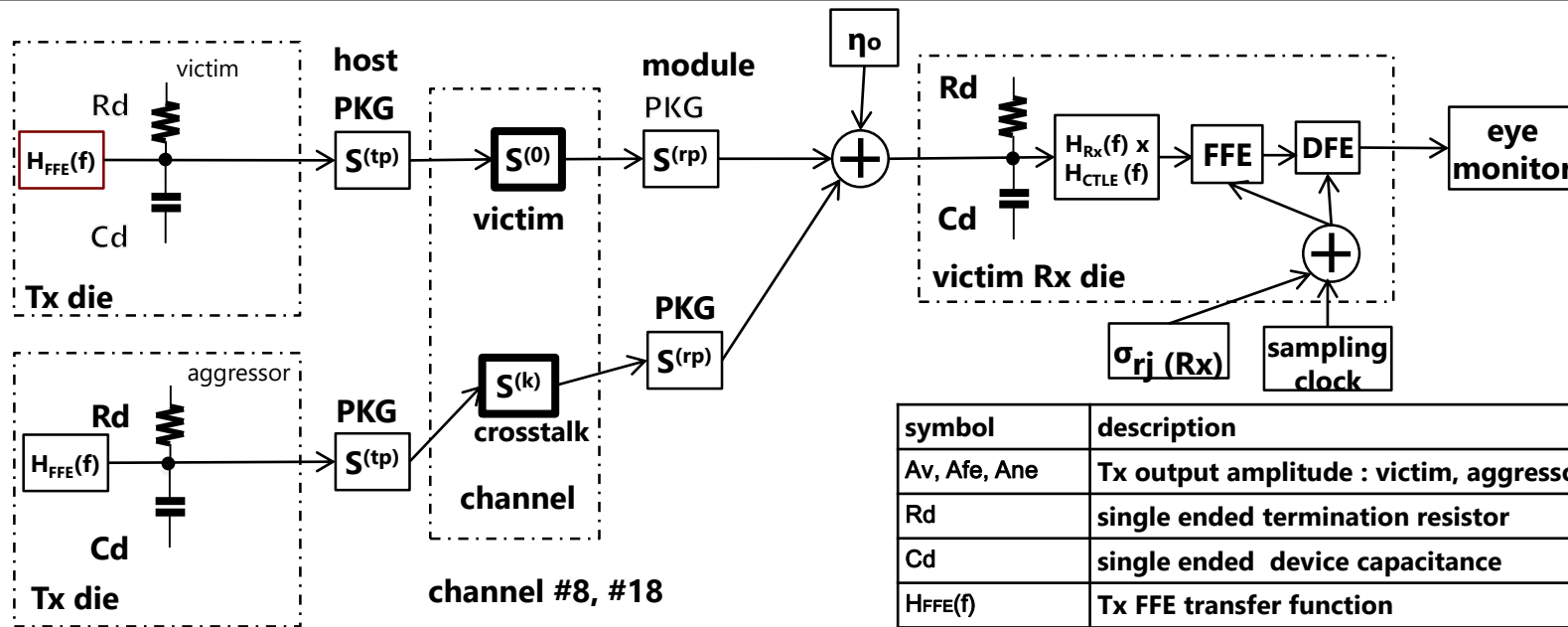
3

Tx FFE : 1-post / 5% (#7/8 : 0-post), fb = 53.125Gbd  
\* 30mm and 20mm Tx/Rx combination (4-cases each)

## 2. Backplane Channels for Simulation

#	contributor	type	IL [dB]*	ERL [dB]**	ICN [mV]	note	name in graph	reference
1	Mellitz	legacy	15.88	12.02	3.53	Tachyon_3"	ST3	[1][2]
2			25.55	12.89	2.68	Tachyon_13"	ST13	[1][3]
3			30.34	13.07	2.65	Tachyon_18"	ST18	[1][4]
4			28.01	52.77	0.00	"smooth" PCB Megtron-6	Sm	[7][8]
5		cabled	23.79	19.85	0.76	24dB_opt1, 30AWG 1m+0.3mx2+PCB 2.3"x2	S241	[5][6]
6			22.98	17.53	0.88	24dB_opt2, 30AWG 1m+0.3mx2+PCB 2.3"x2	S242	
7			27.59	20.85	0.56	28dB_opt1, 30AWG 1m+0.3mx2+PCB 4"x2	S281	
8			26.72	18.35	0.65	28dB_opt2, 30AWG 1m+0.3mx2+PCB 4"x2	S282	
9			31.36	21.80	0.44	32dB_opt1, 30AWG 1m+0.3mx2+PCB 5.8"x2	S321	
10			30.42	19.08	0.50	32dB_opt2, 30AWG 1m+0.3mx2+PCB 5.8"x2	S322	
11			27.98	73.98	0.00	"smooth" 26AWG twinax cabled	St	[7][8]
12	Zambell	cabled	28.60	21.99	0.39	1m 30 AWG, 3.2" PCB	Ac	
13		ortho	26.64	14.55	1.52	20" orthogonal	Ao	[10][11]
14	Heck	legacy	29.74	9.51	2.05	30dB, nominal, 85-ohm	In	[12][13]
15			29.62	8.80	2.03	30dB, high-low-high, 85-ohm	IhIh	[12][14]
16			29.85	8.04	2.05	30dB, low-high-low, 85-ohm	IlIh	[12][15]
17	Tracy	cabled				1m 30 AWG, 12" PCB	Tc	[17][18]
18		ortho				18" orthogonal	To	[17][19]

# 3.1 Simulation Model (proprietary tool)



PKG : 27mm  
extracted model

✓ The same as previous ones.

sakai\_100GEL\_01b\_0118.pdf, sakai\_100GEL\_01\_0318.pdf  
sakai\_3ck\_01b\_0918.pdf

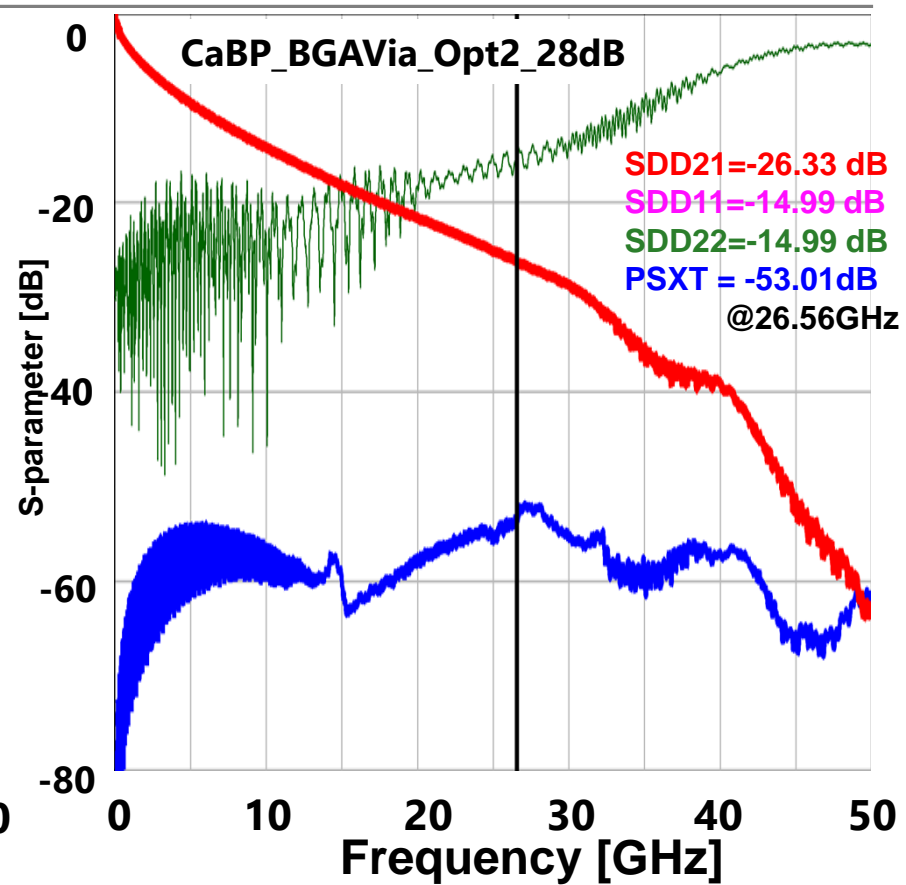
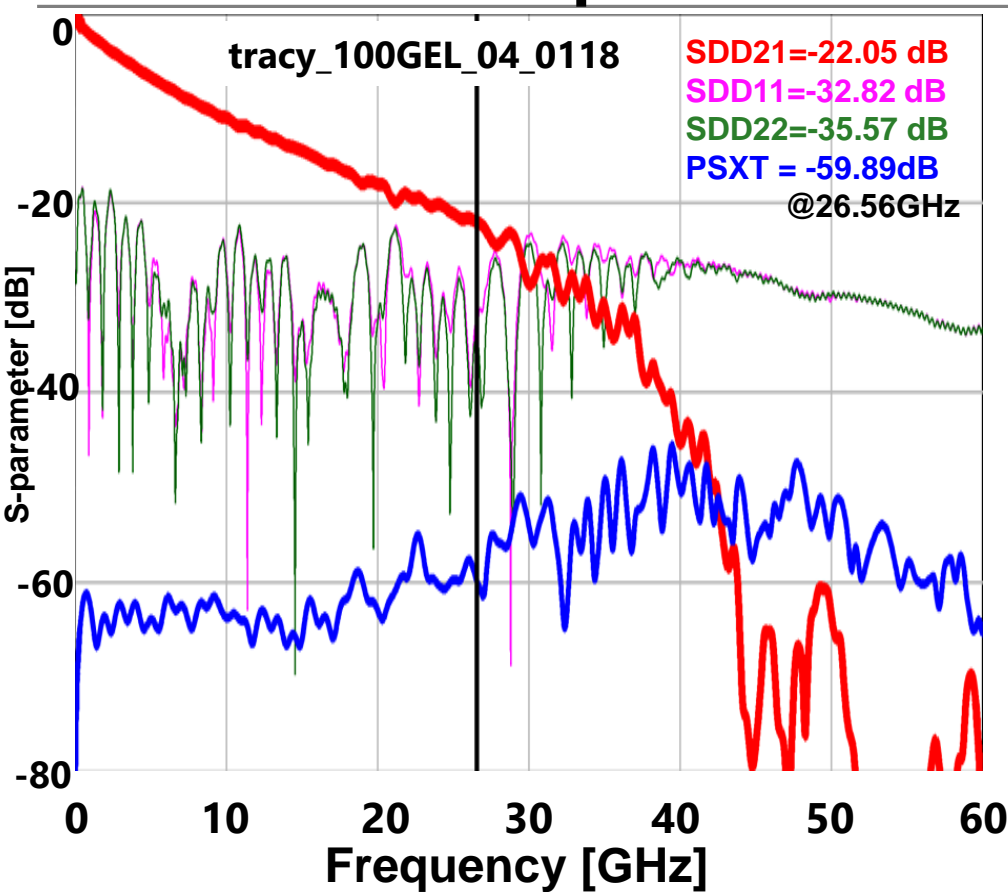
symbol	description
$A_v, A_{fe}, A_{ne}$	Tx output amplitude : victim, aggressor (FEXT, NEXT)
$R_d$	single ended termination resistor
$C_d$	single ended device capacitance
$H_{FFE}(f)$	Tx FFE transfer function
$S^{(tp)}, S^{(rp)}$	PKG model Tx/Rx
$S^{(0)}$	channel under test
$H_{Rx}(f)$	Rx noise filter
$H_{CTLE}(f)$	Rx CTLE transfer function
$\eta_0$	one-sided noise spec
Add	Dual-Dirac jitter, peak to peak Tx : before FFE Rx : considered as eye margin
$\sigma_{rj}$	random jitter, RMS Tx : before FFE Rx : before FFE/DFE

## 3.2 Simulation Set Up (proprietary tool)

- ✓ Static Channel Model Simulation (proprietary)
- ✓ Behavior model using MatLab
- ✓ Rx/CDR jitter (DJ) are considered as eye opening margin. (EW4, EH4)
- ✓ Crosstalk noise in channel S-parameter
- ✓ Impedance are nominal : 50-ohm single ended
- ✓ Transmitter equalization : none
- ✓ Receiver equalization :
  - “FFE” : FFE 3-pre + 16-post + 1-tap DFE
  - “DFE” : FFE 3-pre + 0-post + 16-tap DFE
- ✓ Same CTLE coefficients are used for both “FFE” and “DFE”.
- ✓ PKG model is based on current design.
  - PKG material : “GZ41”

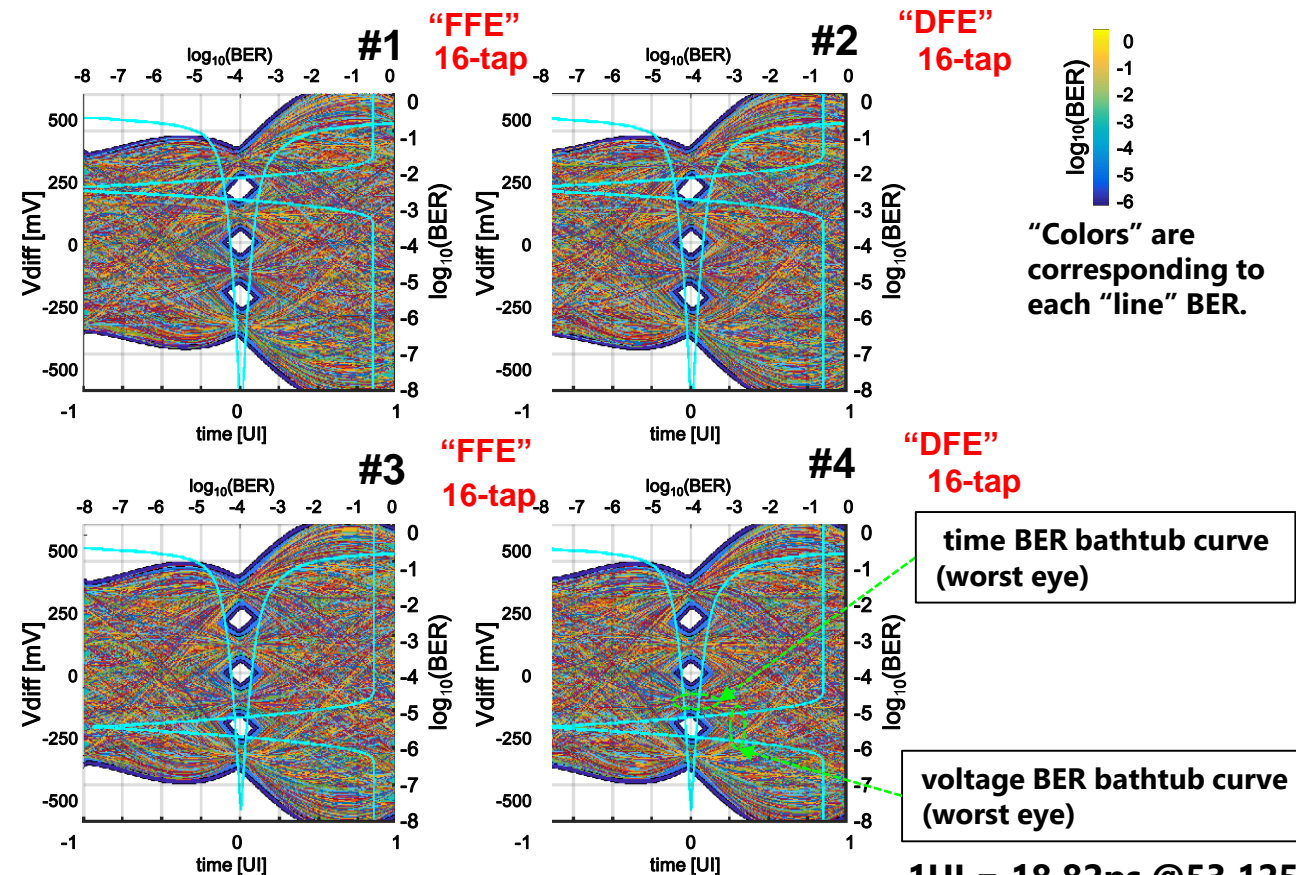
item	value	unit	note
modulation	PAM4		
pattern	PRBS13Q		
baud rate	53.125	Gbd	
DJ_Tx	60	mUI_pk-pk	conservative
RJ_Tx	10	mUI_rms	
EOJ_Tx	0	UI	
SNR_Tx	32.5	dB	
Rt_Tx	50	ohm	
Tx_FFE	1/0	tap/pre	no Tx equalization
Cd_Tx/Rx	110	fF	
Cp Tx/Rx	extracted		S-parameter PKG model
Rx FFE + DFE	3/n+1, 3/0+n		
Rx fr	3/4 fb		
Av	0.8	Vppd	
AVx	1.2	Vppd	
BER	1.0E-4		
$\eta_0$ eta0	8.2E-09	V <sup>2</sup> /GHz	
DJ_Rx	0	UI	included as eye margin
RJ_Rx	10	mUI_rms	
Rt_Rx	50	ohm	

### 3.3 Backplane Channel Characteristics





### 3.4 Simulation Result (FFE/DFE post taps)



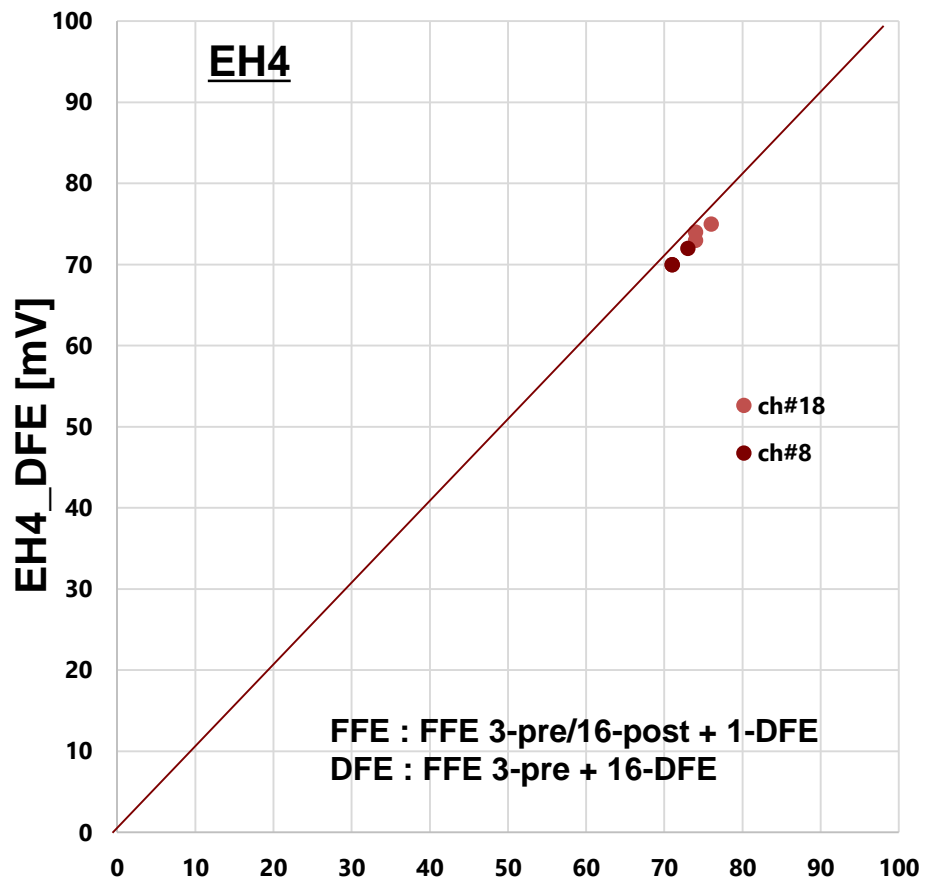
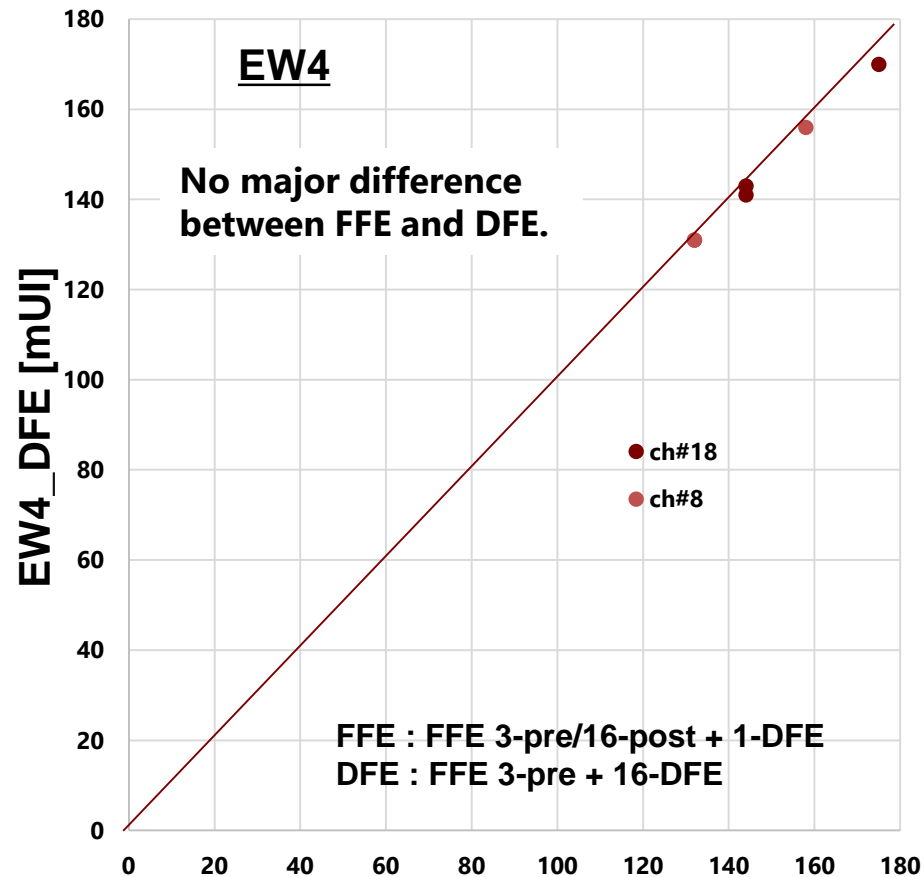
item		unit		#1	#2	#3	#4
baud rate		Gbd		53.125			
channel				#18/ortho		#8/cabled	
Tx	FFE	tap/pre		1/0			
	RJrms		mUI	10			
	SNR		dB	32.5			
Tx/ Rx	PKG trace		mm	27mm (extracted)			
	Cd		fF	110			
	Cp		fF	extracted			
Rx	CTLE	HF/LF		2p-1z/1p-1z			
	eta0	V <sup>2</sup> /GHz		8.2E-9			
	fr	x fb	GHz	3/4			
	FFE	pre		3			
		post		16	0	16	0
	DFE	post		1	16	1	16
	RJrms		mUI	10			
eye	EW4	upp	mUI	144	141	132	131
		mid		175	170	158	156
		low		144	143	132	131
	EH4	upp	mV	74	73	71	70
		mid		76	75	73	72
		low		74	74	71	70

criteria :  $EW4 \geq 100mUI$ ,  $EH4 \geq 20mV$

**1UI = 18.82ps @53.125Gbd**

**No major difference between "FFE" and "DFE".**

### 3.4.1 Simulation Result (FFE/DFE post taps)



1UI = 18.82ps @53.125Gbd

EW4\_FFE [mUI]

EWH\_FFE [mV]

# 4.1 COM parameters (example)

COM 2.51

flex\_PKG model

Table 93B-1 parameters			
Parameter	Setting	Units	Information
f_b	58	Gbd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.3e-4 1.3e-4]	nF	[TX RX]
z_p select	[1 2 3 4 5]		[test cases to run]
z_p (TX)	[15.5 10.20 30.1 8.1 8.1 8.0 0.0; 7.5 12.5 10.0 5.0 0.0; 7.0 12.5 10.0 5.0 0.0]	mm	[test cases]
z_p (NEXT)	[15.5 10.20 30.1 8.1 8.1 8.0 0.0; 7.5 12.5 10.0 5.0 0.0; 7.0 12.5 10.0 5.0 0.0]	mm	[test cases]
z_p (FEXT)	[15.5 10.20 30.1 8.1 8.1 8.0 0.0; 7.5 12.5 10.0 5.0 0.0; 7.0 12.5 10.0 5.0 0.0]	mm	[test cases]
z_p (RX)	[15.5 10.20 30.1 8.1 8.1 8.0 0.0; 7.5 12.5 10.0 5.0 0.0; 7.0 12.5 10.0 5.0 0.0]	mm	[test cases]
C_p	[1.0e-4 1.0e-4]	nF	[TX RX]
C_v	[0.1e-4 0.1e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[ 50 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6	min	
c(-1)	[-0.3;0.025;0]	[min;step;max]	
c(-2)	[0;0.025;0.1]	[min;step;max]	
c(-3)	[0]	[min;step;max]	
c(-4)	[0]	[min;step;max]	
c(1)	[-0.3;0.05;0]	[min;step;max]	
N_b	1	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
g_DC	[-20;1;0]	dB	[min;step;max]
f_z	23.2	GHz	
f_p1	23.2	GHz	
f_p2	58	GHz	
g_DC_HP	[-6;1;0]		[min;step;max]
f_HP_P2	0.725	GHz	
ffe_pre_tap_len	3	UI	
ffe_post_tap_len	12	UI	
Include PCB	0	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		

with Rx FFE

Rx FFE constraints

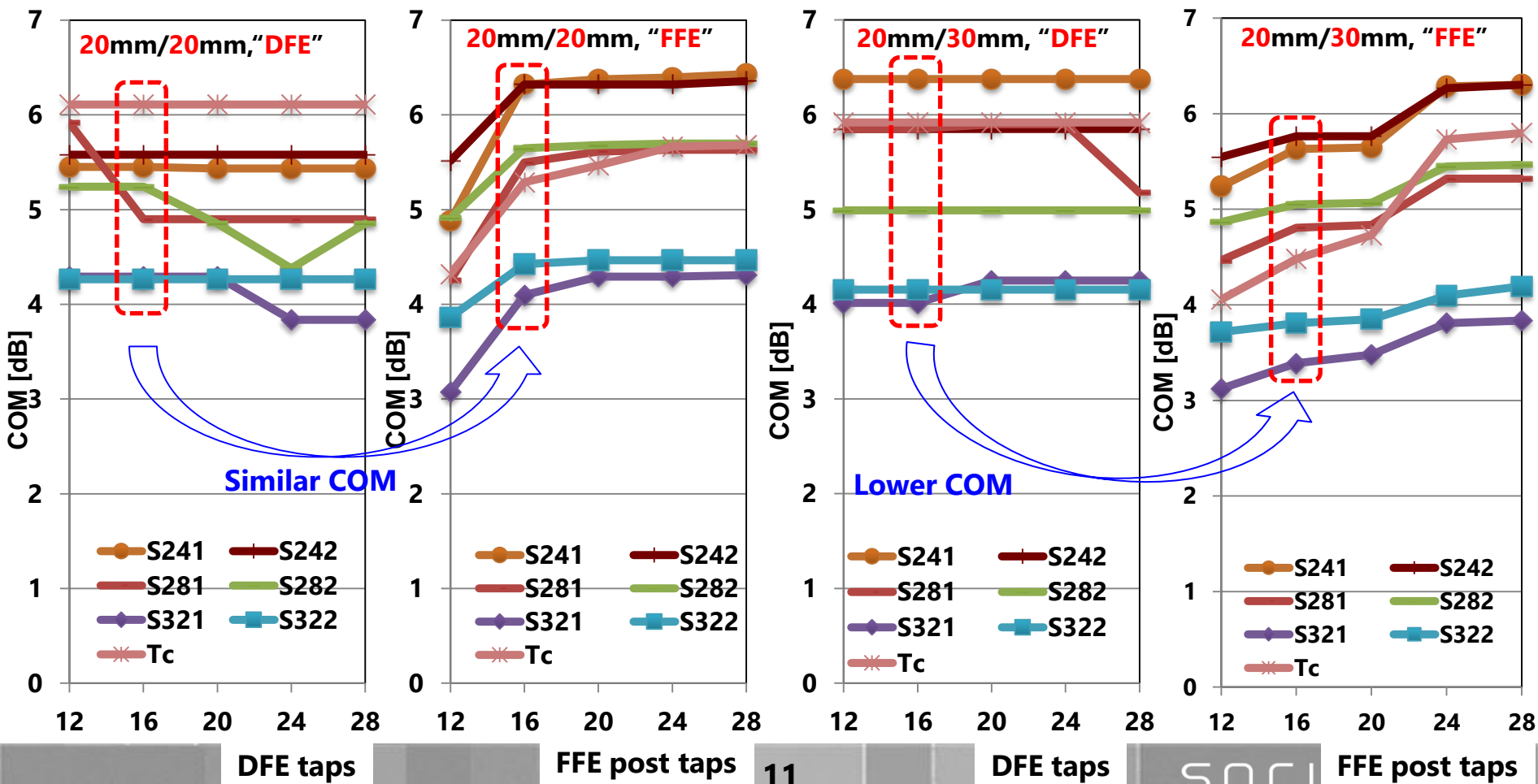
I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	./results/	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	112G-LR_530-D01-R3-12	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.E-04	
Include PCB	0	Value
T_r	6.E-03	ns
FORCE_TR	1	logical

TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR Butterworth	1	logical
beta_x	1.7.E+09	
rho_x	0.18	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	0.005	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.2E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

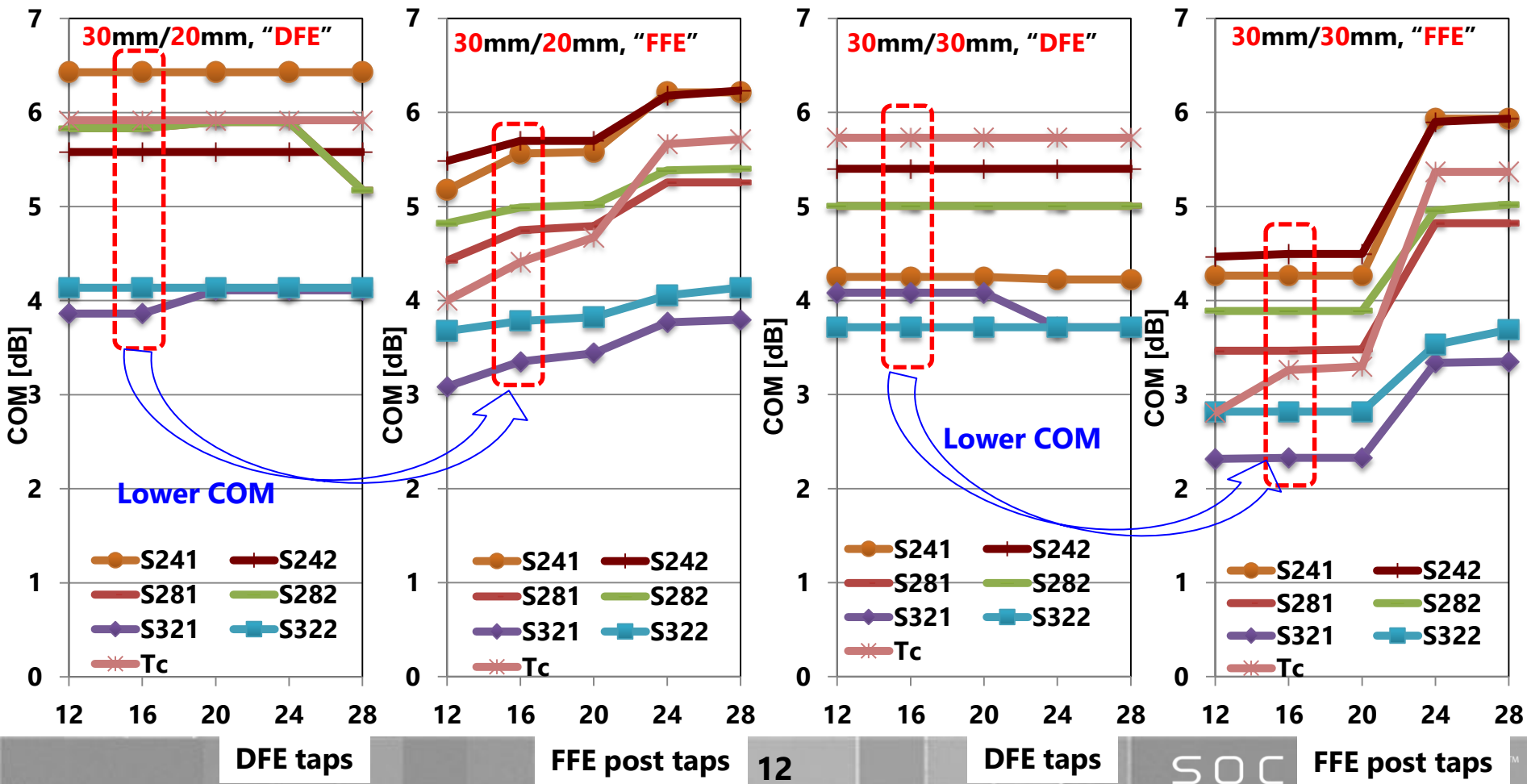
Table 93B-2 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5; 110 110; 87.5 87.5; 87.5 87.5]	Ohm (tldr sel)
Table 92-2 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	0.00579	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	115	mm
z_bp (NEXT)	115	mm
z_bp (FEXT)	115	mm
z_bp (RX)	115	mm

- ✓ fb : **53.125**Gbd (fixed, PAM4)
- ✓ Tx FFE : 2-pre/1-post
- ✓ CTLE pole/zero frequencies : proportional to fb
- ✓ Rx FFE : skewed
- ✓ Rx DFE : 1-tap (fixed)
- ✓ Cd=110fF, Cp/Cv : 80fF/0fF
- ✓ Rd=50 ohm
- ✓ Zc : 92.5-ohm
- ✓ sigma\_RJ : 0.01UI
- ✓ A\_DD : 0.02UI
- ✓ SNR\_TX : 32.5dB
- ✓ DER\_0 : 1E-4

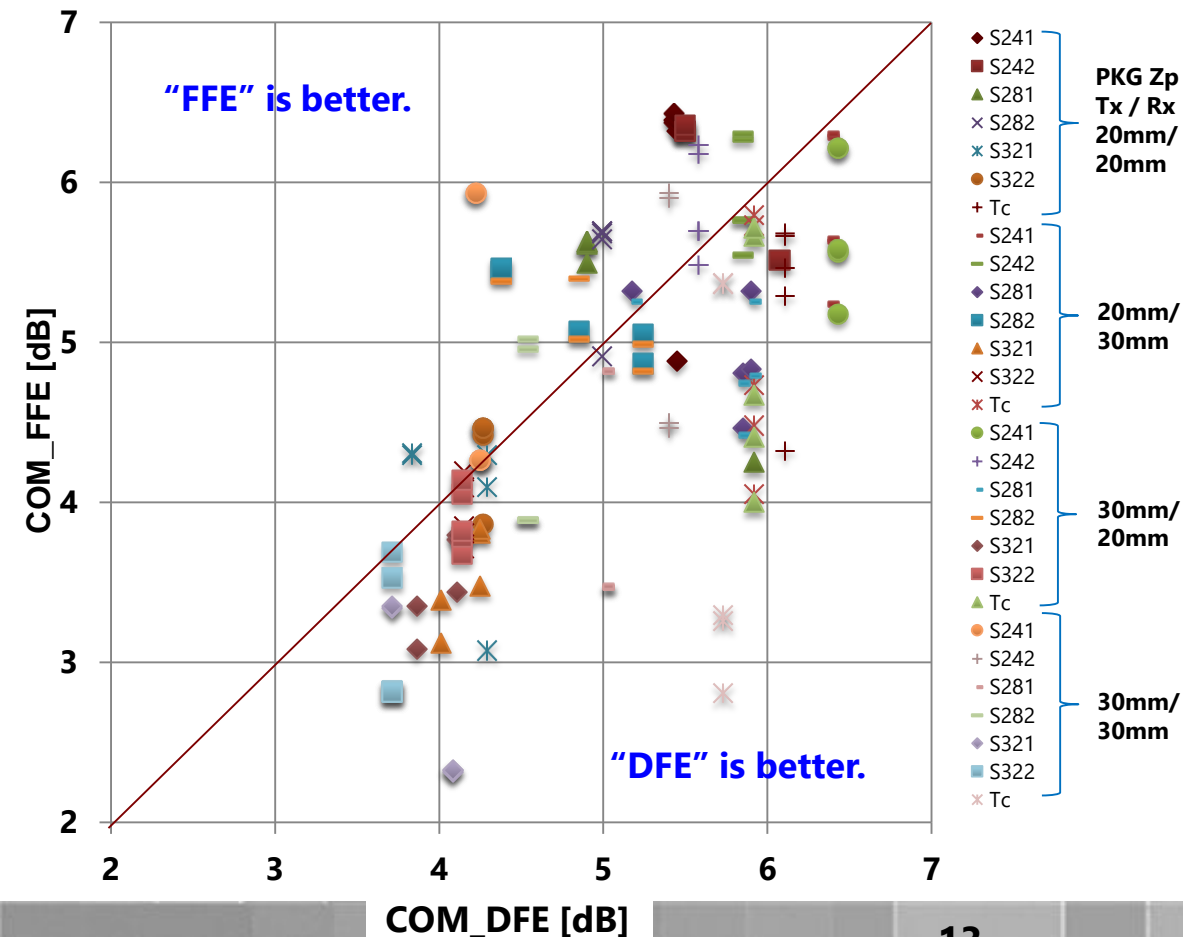
# 4.2 COM Simulation Result ("FFE"/"DFE" post taps)



# 4.3 COM Simulation Result (FFE/DFE post taps)



# 4.4 COM : FFE/DFE comparison



- Rx EQ

“FFE” : FFE (3-pre/n-post) + DFE (1-tap)

“DFE” : FFE (3-pre/0-post) + DFE (n-tap)

- n=12/16/20/24/28

- with crosstalk, noise

- Tx FFE : 2-pre (2.5%/2.5%, 0.1/-0.3)  
1-post (2.5%, -0.3)

- fb=53.125Gbd

- Cd=110fF, Cp=80fF

- PKG Zp Tx/Rx : skewed

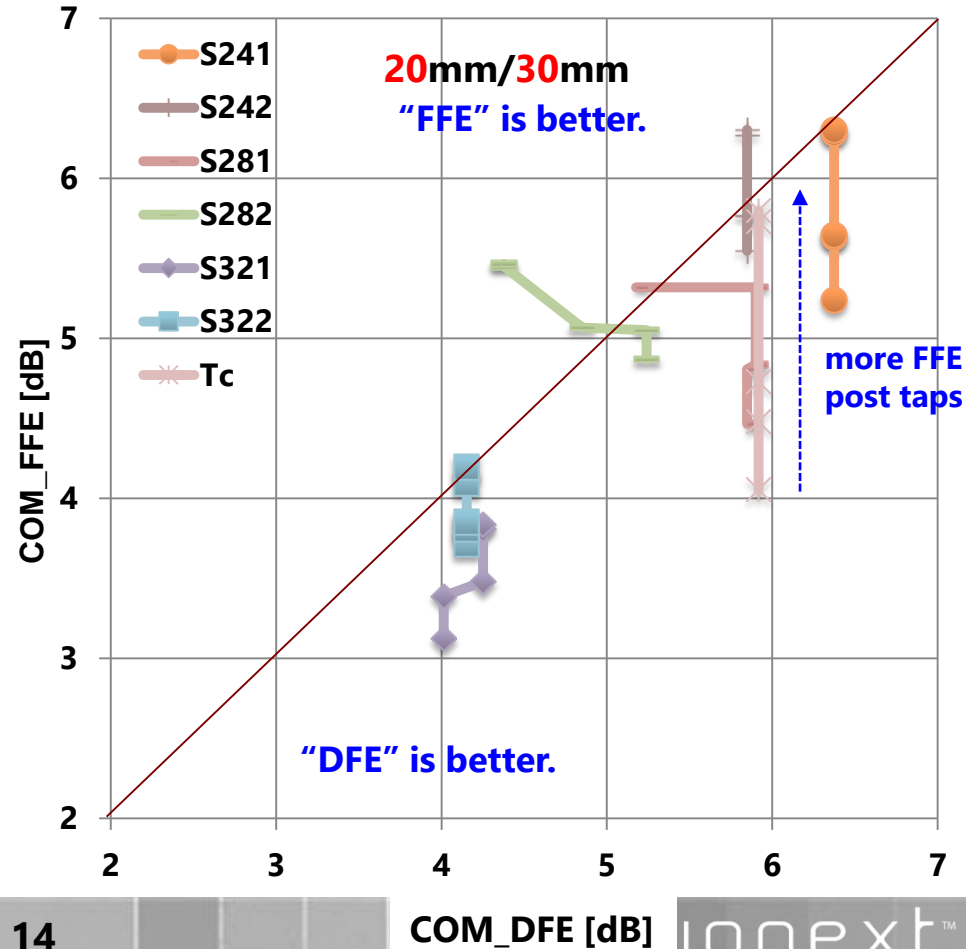
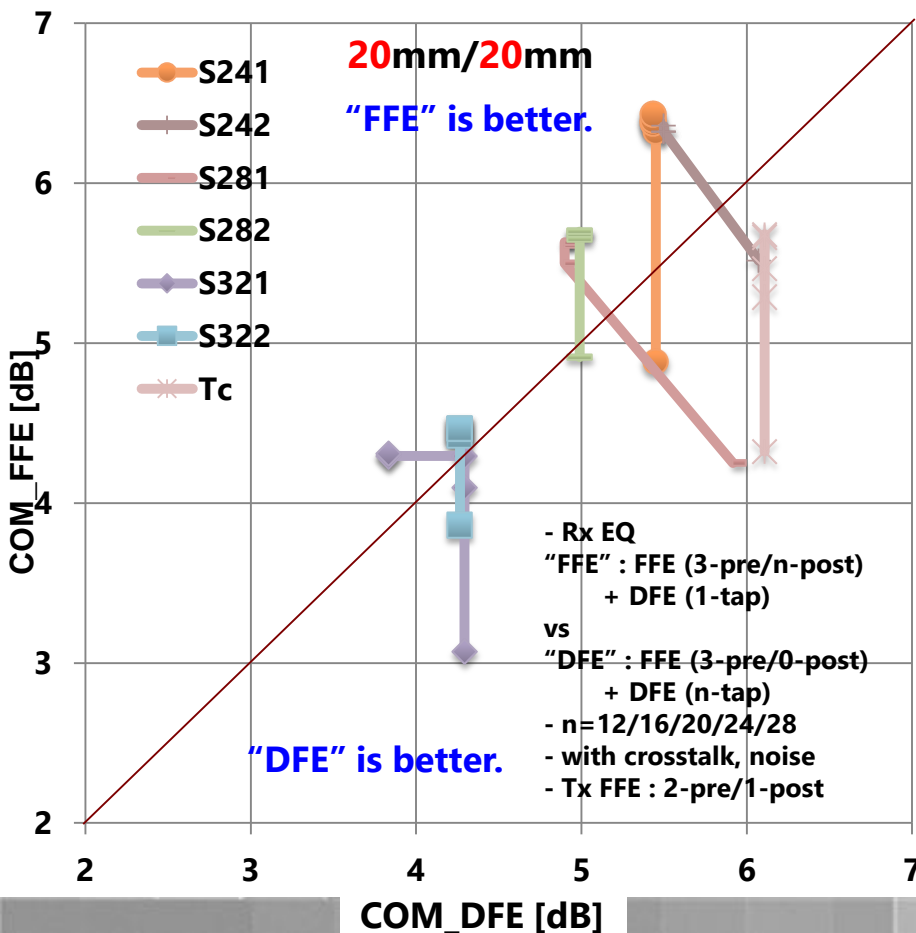
- PKG Zc : 92.5ohm

✓ “DFE” COM values are similar or better than “FFE” COM values, depending on conditions.

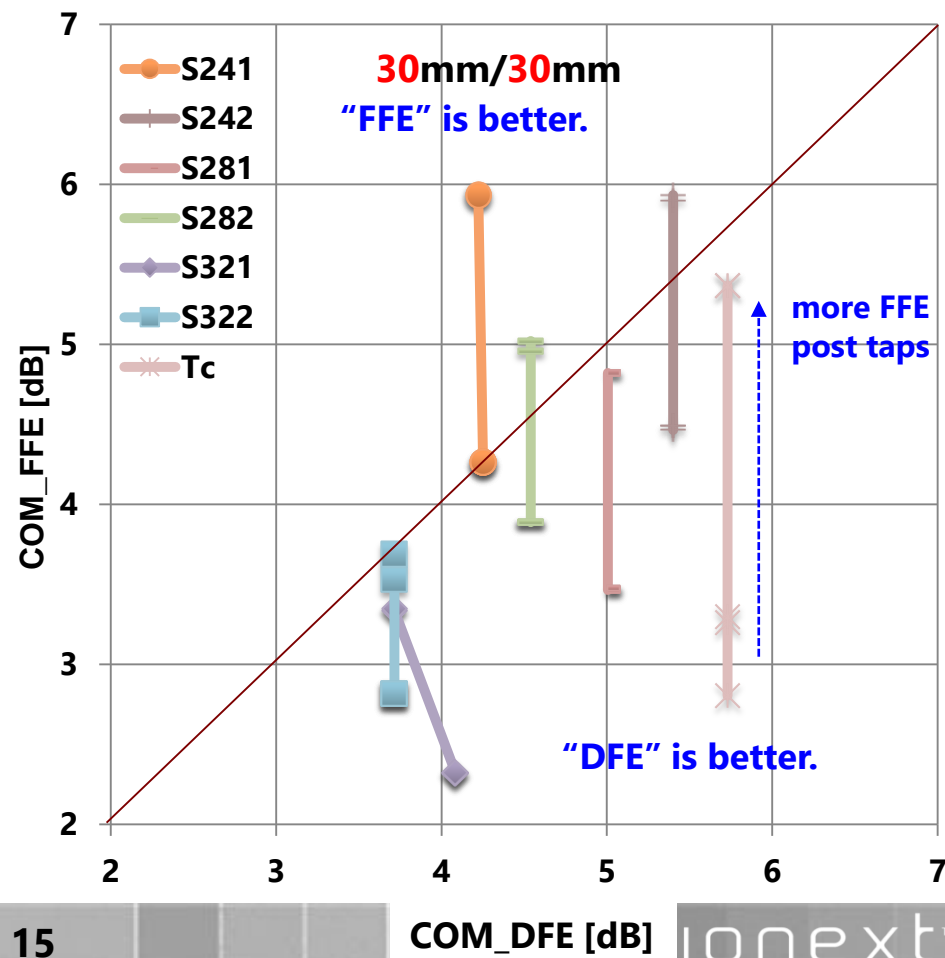
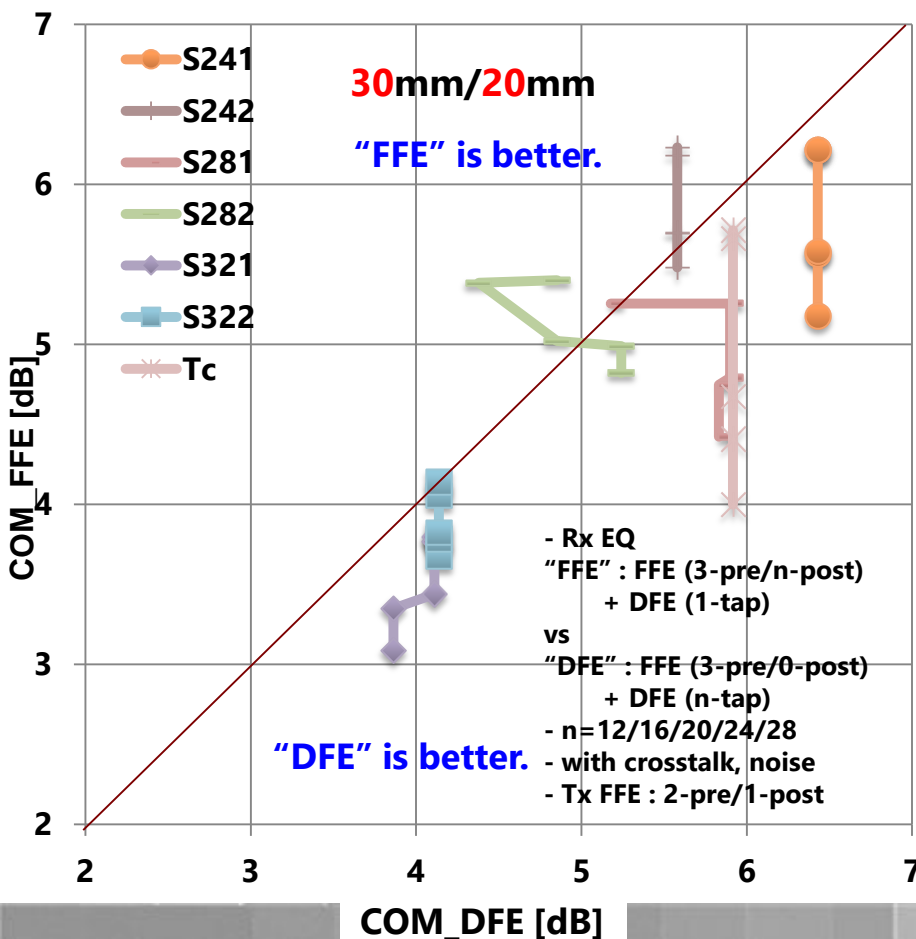
✓ FFE post taps affects significantly, while DFE taps do not.

✓ PKG trace length combination also affects in these cases.

## 4.4.1 COM FFE/DFE

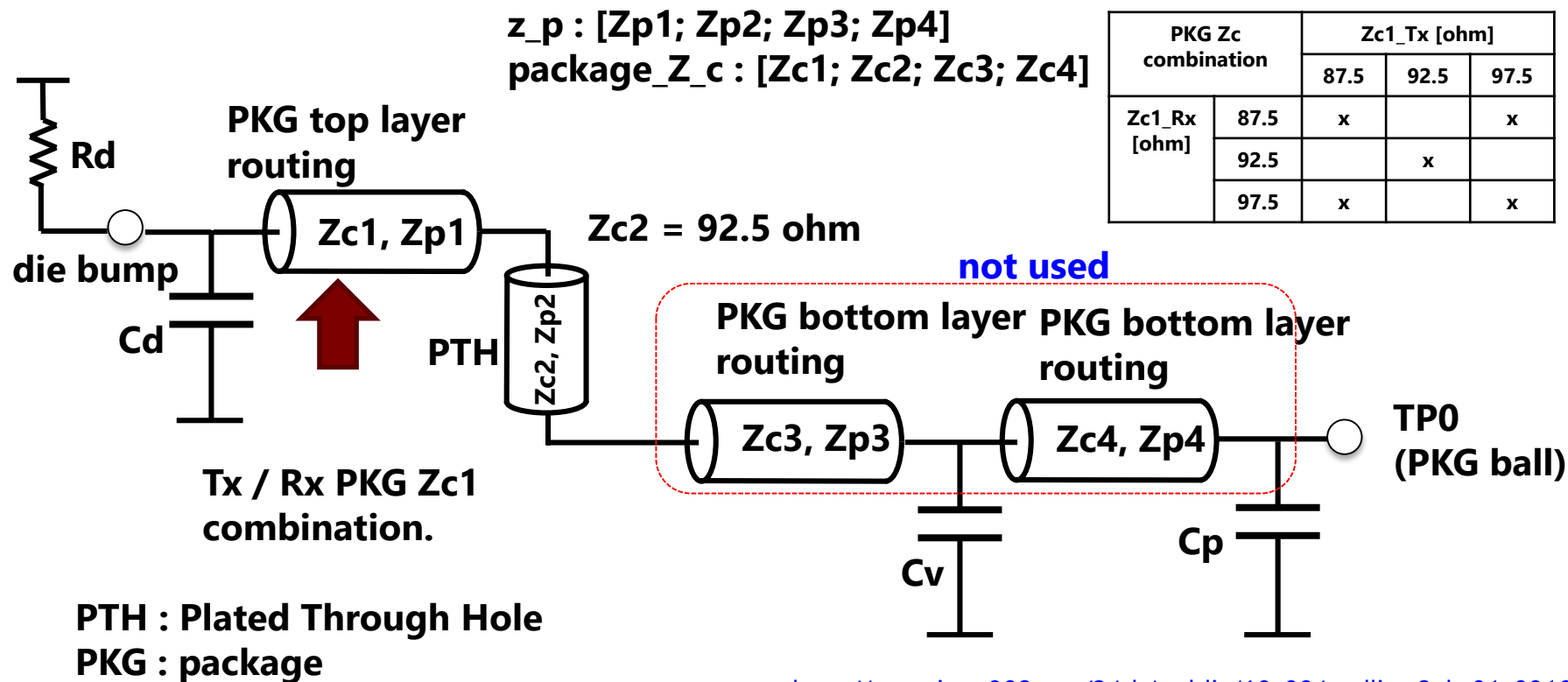


## 4.4.2 COM FFE/DFE comparison



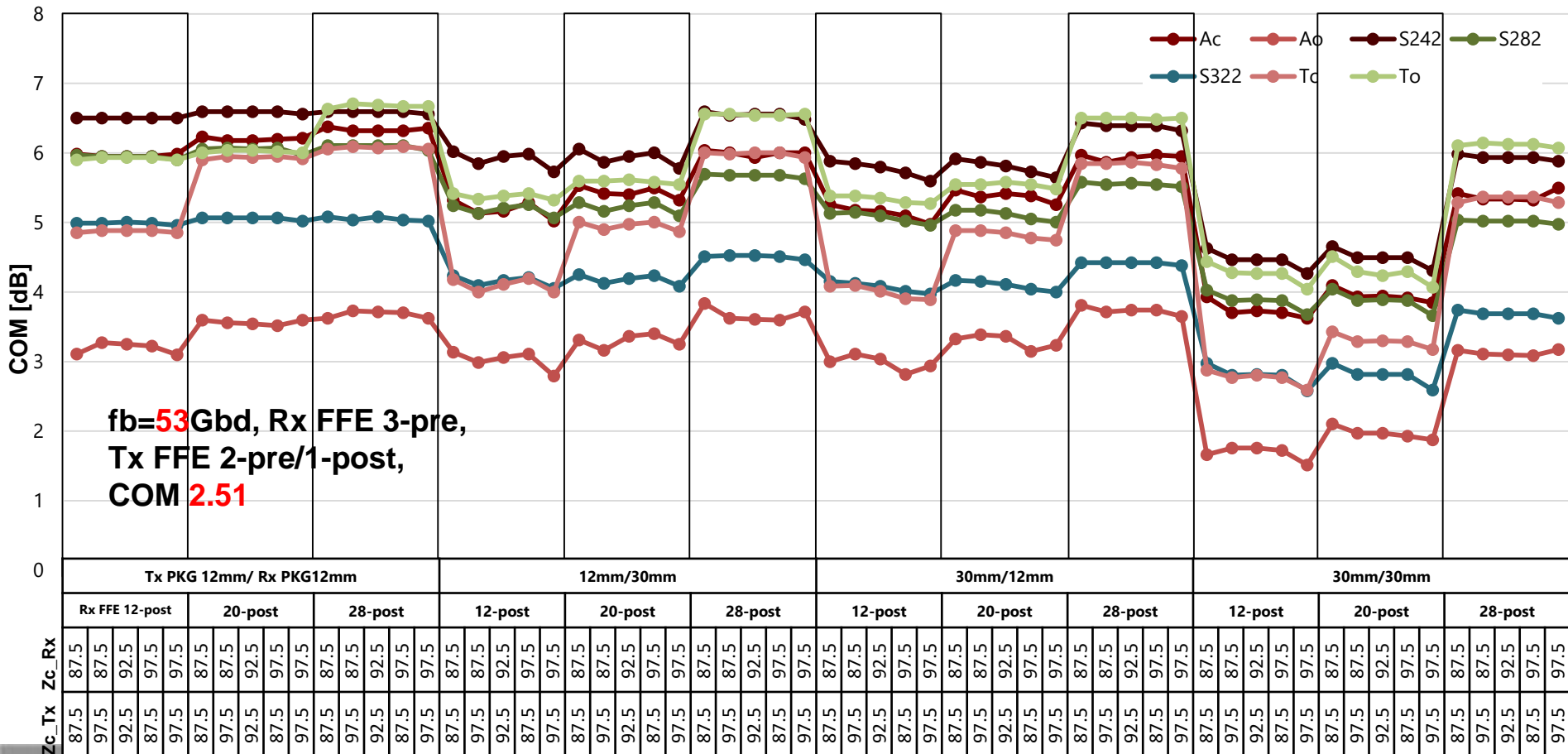


# 5. flexible\_PKG model parameters

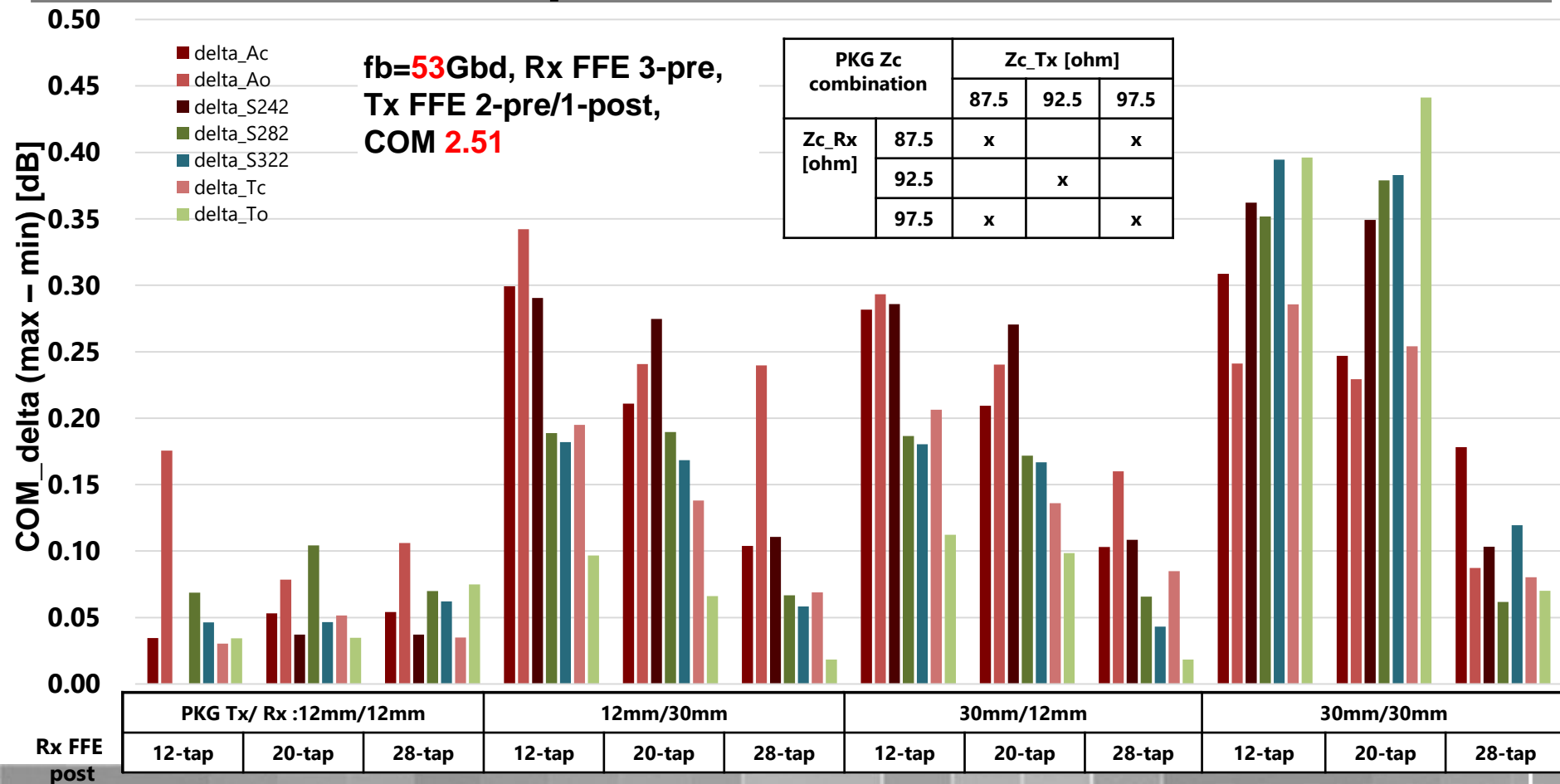


✓ In this COM sim, Zp3 and Zp4 are set to "0".

[http://www.ieee802.org/3/ck/public/18\\_09/mellitz\\_3ck\\_01\\_0918.pdf](http://www.ieee802.org/3/ck/public/18_09/mellitz_3ck_01_0918.pdf)



# 5.2 PKG trace impedance vs COM\_delta (max-min)

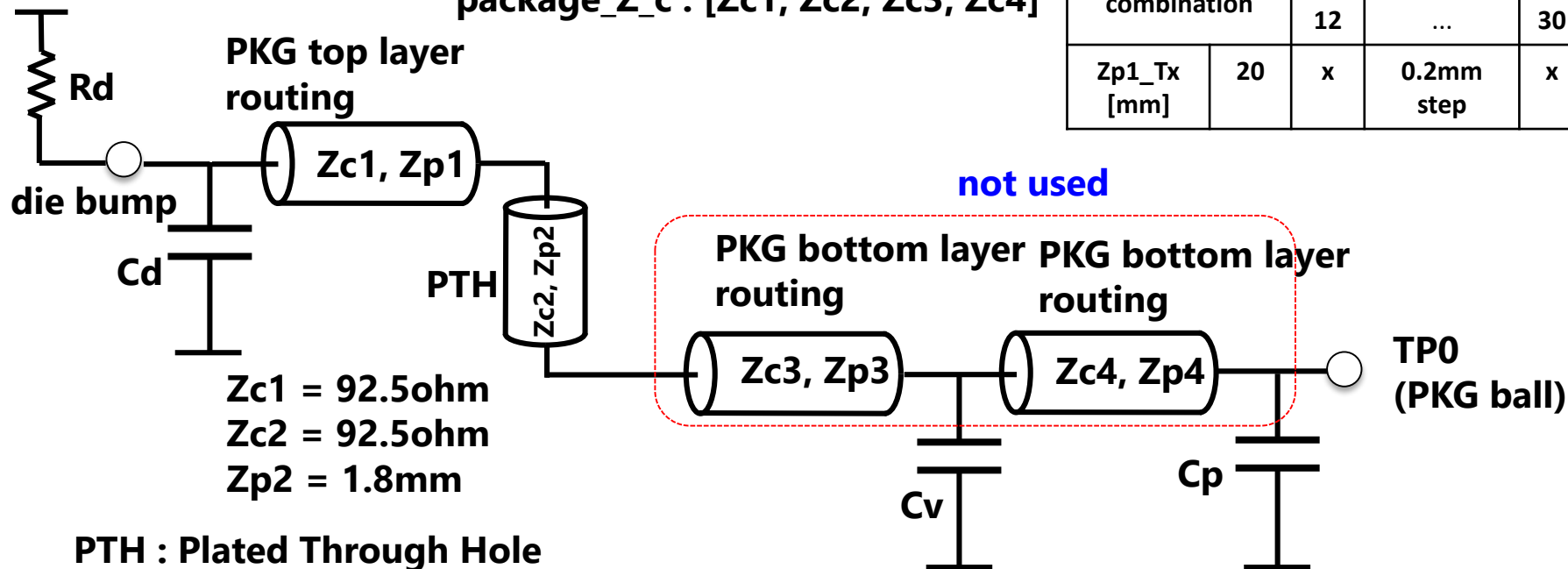


## 6. flexible\_PKG model parameters

$z\_p : [Zp1; Zp2; Zp3; Zp4]$

$package\_Z\_c : [Zc1; Zc2; Zc3; Zc4]$

PKG Zp1 combination		Zp1_Rx [mm]		
		12	...	30
Zp1_Tx [mm]	20	x	0.2mm step	x



$Zc1 = 92.5\text{ohm}$

$Zc2 = 92.5\text{ohm}$

$Zp2 = 1.8\text{mm}$

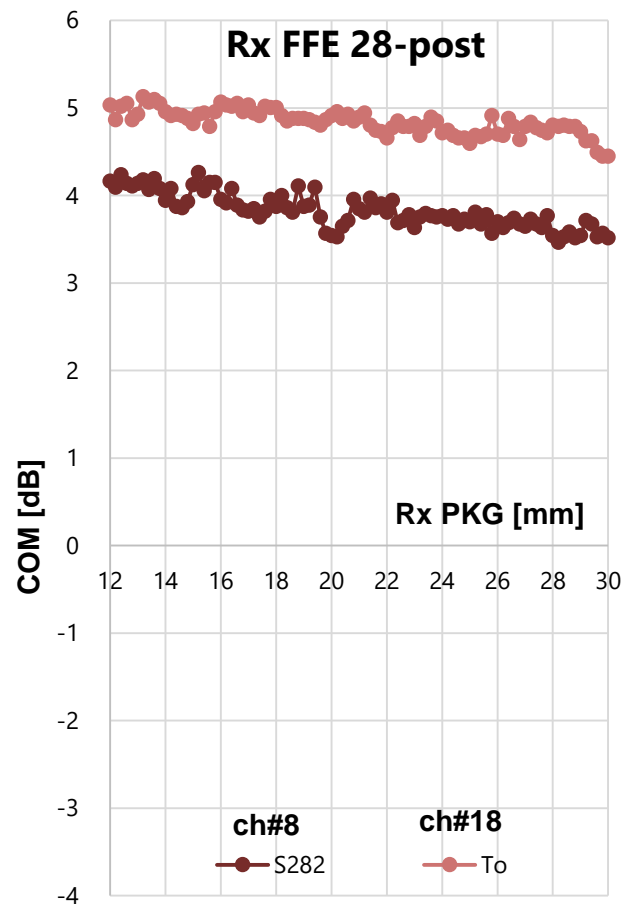
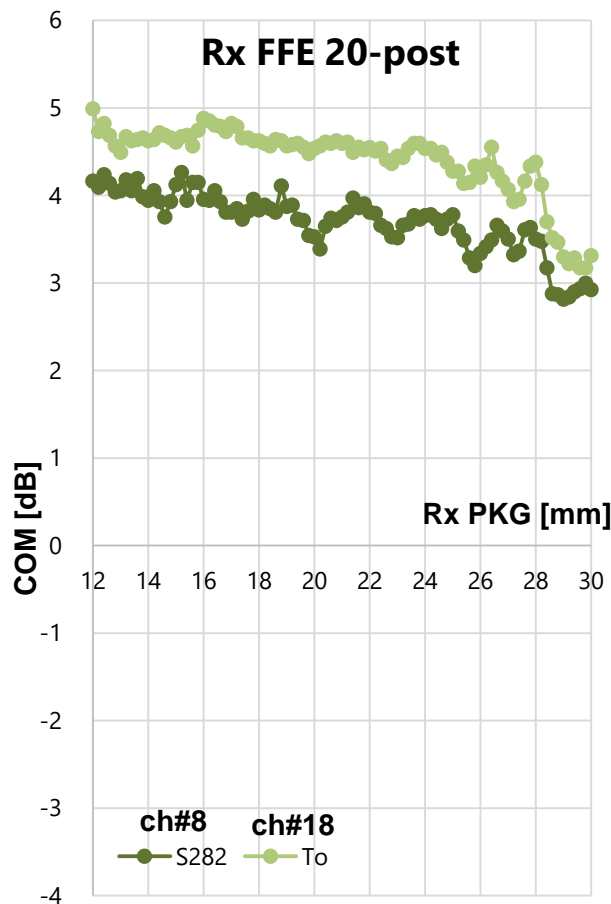
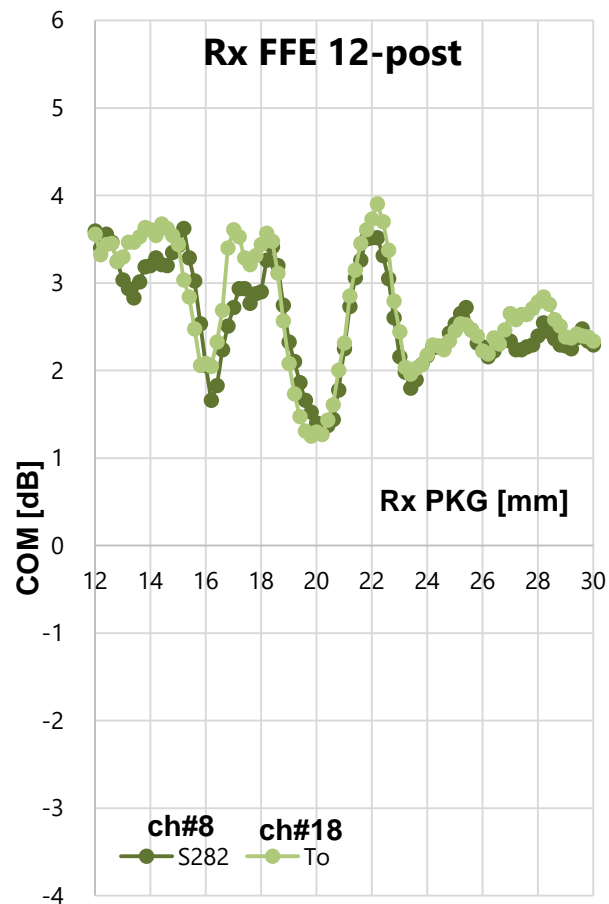
**PTH : Plated Through Hole**

**PKG : package**

✓ In this COM sim,  $Zp3$  and  $Zp4$  are set to “0”.

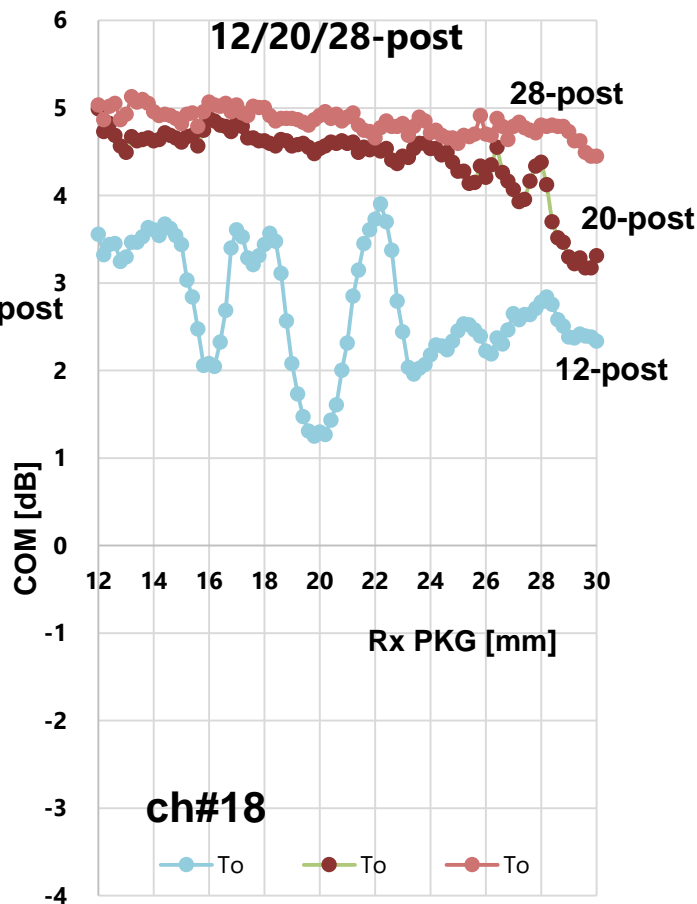
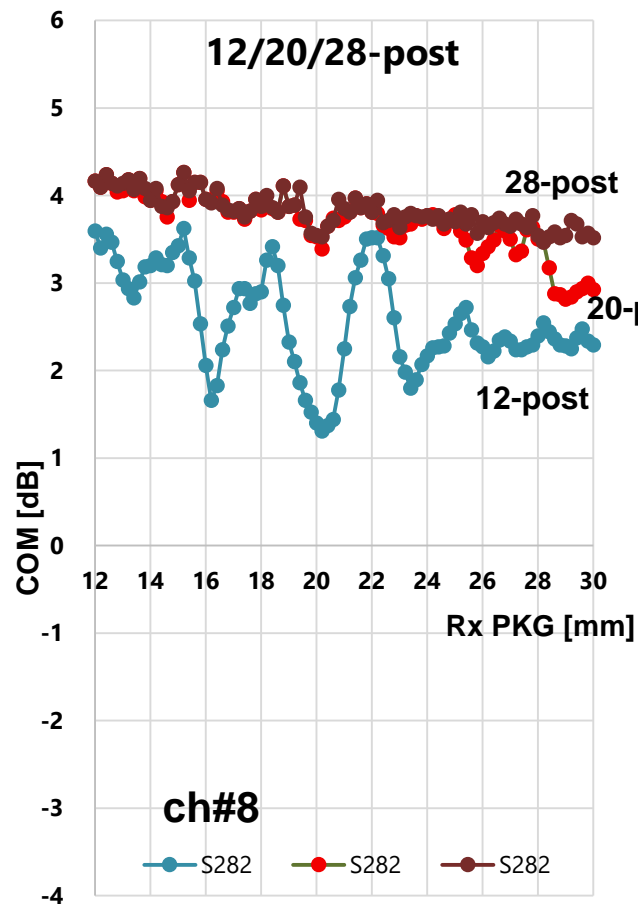
[http://www.ieee802.org/3/ck/public/18\\_09/mellitz\\_3ck\\_01\\_0918.pdf](http://www.ieee802.org/3/ck/public/18_09/mellitz_3ck_01_0918.pdf)

# 6.1 Rx-PKG trace length vs COM (Tx PKG 20mm)



fb=58Gbd, Cp=110fF, Cd=130fF, Rx FFE 3-pre, COM 2.51

## 6.2 Rx-PKG trace length vs COM (Tx PKG 20mm)



fb=58Gbd, Cp=110fF, CD=130fF, Rx FFE 3-pre, COM 2.51

## 7. Conclusion

1. Several results including this contribution show “DFE-based” reference receiver model has comparable performance compared with “FFE-based” model.

- However, some of COM simulation results show “DFE” performs better than “FFE”, depending on conditions.

- Using no Rx FFE pre-taps degrades COM in 0.55~0.96dB\* due to coarse Tx FFE pre-tap resolution (step). However in actual silicon implementation including Tx FFE-rich design with no Rx FFE, fine resolution Tx FFE pre-taps will be used, I think.

- So, for COM reference receiver model, using Rx FFE pre-tap (probably 3-taps) and coarse Tx FFE pre-tap resolution (because of simulation time) will be acceptable.

- For the time being, it is preferable to use “DFE-based” model with Rx FFE pre-taps.

- It is necessary to verify further with more channels, tap conditions (Rx or Tx FFE pre/post-tap, tap resolution) and other parameters (like PKG trace combination) to define COM reference receiver configuration and parameters.

\* [http://www.ieee802.org/3/ck/public/adhoc/oct24\\_18/hidaka\\_3ck\\_adhoc\\_01\\_102418.pdf](http://www.ieee802.org/3/ck/public/adhoc/oct24_18/hidaka_3ck_adhoc_01_102418.pdf)

## 7. Conclusion (continues)

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2. **COM PKG impedance combination (Tx\_PKG and Rx\_PKG) affects up to 0.4dB.**
  - **Is it necessary to run the PKG impedance combinations or just put this effect into “3dB margin” value?**
  
3. **COM PKG Tx and Rx trace combination affects COM values.**
  - **How is this handled?**
  - **Run various combinations? Or putting it into margin?**



# A. references

- Mellitz
- [1] [http://www.ieee802.org/3/100GEL/public/adhoc/jan03\\_18/mellitz\\_100GEL\\_adhoc\\_01\\_010318.pdf](http://www.ieee802.org/3/100GEL/public/adhoc/jan03_18/mellitz_100GEL_adhoc_01_010318.pdf)
  - [2] [http://www.ieee802.org/3/100GEL/public/tools/backplane/mellitz\\_100GEL\\_adhoc\\_03\\_010318.zip](http://www.ieee802.org/3/100GEL/public/tools/backplane/mellitz_100GEL_adhoc_03_010318.zip)
  - [3] [http://www.ieee802.org/3/100GEL/public/tools/backplane/mellitz\\_100GEL\\_adhoc\\_02\\_010318.zip](http://www.ieee802.org/3/100GEL/public/tools/backplane/mellitz_100GEL_adhoc_02_010318.zip)
  - [4] [http://www.ieee802.org/3/100GEL/public/tools/backplane/mellitz\\_100GEL\\_adhoc\\_04\\_010318.zip](http://www.ieee802.org/3/100GEL/public/tools/backplane/mellitz_100GEL_adhoc_04_010318.zip)
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# Thank you!

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