

# Performance comparison study for Rx vs Tx based equalization for C2M links

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# Outline

- AWGN theory on Tx vs. Rx equalization
- Simulation results based on realistic channels and SerDes models

# Assumptions for Theoretical Model

- Channel amplitude response has linear roll-off in dB
- Infinite length linear equalization
- Zero forcing solution
- Noise modeled as AWGN

# Equalization Penalty

## ■ Rx Linear Equalization Penalty:

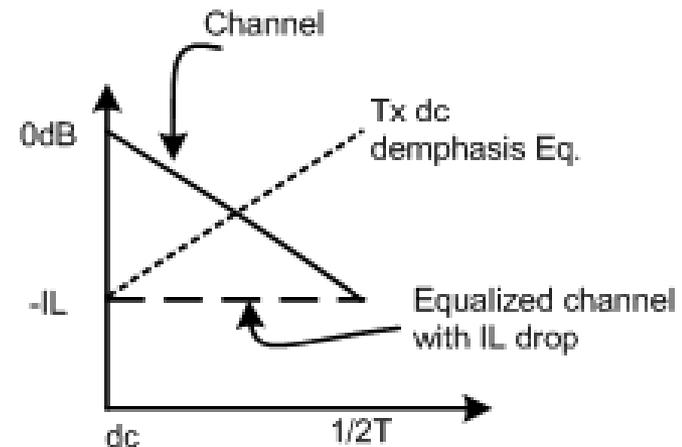
$$Rx\_P = 10 \log_{10} \left( T \int_{-1/2T}^{1/2T} 1/|H(f)|^2 df \right)$$

where  $|H| = 10^{(-2T*f*IL/20)}$  and IL is the insertion loss at Nyquist.

$$Rx\_P = 10 \log_{10} \left( \frac{10^{IL/10} - 1}{IL \cdot \ln(10) / 10} \right)$$

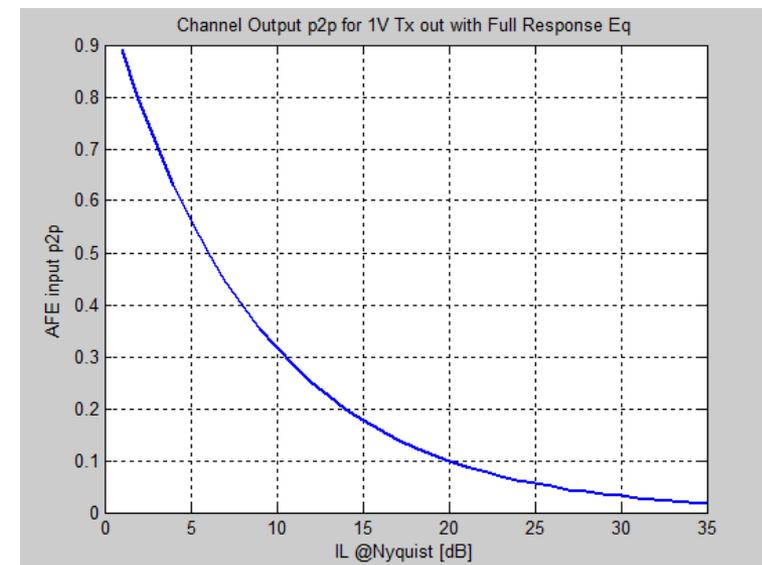
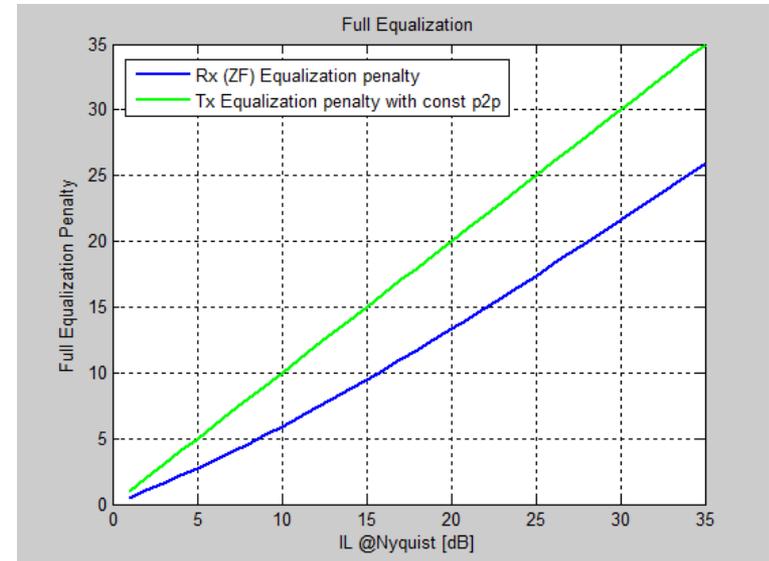
## ■ Tx Equalization Penalty:

$$Tx\_P = IL$$



# Theoretical Equalization Penalty Comparison

- Tx equalization is worse than Rx equalization. Rx Eq penalty follows L2-norm of  $1/|H|$  and Tx Eq penalty follows Infinite-norm of  $1/|H|$ .
- At  $IL=12\text{dB}$ , Tx penalty is 12dB but Rx penalty is 7.3dB. 4.7dB delta.
- With say  $IL=12\text{dB}$ , with Tx equalization, the Rx input p2p is only 250mvp2p for 1Vp2p @ Tx out.



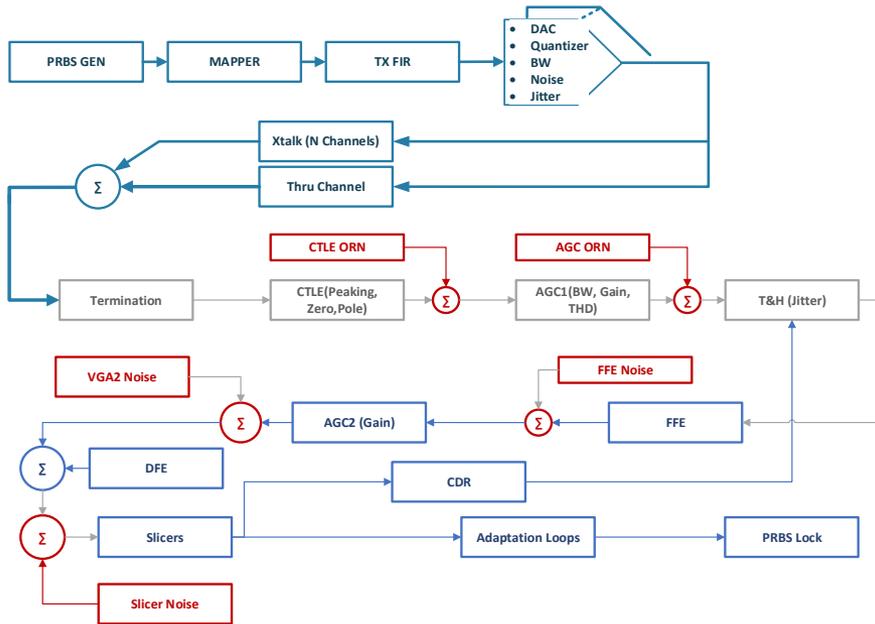
# Specs used for the analysis

	High level specs used for analysis			Comments
	<b>Buad Rate</b>	<b>53.125</b>	<b>Gbuad</b>	
<b>TX</b>	<b>TX Swing</b>	<b>0.8</b>	<b>Vdpp</b>	
	<b>RLM</b>	<b>0.95</b>	<b>-</b>	
	<b>SNDR</b>	<b>33</b>	<b>dB</b>	
	<b>RJ</b>	<b>175</b>	<b>fs rms</b>	
	<b>DJ</b>	<b>400</b>	<b>fs pk-pk</b>	
	<b>FIR</b>	<b>4</b>	<b>Taps</b>	<b>2 Pre</b>
	<b>TX Rise time</b>	<b>6.5</b>	<b>ps</b>	<b>20%-80%</b>
<b>RX</b>	<b>CTLE Boost</b>	<b>10</b>	<b>dB</b>	
	<b>CTLE 2nd Pole</b>	<b>40</b>	<b>GHz</b>	
	<b>Rx Noise</b>	<b>4</b>	<b>mV rms</b>	<b>actual density incorporated</b>
	<b>RJ</b>	<b>175</b>	<b>fs rms</b>	
	<b>DJ</b>	<b>600</b>	<b>fs pk-pk</b>	
	<b>Die CAP</b>	<b>130</b>	<b>fF</b>	

# Simulation Model

## Model 1: "Rx EQ"

### Tx 4 Tap FIR

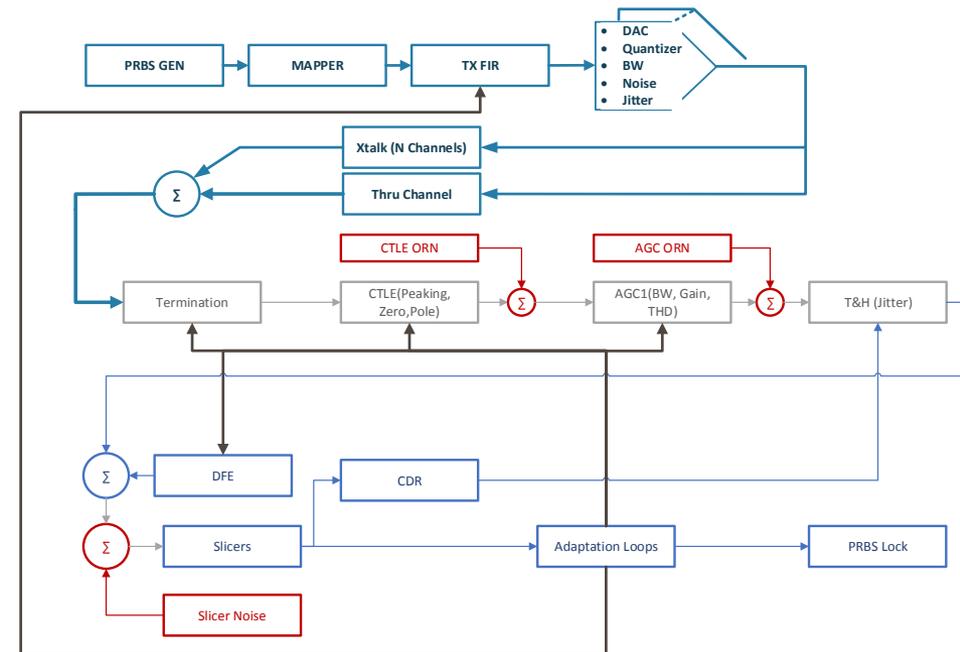


### Rx 6 Tap FFE

Noise contribution of AFE blocks added at the appropriate location in the link

## Model 2: "Tx EQ"

### Tx 11 Tap FIR



### No Rx FFE

# Tx and Rx FFE optimization

- Rx FFE is optimized using Minimum Mean Square Error (MMSE) criteria for any given Tx FIR, channel, xtalk etc.
- The Tx FIR is brute force optimized based on the link SNR.

# Channels

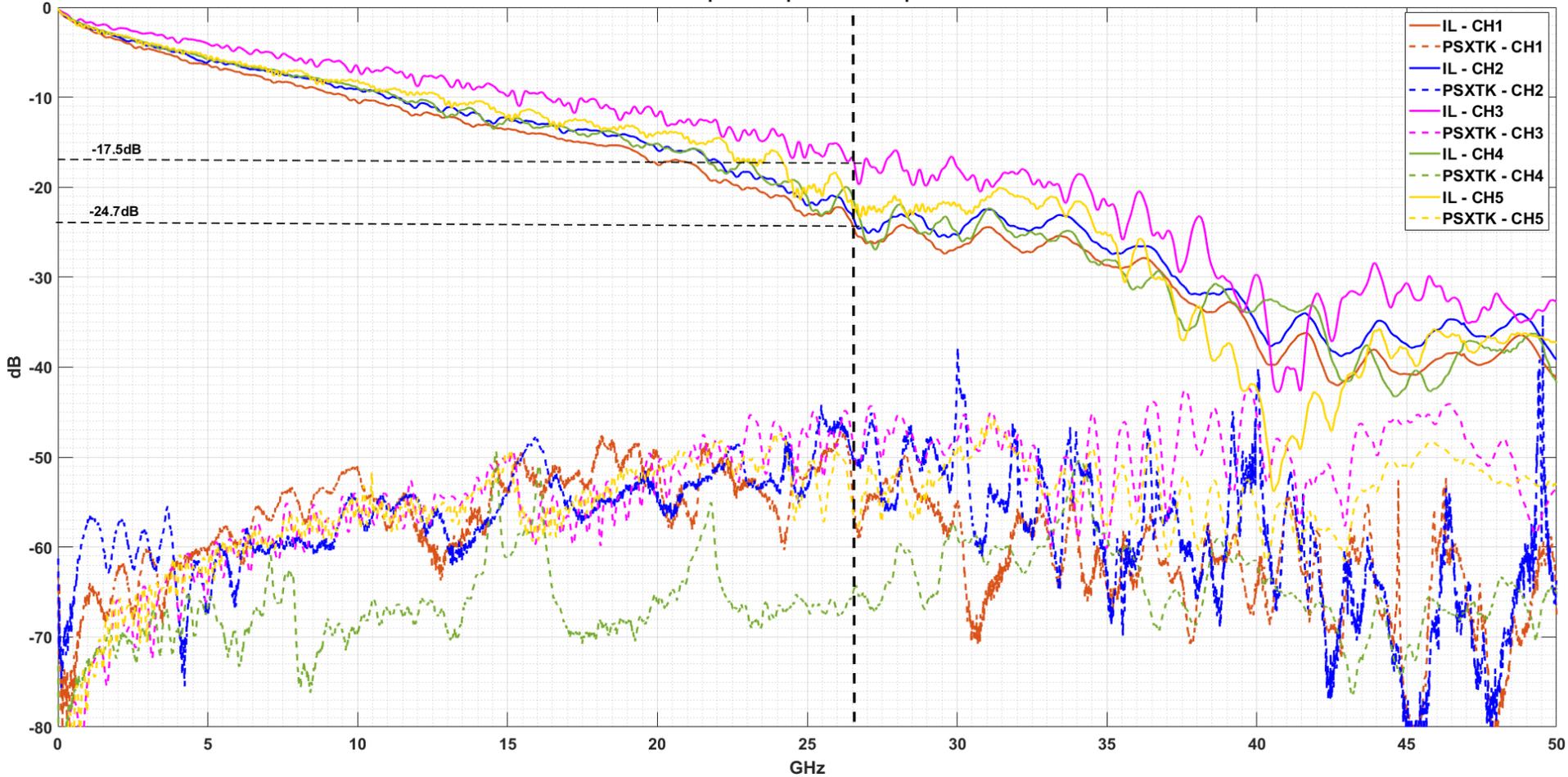
## ■ 5 channels were selected for the analysis

- 16dB C2M channel contribution from lim\_3ck\_01\_0918 (referred to CH1)
  - Spokane contribution
- 14dB C2M channel contribution from lim\_3ck\_01b\_0718 (referred to as CH2)
- Customer proprietary channel (referred to as CH3)
- Channel contribution from tracy\_100GEL\_06\_0118 (referred to CH4)
  - OIF Micro-via case
- Channel contribution from mellitz\_3ck\_02\_0518 (referred to CH5)
  - 14dB BC-BOR-N-N-N

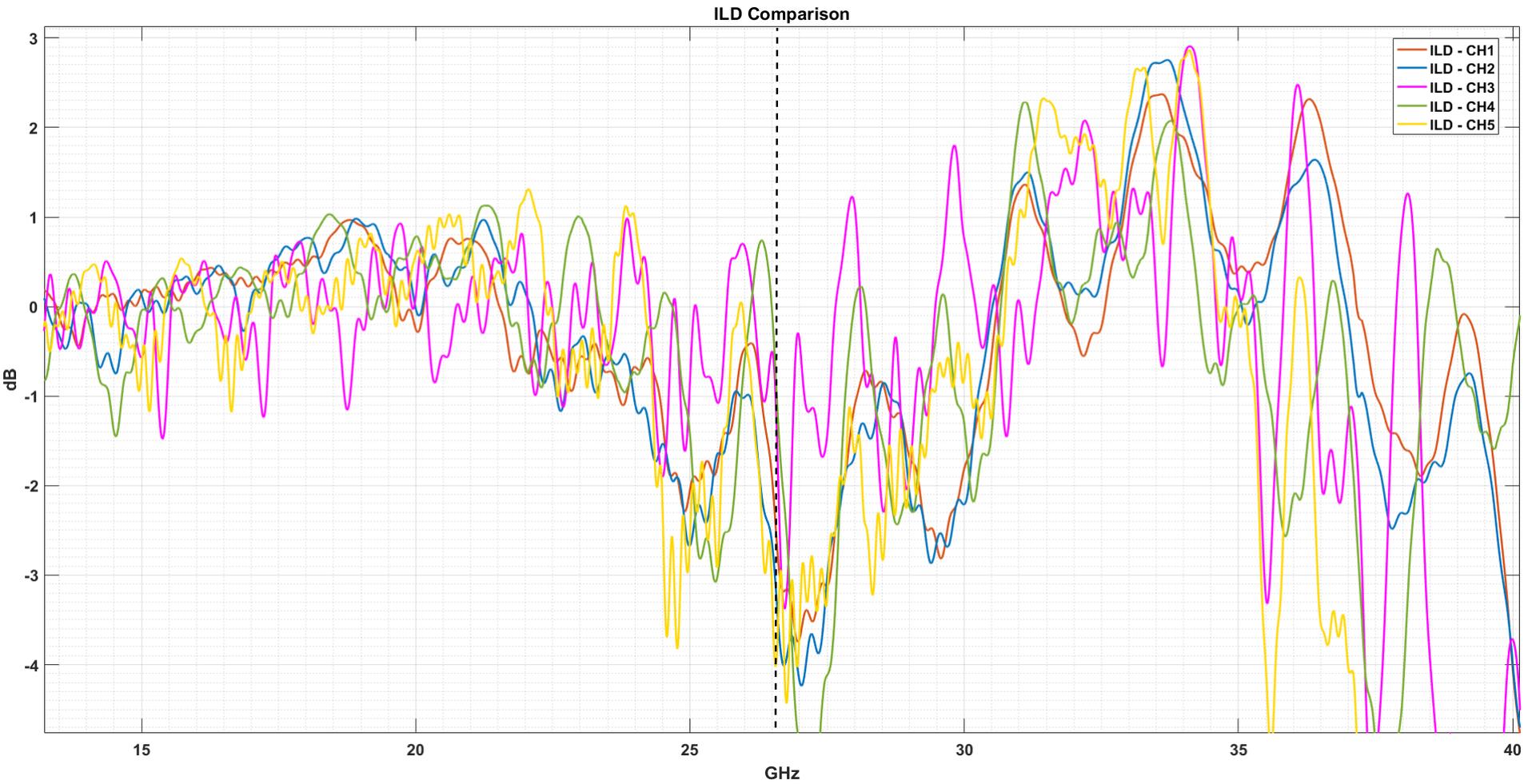
## ■ Package models and die models

- Channel above include cascade of both PKG and Die models for Thru and Xtalk channels
- No PKG cross-talk is included in the simulations
- Uses a 30mm host package design from current customer
- Uses a 4mm package design from current product indicative of 100G devices
- Uses a ~130fF equivalent load for the die

# Bump to bump channel frequency response



# ILD Comparison



# SNR Simulation Results

			Channel - 1	Channel - 2	Channel - 3	Channel - 4	Channel - 5
IL @ Nyq (dB)			24.7	23.4	17.2	21.4	22.9
ILDMax (upto Nyq ) dB			4.8	5.2	4.2	4.7	5.5
Architecture	Configuration		SNR (dB)				
11T TX FFE (2Pre) → RX CTLE/VGA → Tail DFE	#Tail DFE	0	19.3	19.8	19.3	18.8	18.7
	#Tail DFE	16	19.7	20.8	21.1	19.5	19.2
4T TX FFE (2Pre) → RX CTLE/VGA → 6T RX FFE (2 Pre) → Tail DFE	#Tail DFE	0	19.4	19.4	21.8	20.5	20.2
	#Tail DFE	16	22.4	23.5	23.8	21.6	22.5

## ■ Note:

- Rx FFE without DFE has shorter span in the simulations (covers upto 3 post + CTLE), compared to TX FFE case which has upto 8 post taps + CTLE

# Summary

- TX FFE heavy architecture shows worse SNR compared to RX FFE
  - The noise at various input blocks of the receiver was included based on analog simulations
  - 19.5dB SNR is not sufficient to close system budgets to account for tolerances, and yield
  - A brute force search on TX FFE is not a practical solution and does not address background adaptation
- Rx FFE based architecture is more robust under the various channels studied (lossy, reflective, etc)
- A detailed implementation of the RX FFE based architecture and TX FFE based architecture shows only a 10% power delta between the 2 cases in 7nm process
  - Assumes a Tail DFE is present in the receiver