System Complexity/Cost Tradeoffs of Single-Duplex vs. Dual-Duplex schemes

IEEE 802.3ck 100 Gb/s per Lane Electrical Task Force

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Nov 2018

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- 100Gbps/lane signaling pushes the bandwidth limits for the electrical components required in a proper system design close to 30GHz
  - Many signal integrity challenges arise at frequencies > 15GHz
  - Traces, cables, and connectors all need to provide very low loss up to 10s of GHz
  - Additionally, the differential nature of the link puts further restriction for the matching between the traces.
- Look at a comparison of requirements for designing robust systems for 100Gbps/lane signaling using Single-Duplex vs. Dual-Duplex schemes

100Gbps SD/DD Challenges & Risks

100Gbps SD at 53Gbaud

- New materials
  - Significant cost increase 2-3x (e.g. Tachyon 100)
  - Surface roughness challenges at >14GHz
  - Long term laminate reliability → delamination issues
  - Production yields concerns → further cost increase
- New Connectors
  - Significant higher cost to support wide BW=0-27GHz
  - New topologies with new risks (e.g. Flyover)
  - Not resilient to temperature & mechanical changes
- Long Reach Challenges
  - Cabling objective of at least 2m too challenging
    - Even if possible, will require very thick cables
  - Longer reach distances than OIF
    - Leveraging OIF work product unclear
- FEC and Precoding
  - TBD - Still needs to be defined

100Gbps DD at 26.5Gbaud

- Multi-Gbaud Echo cancellation
  - Requires 30-40dB cancellation up to 13.5GHz
  - Proof points
    - 10GBASE-T PHY proved ~60dB cancellation at ~1Gbaud
    - 10GBASE-T1 PHY proved ~40dB cancellation at ~6Gbaud
- Echo Canceller Power Consumption
  - 10GBASE-T PHY Echo canceller high power because
    - ~4000 Echo FIR taps
    - 10-bit input data (THP coded)
  - Earlier 100G DD presentations showed (farjadrad_3ck_01b_0918)
    - ~64 FIR taps for 2-3m DAC
    - 2-bit input data only
    - ~30x higher baud rate

    } 15% power of 10GBASE-T
- Synchronous Tx/Rx clocking
  - Proven to work successfully in BASE-T PHYs

100Gbps SD/DD Overall Concerns

Concern	100Gbps PAM4 SD	100Gbps PAM4 DD
Precoding and FEC	TBD	Based on 802.3cd
Signal Integrity	Super wide-bandwidth design 0 - 27GHz	Similar to 802.3cd
Cables/PCB Materials Concern	Differential lane skews/Surface roughness	Same Cables/PCB Materials as 802.3cd
Cable/PCB Materials Cost	Thicker cables 2-3x more expensive PCBs than 802.3cd (Megtron-8 or Tachyon 100)	Same Cost as 802.3cd
Connectors Maturity/Robustness	All new design prototypes with no field deployment Sensitivity to mechanical/temp changes at high freq	Same Connectors as 802.3cd
Connectors Cost	Significantly more expensive to support ~30GHz	Same Cost as 802.3cd
Overall System Risk	Totally new systems to support up to ~30GHz New unproven topologies	Leverages same Systems/Topologies as in 802.3cd
Overall System Cost	Significantly more expensive	Similar Cost to 802.3cd

Comparison System Requirements: Dual Duplex vs. Single Duplex Channels

Interface	Architecture	IL @26.5GHz Bump to Bump	IL @13.3GHz Bump to Bump	100Gbps PAM4 SD	100Gbps PAM4 DD
Chip to Module	Conventional 10” PCB + Module	28dB	14dB	Practical	Practical
	Internally Cabled Host + Module	23dB	14dB	Practical	Practical
Chip to Chip	Conventional PCB + Mezz Connector	48dB	28 dB	Impractical	Practical
	Internally Cabled Host + Mezz Conn	28-38dB	19-24dB	Limited	Practical
Backplane	1m Conventional PCB	68dB	34 dB	Impractical	Practical
	Cabled Backplane	28-43dB	14-22dB	Very Limited	Practical
Copper Cable	Conv 3m DAC + Host PCB	50dB	30dB	Impractical	Practical
	Internally Cabled Host + DAC	28-38dB	19-24dB	Limited	Practical

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