

PCS, FEC and PMA Baseline Proposal

IEEE P802.3ck

January 2019

Long Beach

Mark Gustlin – Cisco

Pete Anslow – Ciena

Gary Nicholl - Cisco

Shawn Nicholl – Xilinx

Dave Ofelt – Juniper

Kapil Shrikhande – Innovium

Jeff Slavick - Broadcom

Supporters

- Rob Stone – Broadcom
- Mark Nowell – Cisco
- Pirooz Tooyserkani - Cisco

Introduction

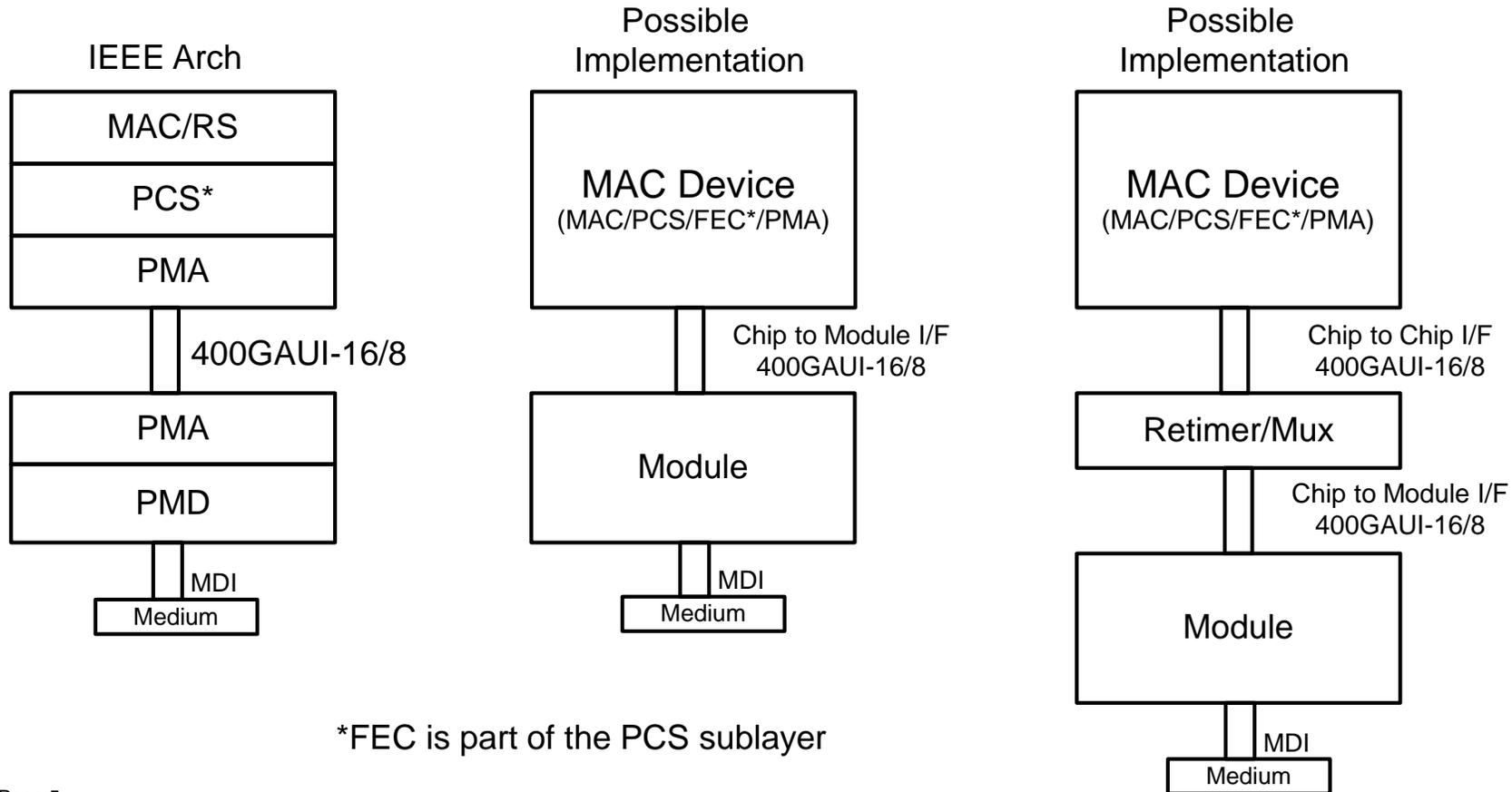
- This describes a possible PCS/FEC/PMA baseline proposal for the various Ethernet speeds covered by the 802.3ck task force
- It proposes to reuse existing PCS/FEC/PMA sublayers that have been defined in 802.3bs and 802.3cd for many of the interfaces
- For the most difficult interfaces at 100GbE, it adds a new FEC sublayer that interleaves two RS(544,514) codewords

Previous Work

- [gustlin_3ck_01_0518.pdf](#), proposes re-use of the 802.3bs and 802.3cd PCS/FEC/PMA sublayers in this project
- [anslow_3ck_adhoc_01_072518.pdf](#), initial FEC performance analysis
- [gustlin_3ck_01_0718.pdf](#), proposes a possible RS symbol muxing scheme in the PMA sublayer, this is no longer being considered
- [anslow_3ck_01_0918.pdf](#), updated FEC performance analysis
- [gustlin_3ck_01_1118.pdf](#), proposes a new interleaved FEC sublayer for the most difficult channels at 100GbE
- [anslow_3ck_01_1118.pdf](#), analyses the interleaved FEC performance
- [nicholl_3cn_01b_181211.pdf](#), proposes baseline for CGMII extender

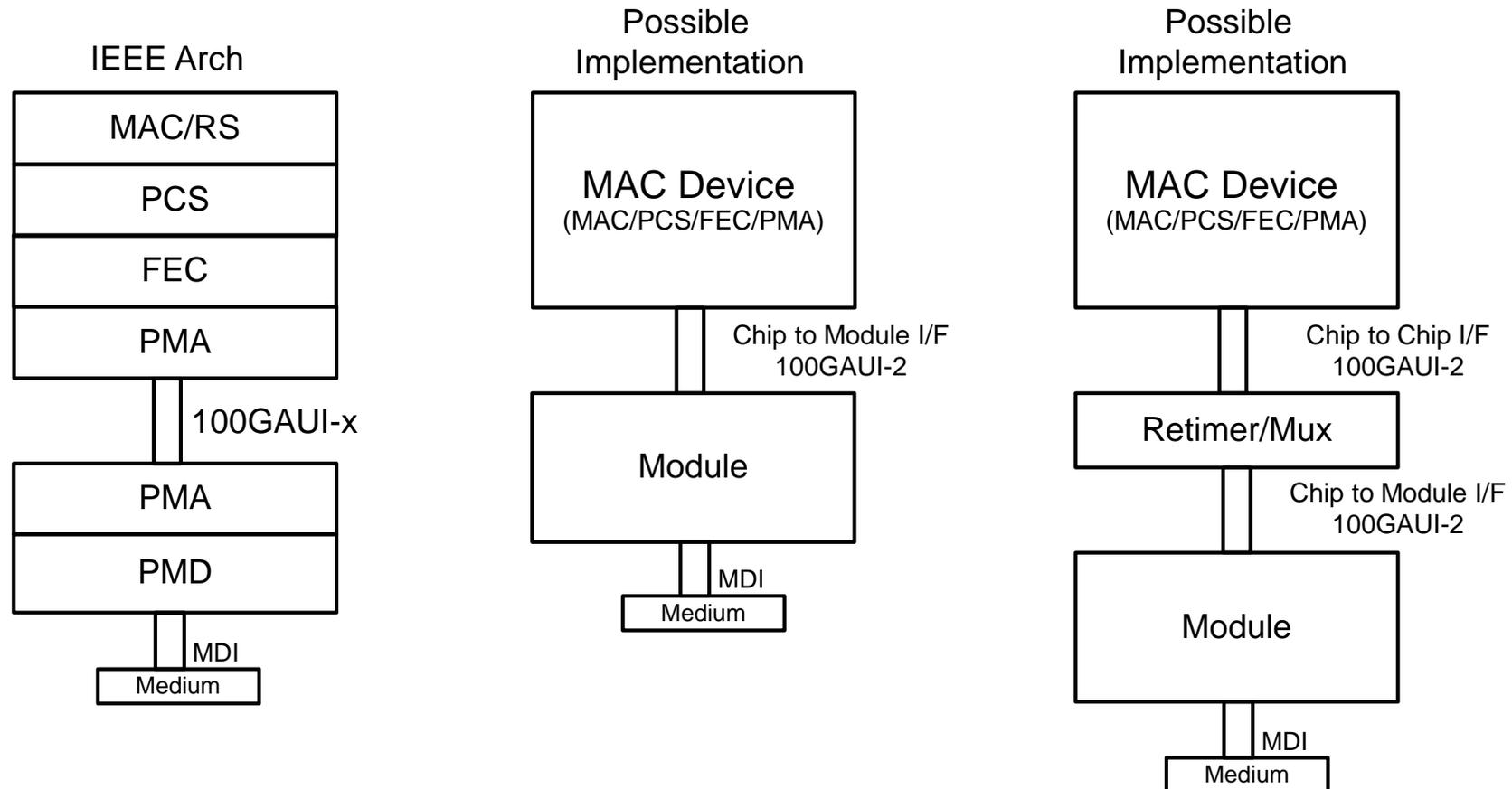
802.3bs Architecture – 200GbE and 400GbE

- Adopted architecture and possible implementations are shown below for 400GbE
 - 200GbE is identical except for # lanes and MAC rate
- FEC is part of the PCS sublayer utilizing the RS(544,514) aka “KP4” FEC code.
- An extender sublayer is also defined



802.3cd Architecture – 100GbE

- Adopted architecture and possible implementations are shown below for 100GbE
- FEC is in the FEC sublayer, RS(544,514) aka “KP4” FEC
 - An AUI may exist between the PCS and FEC sublayers



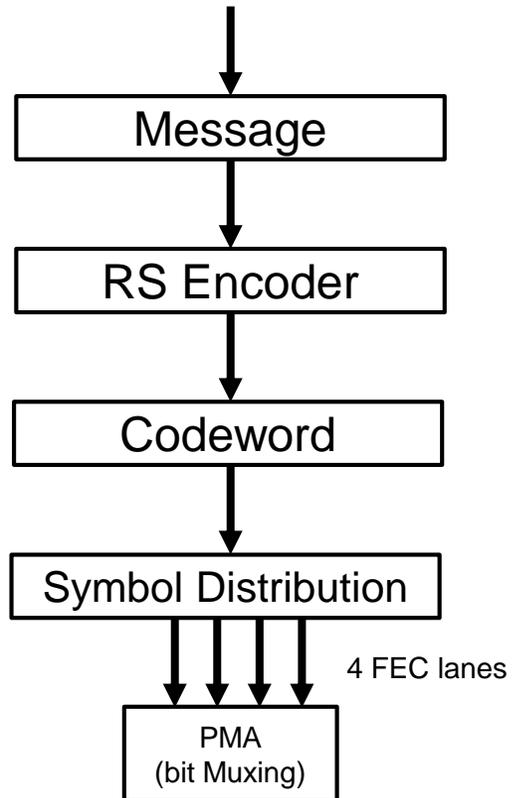
Proposal

- For 200GbE and 400GbE, adopt the 802.3bs Extender, PCS and PMA sublayers including the RS(544,514) FEC code for use in 802.3ck project
 - Clauses 118-120
- For 100GBASE-CR and 100GBASE-KR PHYs, adopt the 802.3cd PCS, a new 2:1 interleaved FEC sublayer based on RS(544,514) and the 802.3cd PMA sublayers for 100GbE
 - Clause 82, a new interleaved FEC clause, clause 135
- For the 100GbE C2M, C2C and all other related PHYs, adopt the PCS, FEC and PMA used in 802.3cd, including the RS(544,514) FEC code for use in 802.3ck project
 - Clauses 82, 91, 135
- Adopt the CGMII Extender Sublayer (100GXS) as proposed in 802.3cn
- Add all 802.3ck AUIs and copper/backplane PHYs to the list of interfaces with precoding capability
 - As in 802.3cd, PMA output lanes must support capability; PMA input lanes optional to implement, optional to enable

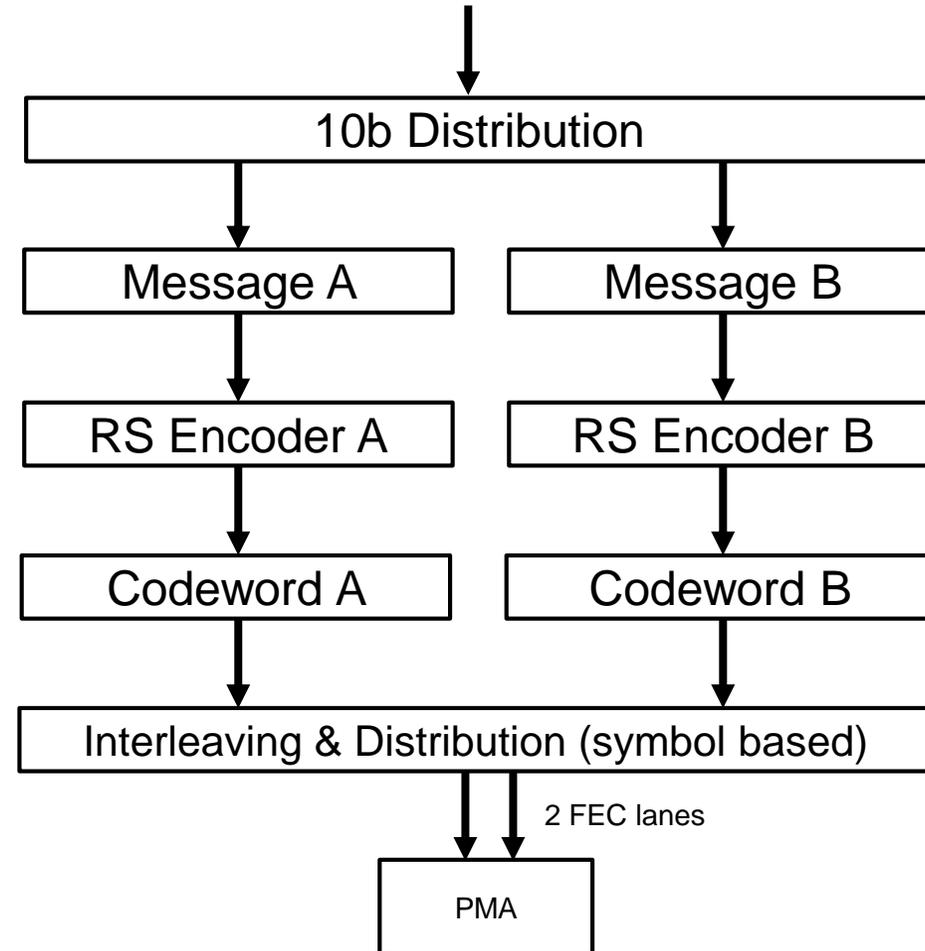
New 100GbE Interleaved FEC Sublayer

- Based on 2x50G RS(544,514) FEC interleaving, similar to 802.3bs

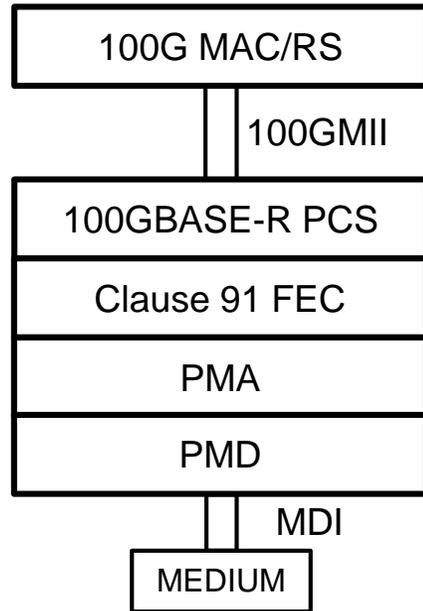
A portion of today's Clause 91 FEC



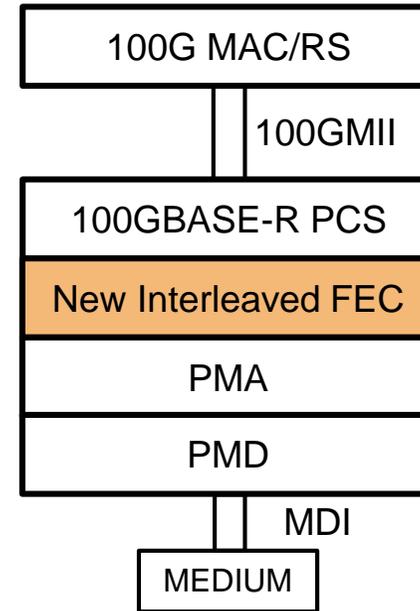
A portion of a possible new FEC sublayer



Proposed 100GbE FEC Sublayer Architectural View

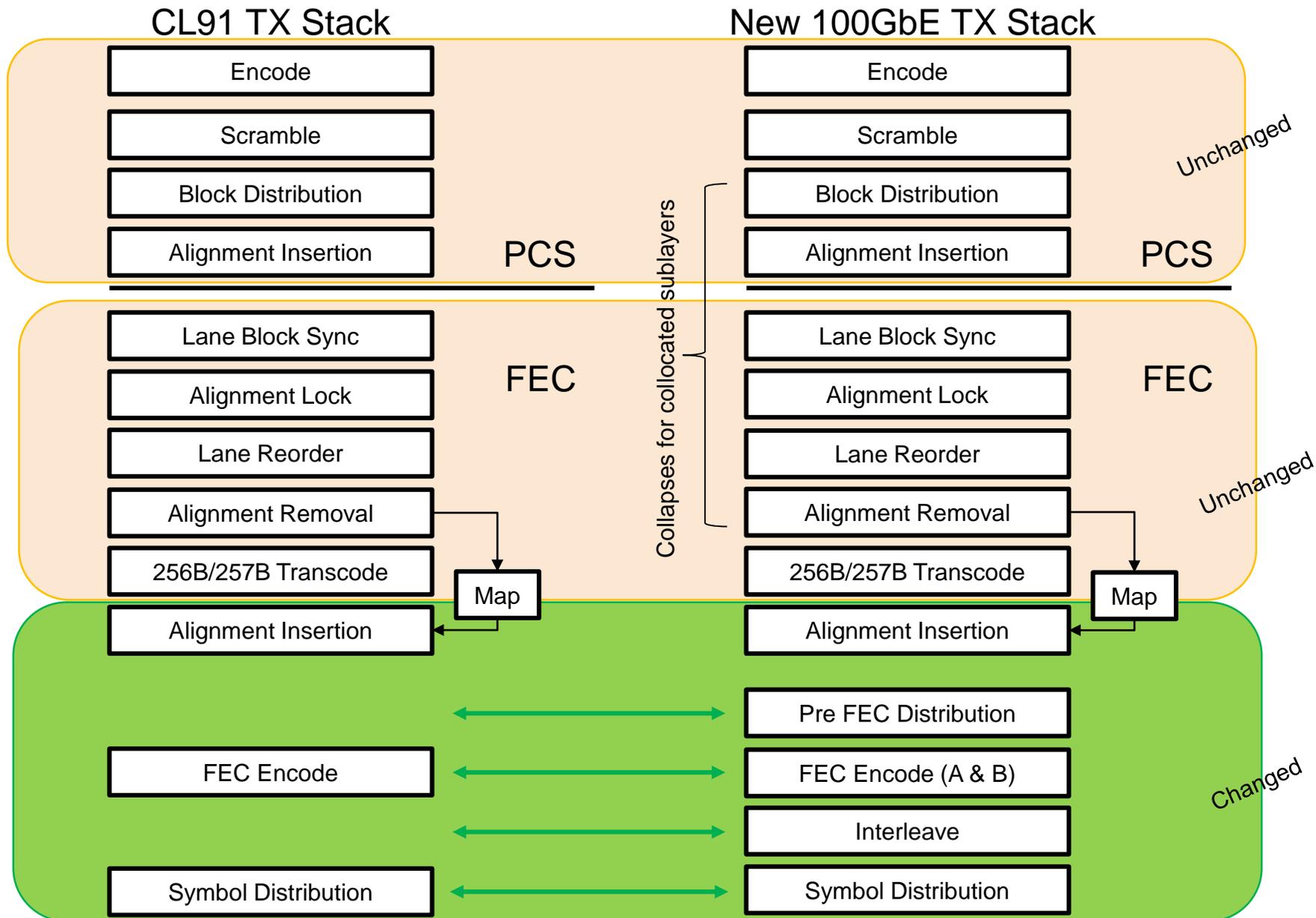


100GBASE-DR
C2M/C2C I/F



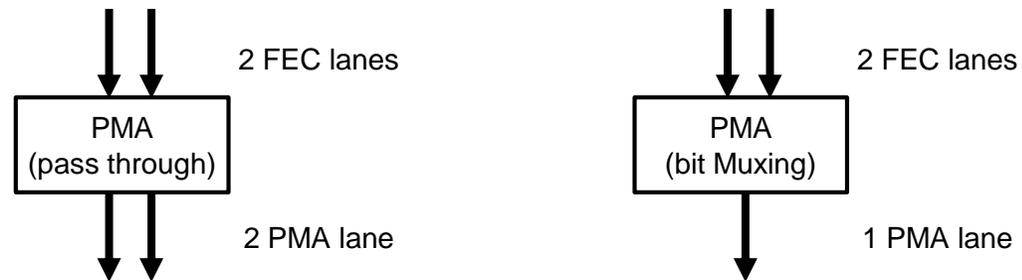
100GBASE-KR
100GBASE-CR

New Interleaved Protocol Stack Comparison with CL91



PMA for the New 100GbE FEC Sublayer

- PMA can be used as a pass through (2x53G)
- Or to bit mux down to a single lane (1x106G)
- Simple bit muxing
- Re-use of Clause 83



Alignment Markers for Interleaved 100GbE FEC

➤ Existing Clause 82/91 Marker Format

FEC lane, <i>i</i>	Reed-Solomon symbol index, <i>k</i> (10-bit symbols)																																				
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33			
0	0	amp_tx_0					63	0	amp_tx_4					63	0	amp_tx_8					63	0	amp_tx_12					63	0	amp_tx_16					63	█	
1	0	amp_tx_1					63	0	amp_tx_5					63	0	amp_tx_9					63	0	amp_tx_13					63	0	amp_tx_17					63		
2	0	amp_tx_2					63	0	amp_tx_6					63	0	amp_tx_10					63	0	amp_tx_14					63	0	amp_tx_18					63	↑	
3	0	amp_tx_3					63	0	amp_tx_7					63	0	amp_tx_11					63	0	amp_tx_15					63	0	amp_tx_19					63	↑	

█ = 5-bit pad

↑ tx_scrambled

Figure 91-4—Alignment marker mapping to FEC lanes

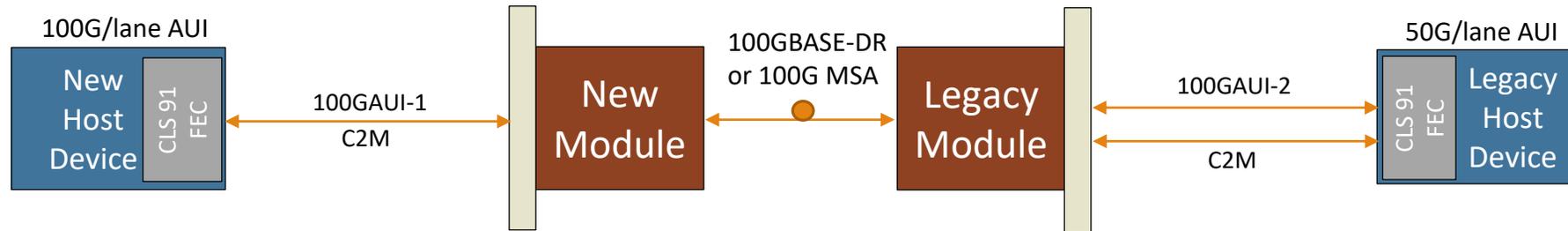
➤ Proposed New Interleaved Marker Format (supporting two FEC lanes)

- amp_tx_0 = am0, amp_tx_1 = am0, amp_tx_2 = am2 etc.
- No repetition at the end of the AM block

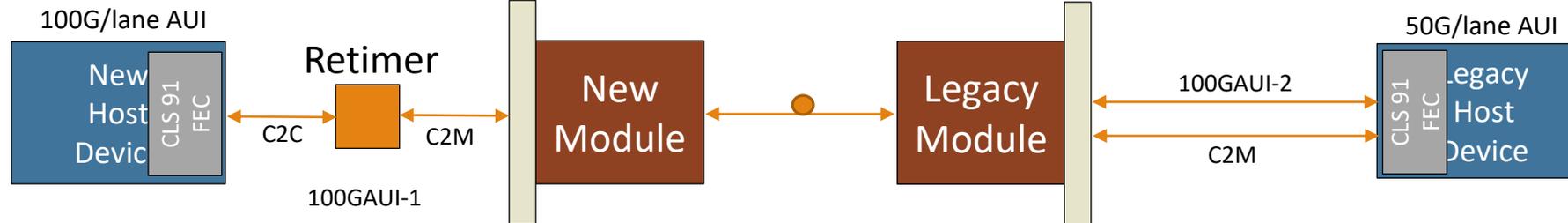
FEC Lane, <i>i</i>	Reed-Solomon symbol index, <i>k</i> (10-bit Symbols)																																					
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33				
0	amp_tx_0					amp_tx_2					amp_tx_4					<u>000</u>											amp_tx_16					amp_tx_18					█	
1	amp_tx_1					amp_tx_3					amp_tx_5																amp_tx_17					amp_tx_19						

100GbE Example Use Cases - Optical

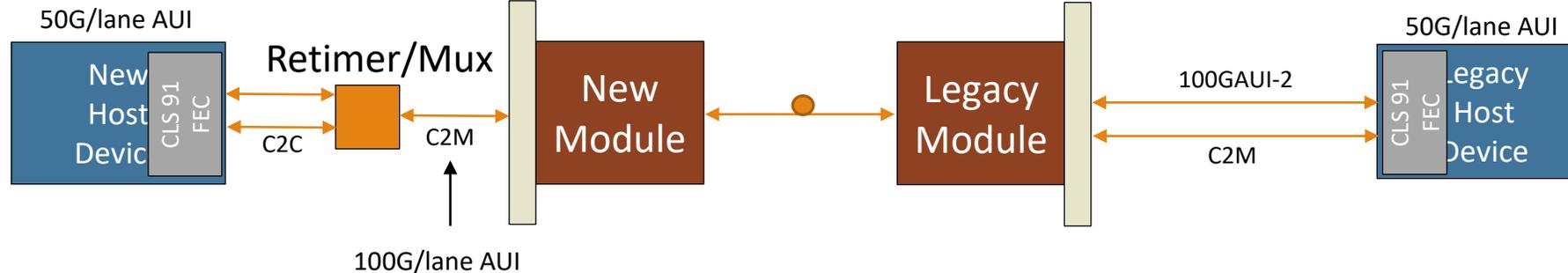
Seamless Clause 91 FEC end to end, backwards compatible



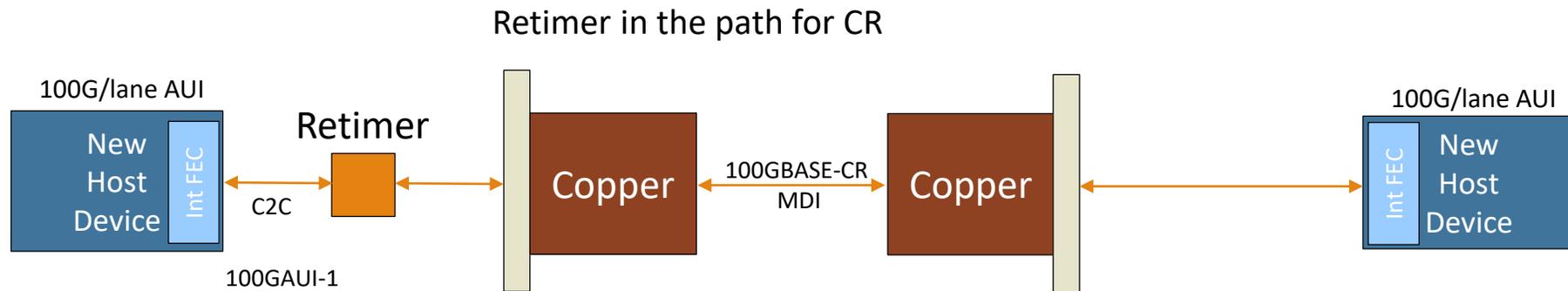
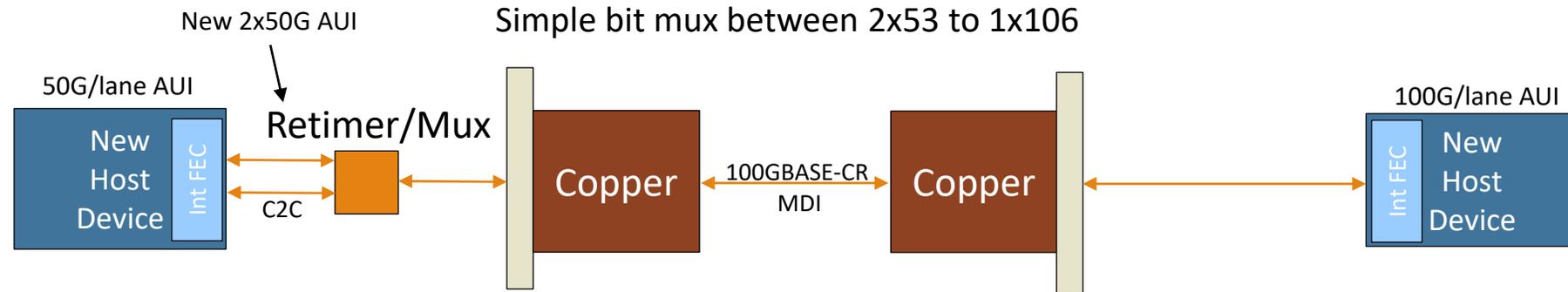
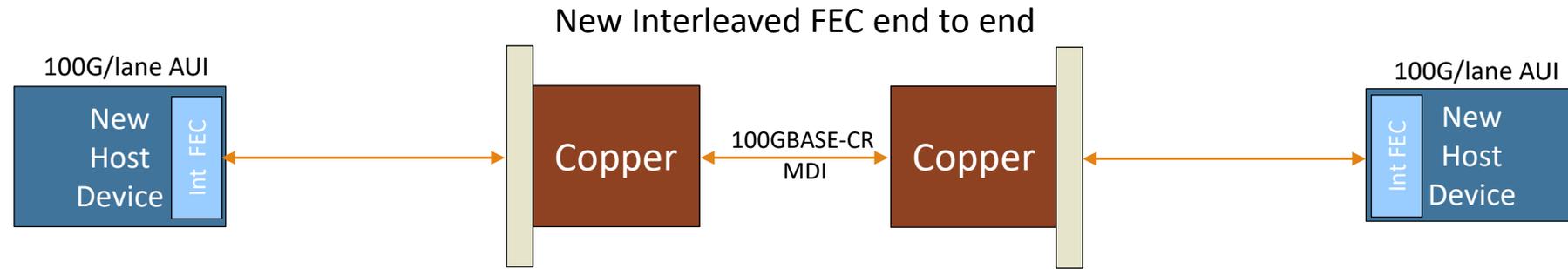
Retimer to 100G AUI-1, backwards compatible



Retimer/mux to 100G AUI-1, backwards compatible

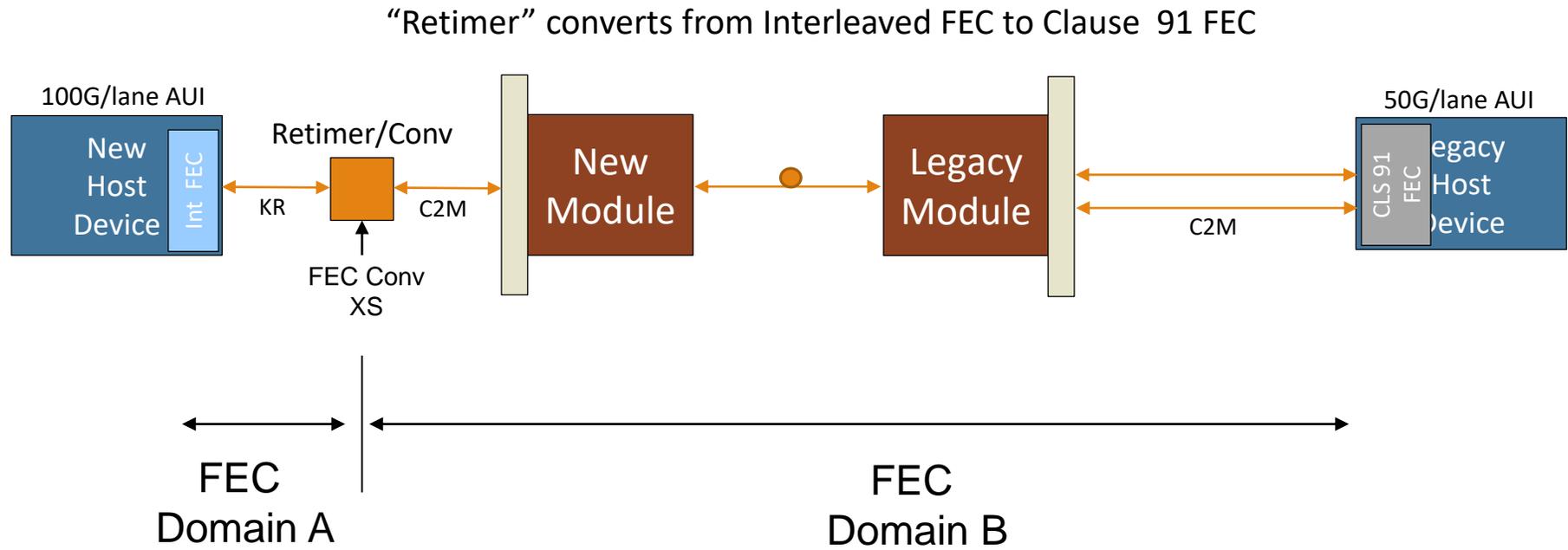


100GbE Example Use Cases – Copper



100GbE Example Use Cases – With an XS

- A CGMII Extender (proposed in 802.3cn) can be used for this scenario



Conclusion

- Once sufficient simulations and other work is done to show that the RS(544,514) FEC is sufficient for the 802.3ck channels, adopt these slides as the baseline for the PCS/FEC/PMA sublayers, including the new interleaved FEC sublayer

Thanks!