



Latency Concerns on Interleaved FEC for 100G-KR/CR

Ilya Lyubomirsky, Arash Farhoodfar, Karthik Gopalakrishnan, Jamal Riani,
Yu Liao, and Sudeep Bhoja, Inphi Corp.

IEEE P802.3ck Task Force Meeting, Jan. 2019

Summary

- A new interleaved RS(544,514) FEC has been proposed in `gustlin_3ck_01_0119` for mitigating potential burst error issues in 100G-KR/CR systems based on multi-tap DFE Rx architectures
- Some analysis has been provided in `anslow_3ck_01_0918` showing BER error flaring can occur in multi-tap DFE Rx architectures when DFE taps are sufficiently large (e.g. 5-tap DFE [0.7,0,0.2,0,0.2]), and `anslow_3ck_01_1118` showed that interleaved FEC can improve the performance for some cases considered
- A major disadvantage of interleaved FEC is a significant increase of the FEC latency. This may be an important issue for latency sensitive systems based on 100G-KR/CR
- Alternative solutions exist: the burst error issue can be solved by limiting the DFE tap values (as shown in `anslow_3ck_01_0119`), and/or implementing Rx architectures which are not prone to burst error problems
- We show simulation results for 100G SerDes that successfully closes 100G-KR link with FFE and 1-tap DFE Rx

Interleaved FEC Latency

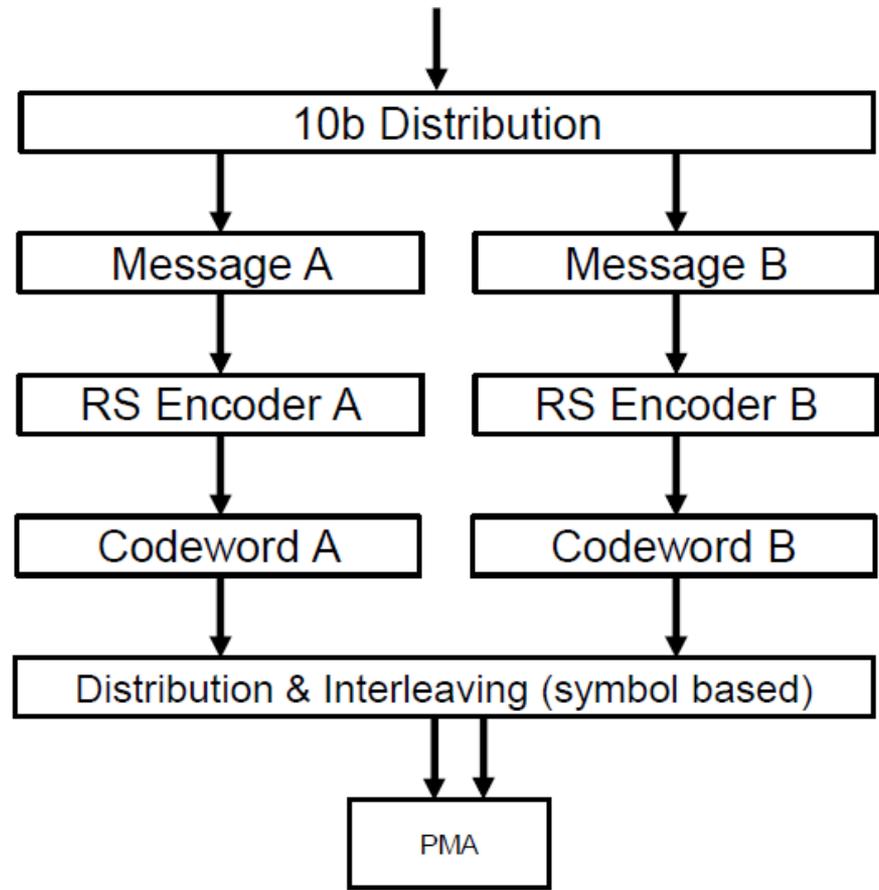
Latency estimate in gustlin_3ck_01_1118

Current Clause 91 RS544

Latency	Contributor
51ns	Block time
50-100ns	Processing*
101-151ns	Total

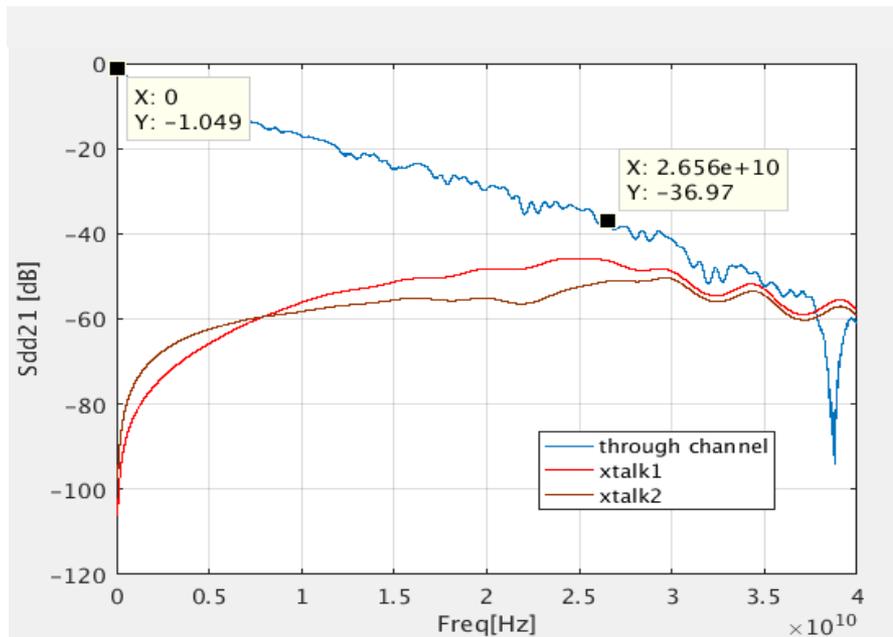
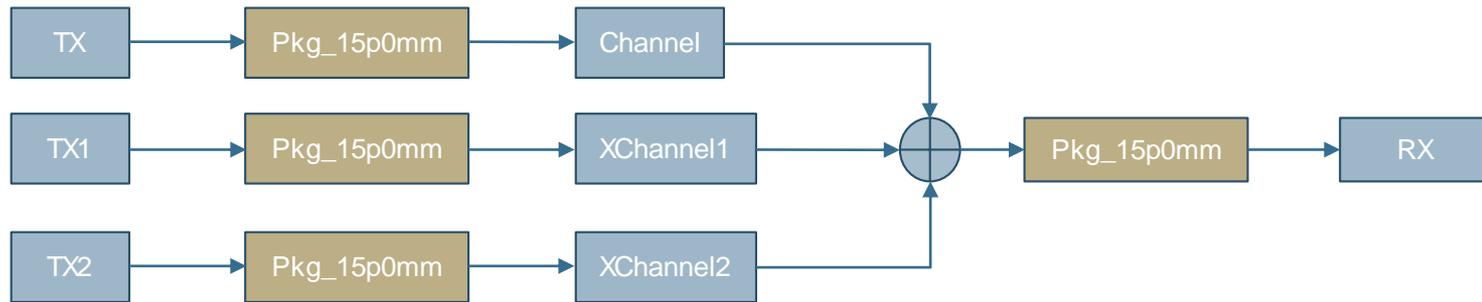
Potential RS544 Interleaved

Latency	Contributor
102ns	Block time
50-150ns	Processing*
152-252ns	Total



*depends on parallelism/latency tradeoffs

100G-KR Channel Simulation Results PAM4 53 Gbaud



- 15mm PKG model is cascaded at both ends of the through and cross channels.
- Total channel insertion loss $\sim 36\text{dB}$ @ Nyquist.
- TX swing = 800mV.

	FFE + 1-tap DFE	Longer FFE + 1-tap DFE
BER	5.5e-4	5.5e-6
DFE Tap	0.7	0.7

Recommendation

- Preferable not to burden 100G-KR/CR system designs by significantly increasing FEC latency with interleaved FEC
- Alternative solutions exist by imposing constraints on DFE tap values and/or implementing Rx architectures which are not prone to burst error problems
- More work is needed before making a decision on adopting interleaved FEC for 100G-KR/CR