Updated TP1-TP4 QSFP-DD 2m Reach Channel



Tom Palkert, Alex Haser, Scott Sommers tpalkert1@gmail.com

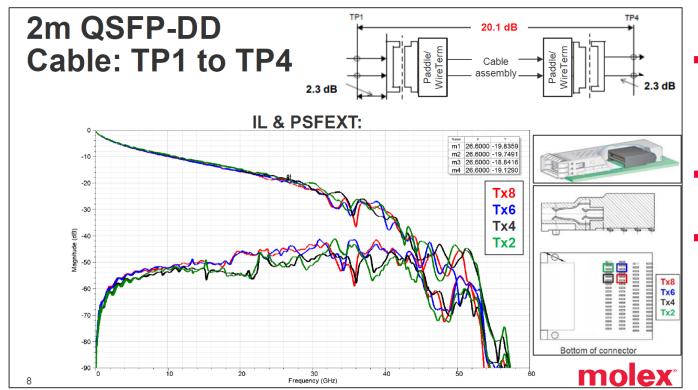


Overview:

- Previously provided data on QSFP-DD:
 - Brief review of QSFP-DD contributions
- For the updated model (see subsequent slides):
 - Nominal bulk cable model was replaced with an improved model
 - This bulk cable model includes manufacturing variation
 - This s-parameter has been made available for public use
- TP0-TP5 Loss Budget



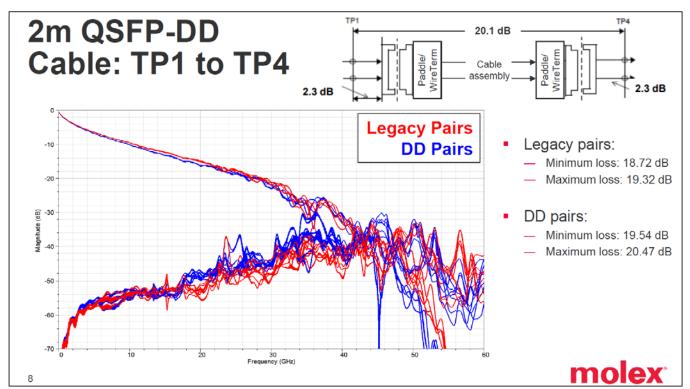
From haser_3ck_adhoc_01_021219: Partial 2m QSFP-DD TP1-TP4 Channel



- Max loss from simulation: 19.84 dB (only includes 2 bottom rows of connector)
- Proposed TP1-TP4 budget: 20.1 dB
- PSXT curves include contributions from 3 FEXT aggressors & 0 NEXT aggressors



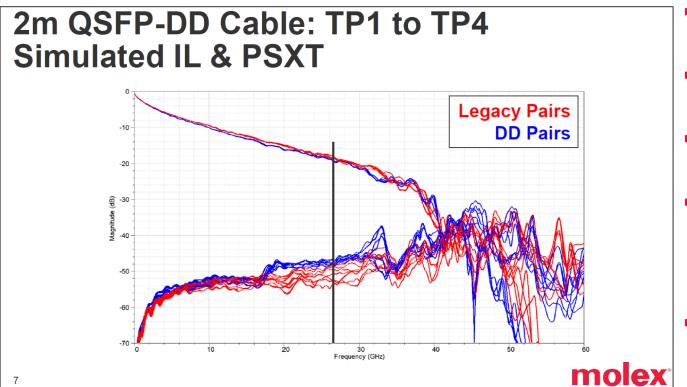
From palkert_3ck_01_0319: Full 2m QSFP-DD TP1-TP4 Channel



- Max loss from simulation: 20.47 dB
- Proposed TP1-TP4 budget: 20.1 dB
- PSXT curves include contributions from 7 FEXT aggressors & 8 NEXT aggressors
- Worst case COM (Version 2.58)*: 3.531 dB



From palkert_3ck_01_0519: Updated 2m QSFP-DD TP1-TP4 Channel



- Max loss from simulation: 19.5 dB
- Proposed TP1-TP4 budget: 20 dB
- Improved wire termination model
- PSXT curves include contributions from 7 FEXT aggressors & 8 NEXT aggressors
- Worst case COM (Version 2.58)*:3.728 dB



S-Parameter Model

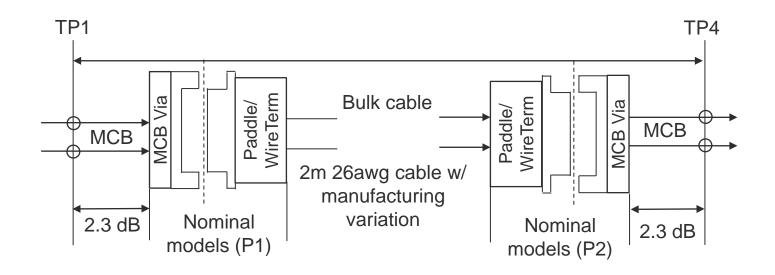


Model Information:

- This model captures:
 - Manufacturing variation in bulk cable
 - Connector and wire termination models are nominal
- Frequency content:
 - 50 MHz-60 GHz
 - 10 MHz steps
- See next slides for topology

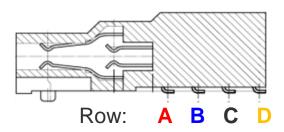


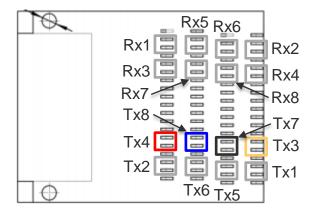
Topology:





Files Provided:





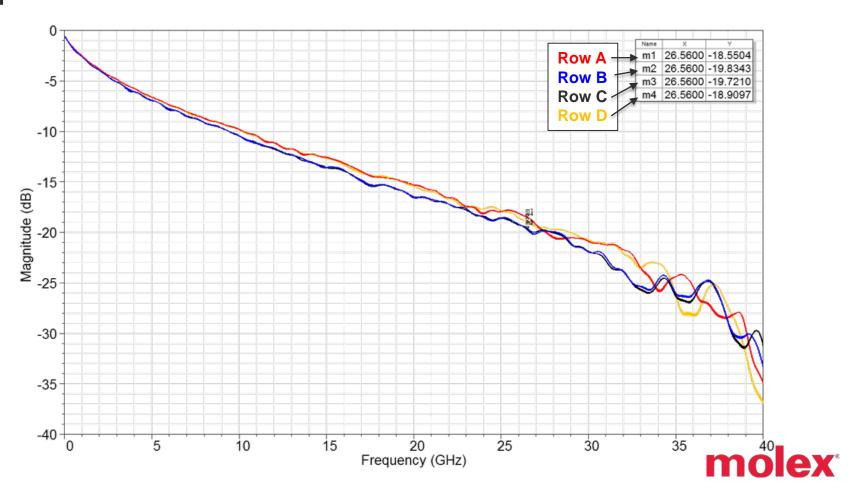
Bottom of P1 connector

- For each row:
 - One THRU victim pair s4p
 - 7 FEXT s4ps
 - 8 NEXT s4ps
 - 16 files per row
- 64 total files provided

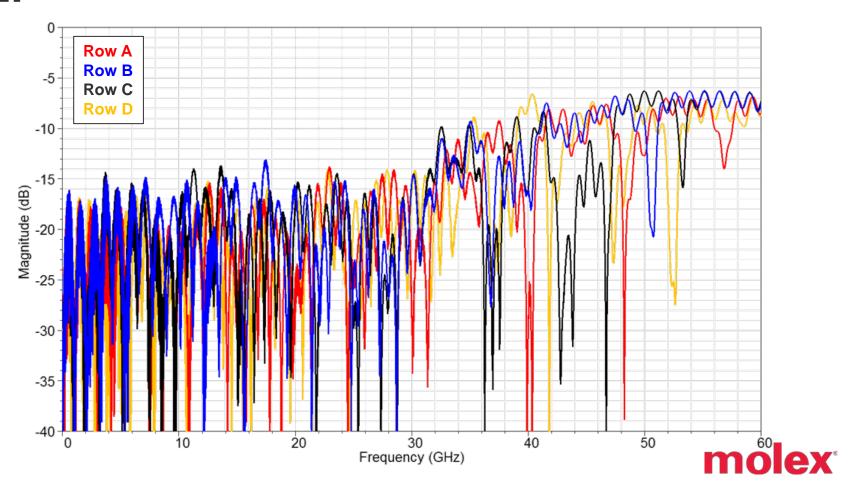
Note: Cables crossover from P1 connector to P2 connector (e.g. Tx4 P1 connects to Rx4 P2)



IL:

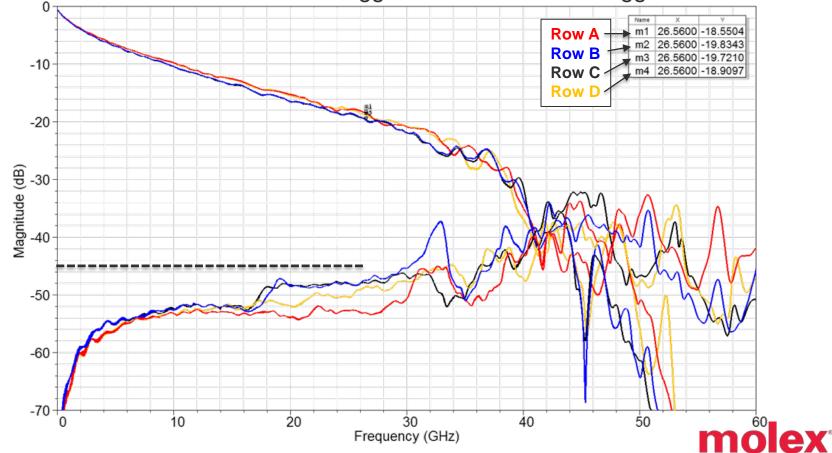


RL:



IL & PSXT:

Each PSXT curve contains contributions from 7 FEXT aggressors and 8 NEXT aggressors



Row B COM Results:

Ran on Row B data (most lossy pair)

COM Version	IL (dB)	ERL11	ERL22	FOM _{ILD}	ICN (mV)	ICN _{NEXT} (mV)	ICN _{FEXT} (mV)	COM (dB)
2.6	29.280	11.781	12.020	0.724	0.583	0.313	0.492	3.622
2.6 (see Note)	28.977	11.781	12.020	0.721	0.598	0.325	0.502	3.675

COM 2.60 config: config_com_ieee8023_93a=100GEL-CR_030119 NOTE: PCB length changed from 92.7mm to 90 mm (to hit 29 dB IL) (See back up slides for config sheets)



Summary:

- Previously supplied nominal data on QSFP-DD estimated TP1-TP4 loss to be 19.84 dB
- Bulk cable design was improved and expected manufacturing variation was added to it
 → Maximum TP1-TP4 channel loss is 19.83 dB
- 20 dB is needed for the TP1-TP4 budget to realistically support 2m reach objective
- 29dB is needed to support the 20 dB TP1-TP4 budget

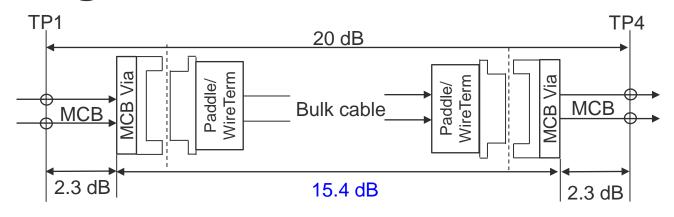


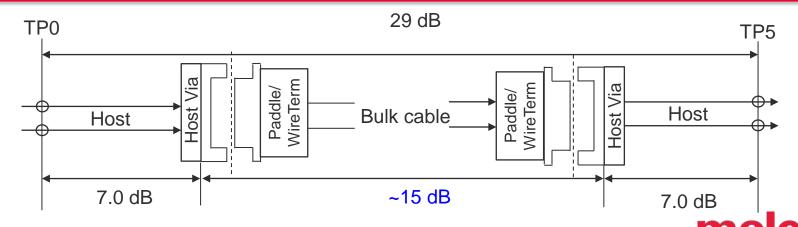


TP0-TP5 Budget:

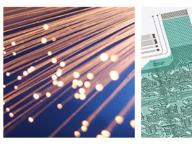


Loss Budget:









Back Up



Original:

	Table 93A-1 parameters	I/O control				
Parameter	Setting	Units	Information	DIAGNOSTICS	0	logical
f_b	53.125	GBd		DISPLAY_WINDOW	0	logical
f_min	0.05	GHz		CSV_REPORT	1	logical
Delta_f	0.01	GHz		RESULT_DIR	\results\100GEL_WG_{dat	e}\
C_d	[1.1e-4 1.1e-4]	nF	[TX RX]	SAVE_FIGURES	1	logical
z_p select	[2]		[test cases to run]	Port Order	[1324]	
z_p (TX)	[12 32; 1.8 1.8]	mm	[test cases]	RUNTAG	CR_eval_	
z_p (NEXT)	[12 32; 1.8 1.8]	mm	[test cases]	COM_CONTRIBUTION	0	logical
z_p (FEXT)	[12 32; 1.8 1.8]	mm	[test cases]	Operational		
z_p (RX)	[12 32; 1.8 1.8]	mm	[test cases]	COM Pass threshold	3	dB
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]	ERL Pass threshold	10.5	dB
R_0	50	Ohm		DER_0	1.00E-04	
R_d	[50 50]	Ohm	[TX RX]	T_r	6.16E-03	ns
A_v	0.413	V	vp/vf=.694	FORCE_TR	1	logical
A_fe	0.413	V	vp/vf=.694	Include PCB	1	logical
A_ne	0.608	V		TDR and ERL options		
L	4			TDR	1	logical
M	32			ERL	1	logical
	filter and Eq			ERL_ONLY 0		logical
f_r	0.75	*fb		TR_TDR 0.01		ns
c(0)	0.54		min	N 1000		
c(-1)	[-0.34:0.02:0]		[min:step:max]	TDR_Butterworth	1	logical
c(-2)	[0:0.02:0.12]		[min:step:max]	beta_x	1.70E+09	
c(-3)	[-0.06:0.02:0]		[min:step:max]	rho_x	0.25	
c(1)	[-0.1:0.05:0]		[min:step:max]	fixture delay time	0	enter sec
N_b	24	UI		Receiver testing		
b_max(1)	0.85			RX_CALIBRATION	0	logical
b_max(2N_b)	0.3			Sigma BBN step	5.00E-03	V
g_DC	[-20:1:0]	dB	[min:step:max]	Noise, jitter		
f_z	21.25	GHz		sigma_RJ 0.01		UI
f_p1	21.25	GHz		A_DD 0.02		UI
f_p2	53.125	GHz		eta_0 8.20E-09		V^2/GHz
g_DC_HP	[-6:1:0]		[min:step:max]	SNR_TX 33		dB
f_HP_PZ	0.6640625	GHz		R_LM	0.95	

	Table 93A–3 parameters								
	Parameter	Setting	Units						
T	package_tl_gamma0_a1_a2	[0 0.0009909 0.000	2772]						
٦	package_tl_tau	6.141E-03		ns/mm					
┪	package_Z_c	[87.5 87.5 ; 92.5 9	2.5]	Ohm					
\forall									
\dashv	Table 92–12 parameters								
\dashv	Parameter	Setting							
\dashv	board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]							
_	board_tl_tau	6.200E-03		ns/mm					
_	board_Z_c	90	Ohm						
_	z_bp (TX)	92.7		mm					
	z_bp (NEXT)	92.7		mm					
	z_bp (FEXT)	92.7		mm					
	z_bp (RX)	92.7		mm					
- 1									



Modified:

Table 93A-1 parameters					I/O control			
Parameter Setting		Units	Information		DIAGNOSTICS	0	logical	
f_b	53.125	GBd		DISPLAY_WINDOW 0		0	logical	
f_min	0.05	GHz		CSV REPORT 1		1	logical	
Delta_f	0.01	GHz			RESULT_DIR			
C_d	[1.1e-4 1.1e-4]	nF	[TX RX]		SAVE_FIGURES	1	logical	
z_p select	[2]		[test cases to run]		Port Order			
z_p (TX)	[12 32; 1.8 1.8]	mm	[test cases]		RUNTAG	CR_eval_		
z_p (NEXT)	[12 32; 1.8 1.8]	mm	[test cases]	COI	M_CONTRIBUTION	0	logical	
z_p (FEXT)	[12 32; 1.8 1.8]	mm	[test cases]		(Operational		
z_p (RX)	[12 32; 1.8 1.8]	mm	[test cases]	CO	M Pass threshold	3	dB	
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]	ER	ERL Pass threshold		dB	
R_0	50	Ohm			DER_0	1.00E-04		
R_d	[50 50]	Ohm	[TX RX]		T_r	6.16E-03	ns	
A_v	0.413	V	vp/vf=.694		FORCE_TR	1	logical	
A_fe	0.413	V	vp/vf=.694		Include PCB	1	logical	
A_ne	0.608	V		TDR and ERL options				
L	4				TDR	1	logical	
M	32				ERL	1	logical	
filter and Eq					ERL_ONLY	0	logical	
f_r	0.75	*fb			TR_TDR	0.01	ns	
c(0)	0.54		min		N	1000		
c(-1)	[-0.34:0.02:0]		[min:step:max]	ax] TDR_Butterworth		1	logical	
c(-2)	[0:0.02:0.12]		[min:step:max]	beta_x 1.70		1.70E+09		
c(-3)	[-0.06:0.02:0]		[min:step:max]	nax] rho_x		0.25		
c(1)	[-0.1:0.05:0]		[min:step:max]	fi	xture delay time	0	enter sec	
N_b	24	UI		Receiver testing		ceiver testing		
b_max(1)	0.85			R	X_CALIBRATION	0	logical	
b_max(2N_b)	0.3			9	Sigma BBN step	5.00E-03	V	
g_DC	[-20:1:0]	dB	[min:step:max]	Noise, jitter		Noise, jitter		
f_z	21.25	GHz			sigma_RJ	0.01	UI	
f_p1	21.25	GHz		A_DD 0.02		0.02	UI	
f_p2	53.125	GHz			eta_0	8.20E-09	V^2/GHz	
g_DC_HP	[-6:1:0]		[min:step:max]	nax] SNR_TX 33		33	dB	
f_HP_PZ	0.6640625	GHz		R_LM 0.95		0.95		

Table 93A–3 parameters								
Parameter		Units						
package_tl_gamma0_a1_a2	[0 0.0							
package_tl_tau	6.141E-03			ns/mm				
package_Z_c	ackage Z c [87.5 87.5 ; 92.5 92.5]							
Table 92–12 parameters								
Parameter								
board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]							
board_tl_tau	6.200E-03			ns/mm				
board_Z_c	90			Ohm				
z_bp (TX)	90		mm					
z_bp (NEXT)		90		mm				
z_bp (FEXT)		90		mm				
z_bp (RX)		90		mm				

