

Electrical PMD measurements: What About Test Fixtures

Rich Mellitz, Samtec

Adee Ran, Intel

Liav Ben-Artzi, Marvell Semiconductor

(Additional authors from consensus group)

June 10, 2020, IEEE 802.3 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force Ad Hoc

Focus Group Participants & Contributors

This presentation summarizes thoughts, feedback and recommendations of a group of contributors in multiple teleconference sessions:

- ❑ Matt Brown, Huawei Technologies Canada
- ❑ Piers Dawe, Mellanox
- ❑ Howard Heck, Intel
- ❑ Phil Sun, Credo
- ❑ Rich Mellitz, Samtec
- ❑ Adee Ran, Intel
- ❑ Liav Ben-Artzi, Marvell Semiconductor

Problem statement

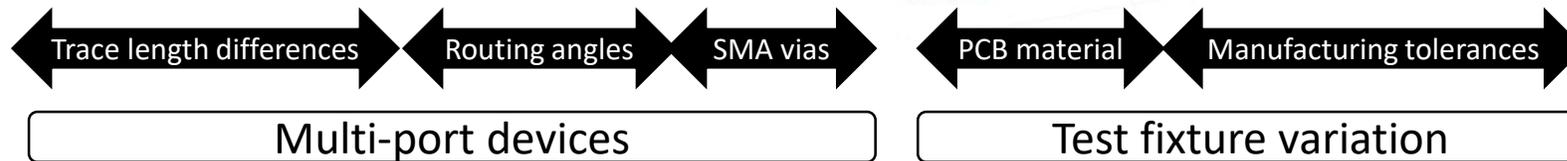
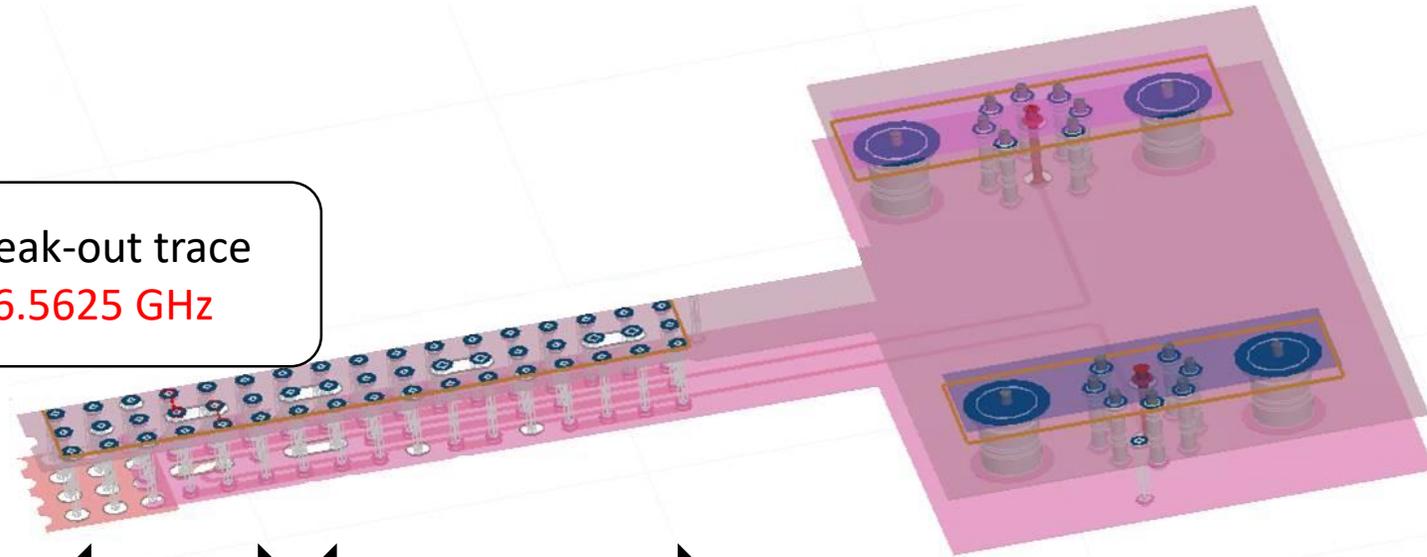
❑ As presented in [mellitz 3ck 01a 0120](#)

(“Practical Device Test Fixtures for 100G KR ... or Not and the Impact on ERL and P max /V f”)

- Test fixtures introduce offset and variability
- Accounting for practical test fixture variability test dwarfs the limit we would want set
- Recommend: Specify transmitter at a TP0 and receiver at TP5

Why Throw Away the “Good-Old method” of specs at TP0a?

Even with high quality material, ~2.4mm via → break-out trace from an internal ball → μvia to SMA $\geq 3\text{dB}$ @ 26.5625 GHz



- ❑ These inaccuracies makes TP0-TP0a highly implementation and manufacturing dependent → results will vary
- ❑ “Can’t you de-embed the fixture?!”
- ❑ Just thinking:

It is easier to *measure* a test fixture than to *de-embed* it!

The focus group dealt with the following

- ❑ Identify parameters which are “straightforward”, don’t require a sophisticated simulation/calculation
- ❑ How we have reached spec limits for measured parameters in previous projects
- ❑ How to define normative measurement at an implementation-dependent TP
- ❑ Need to specify limits of a test fixture
- ❑ Need for informative values at TP0 or TP0a

Measurements which do not vary with TP location

Thus, no need to change specs

- ❑ Signaling rate
- ❑ Differential pk-pk voltage (max) Tx disabled/enabled
- ❑ DC common mode voltage (max/min)
- ❑ AC common mode voltage RMS (fixture has low effect)
- ❑ Transmitter steady state voltage (max/min)
- ❑ Transmitter waveform
 - The method for finding Tx FFE taps is independent of TP0-TP0a; actually works even at TP2.
 - See: http://www.ieee802.org/3/cb/public/jan16/mellitz_cb_01a_0116.pdf slide 6-15
C is vector of tap coefficients. P is fitted un-equalized pulse response. R is the fitted equalized pulse response. $C = (R^T * R)^{-1} * R^T * P$.
 - Need to make sure scope CDR can lock → suggested TP0-TP0v loss ≤ 5dB @ 26.5625GHz; $ILD \leq Loss/20$
(2dB ≤ Loss ≤ 5dB → 0.25dB for 5dB loss)
- ❑ SNDR – Tx parameters to be measured on an optimized test board, breakout section is part of the device budget; package/breakout Xtalk is included in measurement

Parameters that should be measured with adjustment to overcome test fixture loss

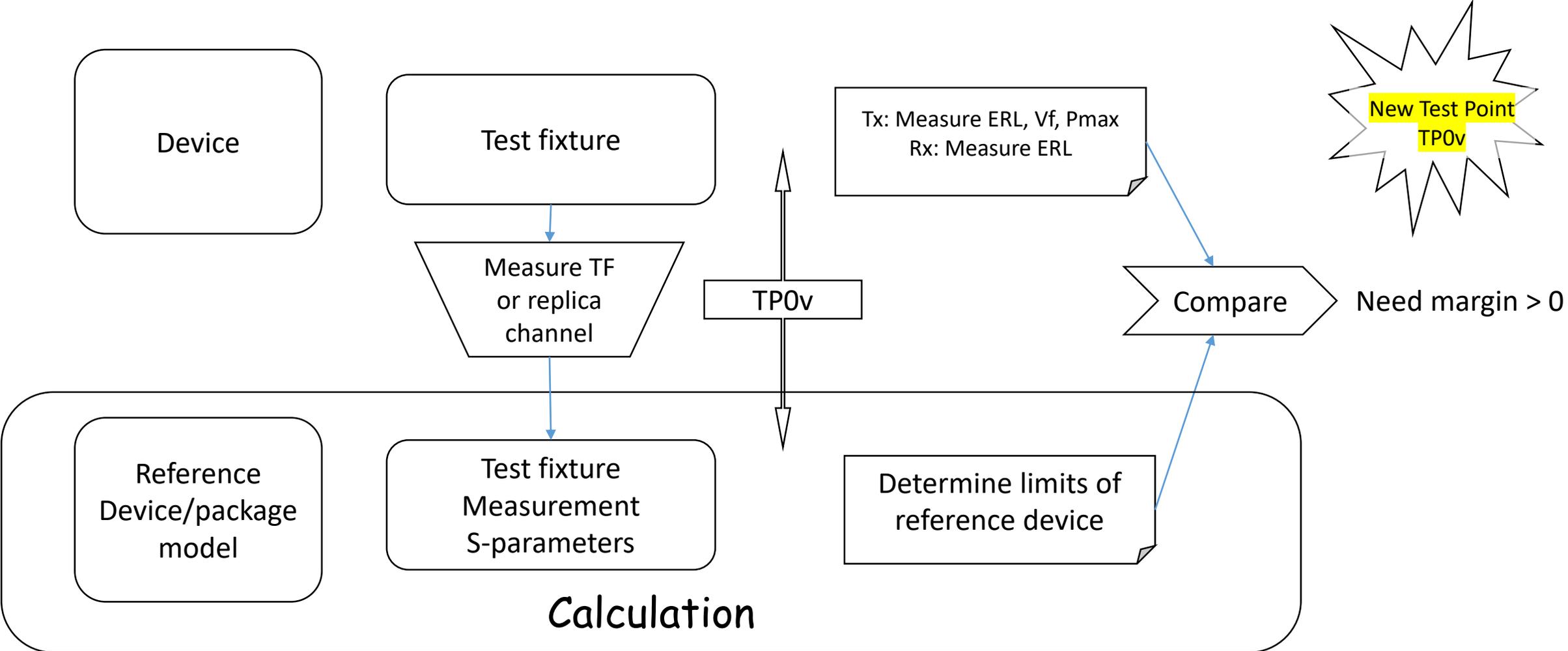
□ Jitter

- In D1.2: “jitter measurements are made with a single transmit equalizer setting selected to compensate for the loss of the transmitter package and TPO to TPOa test fixture”
- Need to be clarified to avoid ambiguity
- Spec limit value can stay unchanged

□ RLM

- In Annex 120D it is under **Output waveform** for which “The state of the transmit equalizer is controlled by management interface “
- Clarify that Tx equalization should be used to get clean level measurements
- Spec limit value can stay unchanged

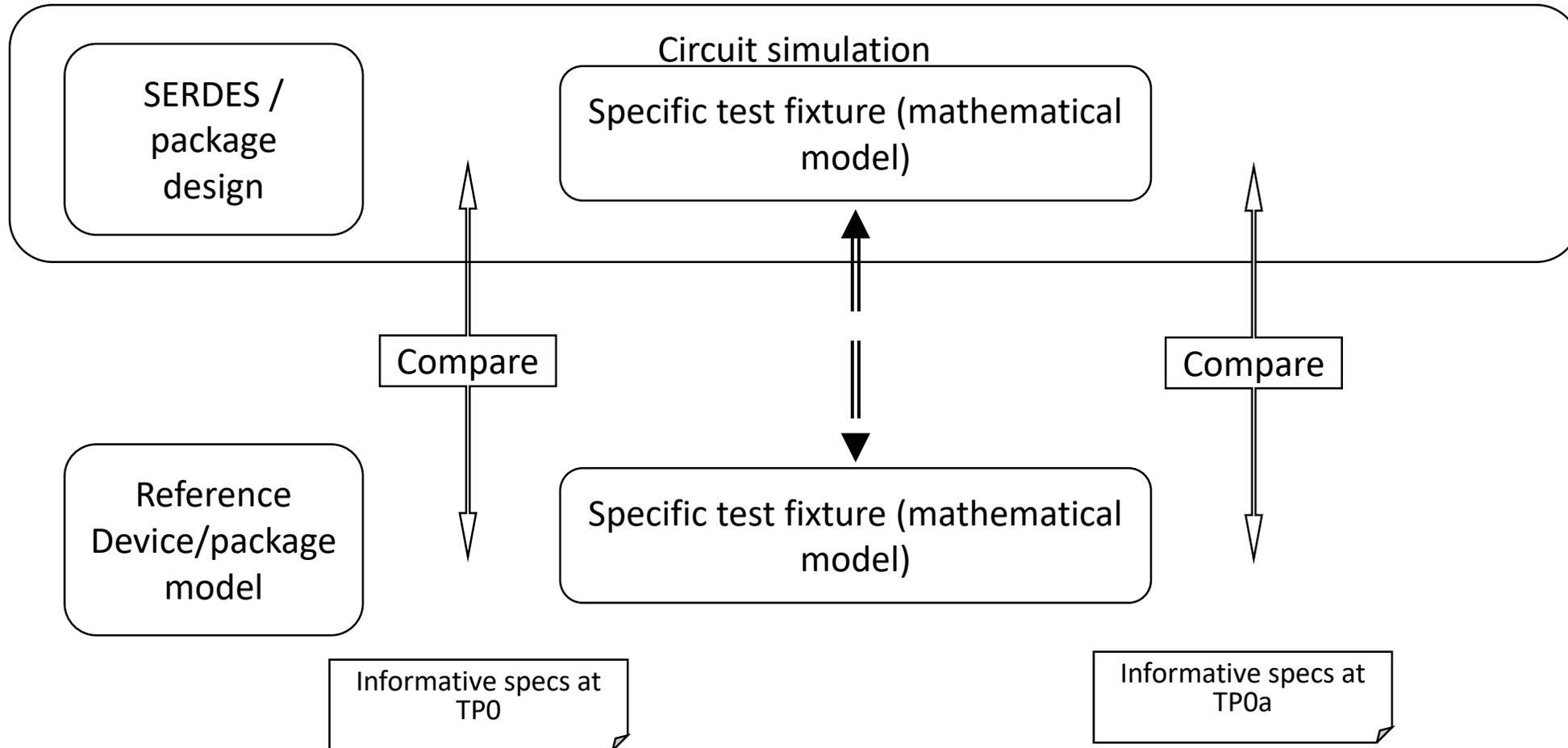
Enabling implementation-dependent test fixture



Proposed new Methodology

- ❑ Measure TP0-TP0v channel (or replica) for the device/lane under test
- ❑ Concatenate Tr filter, Tx reference device and package model, and B-T measurement filter (same equations used in COM)
- ❑ Using the concatenated channel, calculate an output pulse response (with minimum A_v) and TDR at TP0v, with ideal termination
- ❑ Calculate V_f , V_{peak}/V_f , and ERL
 - The results are the expected parameters of the reference Tx at this TP0v
 - This is the bar that the DUT should be compared to!
- ❑ Now measure V_f , V_{peak} , and ERL of the DUT at TP0v using existing method
- ❑ Margin from the calculated reference values → pass/fail

Informative specifications are useful to get things rolling prior to HW availability, or as a reference to validate calculation accuracy



Informative TP0/TP0a values

- ❑ Replace the reference insertion loss of the test fixture in Equation (163–1) with the following equations:

$$IL_{ref}(f) = s_{21}^{(l)}(f)$$
$$RL_{ref}(f) = s_{22}^{(l)}(f)$$

- Where $s_{21}^{(l)}(f)$ and $s_{22}^{(l)}(f)$ are defined in Equation 93A–14 with parameters taken from Table 162–17, and $z_p = 76.5$, representing an insertion loss of 3 dB at 26.5625 GHz.
- ❑ Perform ERL; Linear fit pulse peak analysis to define informative values at reference points (TBD until calculated)
- ❑ Common mode return loss? May be TBD for now

Summary:

- ❑ Change 163.9.1.2 Transmitter normative test fixture requirements to:
 - TP0-TP0v loss $\leq 5\text{dB}$ @ 26.5625GHz
 - ILD magnitude $\leq \text{Loss at } 26.5625\text{GHz} / 20$ ($2\text{dB} \leq \text{Loss at } 26.5625\text{GHz} \leq 5\text{dB}$ → 0.1dB for 2dB loss ; 0.25dB for 5dB loss)
- ❑ Keep current values of parameters specified on slide #6
- ❑ Add subclauses with text based on the notes in slide #7 as clarification for jitter and RLM
- ❑ Add a subclause based on slide #9 explaining how to come up with required limits for test-fixture-dependent parameters
- ❑ Add a reference TP0-TP0a loss model and informative values as described on slide #11

THANK YOU