P802.3ck D3.0 Comment Resolution Clause 162

Howard Heck, Intel
Chris Diminico, MC Communications/PHY-SI LLC/Panduit

Clause/Annex 162

Clause	Topic	Comments
162	TX Residual ISI	237
162	TX SNDR	53, ~~ran_01~~
162	TX ERL	176, 177
162	TX J3u	156, 171, ~~rysin_adhoc_011922~~
162	TX jitter	173, 174, 175, 225
162	TX measurement	224, 49
162	TX quiet mode	[48, 78, 121], [47, 79]
162	TX Rpeak	51, 136, 172
162	TX control	52
162	RX RITT	[179, dawe_01], [54, 124], ~~calvin_01a~~

Clause/Annex 162 CA, 162A, 162B, 162C (Chris/Howard)

Clause	Topic	Comments
162	CR loss budget	[170, dawe_04], 180
162	CA ILcd	57
162	CA RLcc	[181, dawe_04]
162	COM parameter	183
162B	MTF ILdd	[218, ~~dawe_02~~]
162B	PICS	119
162C	MDI table	[1, 120], ~~lusted_01~~

162 TX Residual ISI
237

Cl **162** *SC* **162.9.3** *P* **166** *L* **45** # I-237

Dudek, Michael Marvell

Comment Type **TR** *Comment Status* **D** *Residual ISI*

With the Np=200 value used for the linear fit procedure in the SNDR measurement it is possible that the transmitter can have significant pulse distortions at times beyond the reach of the receiver DFE. These pulse distortions cannot be equalized and could increase the BER unacceptably.

SuggestedRemedy

Add a Residual Intersymbol Interference specification with value -31dB max referring to the test procedure in 163.9.2.6

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The suggested remedy does not provide sufficient evidence to support the proposed changes. Further data or analysis is necessary.
For task force discussion.

Clause 162.9.3 Table 162-10, p 166

Signal-to-noise-and-distortion ratio, SNDR (min)	162.9.3.3	31.5	dB

Suggested remedy:

Signal-to-noise and distortion ratio, SNDR (min)	162.9.3.3	31.5	dB
Residual intersymbol interference, ISI_RES (max)	163.9.2.6	-31	dB

162 TX SNDR
53

Cl **162**	*SC* **162.9.3.3**	*P* **170**	*L* **31**	# I-53

Ran, Adee — Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **D** *SNDR*

The definition of SNDR refers back to 120D which does not state what the Tx equalization should be in this measurement. Based on a previous specification in clause 92, it may be understood that the limit in Table 162–10 applies to any valid equalization setting.

Since transmitters typically have noise sources that are independent of equalization, and applying equalization reduces the pulse peak, it is expected that increasing the "strength" of Tx equalization would degrade the measured SNDR. We can assume equalization settings with c(0) close to 0.5, which would reduce the measured pulse peak by 5-6 dB; this makes the SNDR spec more difficult than it seems.

A related concern is that the noise injected in the receiver ITT is also after Tx equalization (like realistic transmitters), and it is calibrated by measuring SNDR and using the results as TX_SNR. However, TX_SNR in COM represents a white noise source _before_ the Tx equalization, since it should have the same spectrum as the victim signal.

There seems to be a mismatch between the effect of TX_SNR in COM and the effect of SNDR in real links.

This may also affect SNDR and/or SNR_TX in clause 163 and annex 120F, although the receiver test signal is calibrated differently.

SuggestedRemedy

The definition of SNDR and/or the calculation of the effect of SNR_Tx in COM may need to be changed.

A detailed presentation is planned.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
The following related presentation was reviewed by the task force at a previous ad hoc meeting:
https://www.ieee802.org/3/ck/public/22_01/ran_3ck_01_0122.pdf
For task force discussion.

162 TX SNDR
53

Possible changes to the draft

1. Use a modified Equation 93A-30:

$$\sigma_{TX}^2 = \left[H^{(0)}(t_s)\right]^2 10^{-\frac{SNR_{TX}}{10}} \quad \rightarrow \quad \sigma_{TX}^2 = \left[\frac{H^{(0)}(t_s)}{c(0)}\right]^2 10^{-\frac{SNR_{TX}}{10}}$$

   This change amplifies the noise by the reciprocal of c(0) – similar to the effect of c(0) on measured SNDR.

2. Specify SNDR to be measured with equalization off (c(0)=1, to match the definition above).
3. SNDR and SNR_{TX} per case:
   - In Table 162–19, change the value of SNR_{TX} from 32.5 dB to 36.9 dB.
   - In Table 163–11 and Table 120F–8, change the value of SNR_{TX} from 33 dB to 37.4 dB.
   - In Table 162–10, change the value of SNDR (min) from 31.5 dB to 35.9 dB.
   - In Table 163–5 and Table 120F–1, change the value of SNDR (min) from 32.5 dB to 36.9 dB.

Editorial license to be provided for implementing the above in a clean way.

January 2022 802.3ck interim meeting 10

https://www.ieee802.org/3/ck/public/22_01/ran_3ck_01_0122.pdf

162 TX ERL
176

Cl **162** *SC* **162.9.3.5** *P* **172** *L* **13** *#* I-176

Dawe, Piers J G NVIDIA

Comment Type **T** *Comment Status* **D** *TX ERL*

ERL needs a parameter Delta f for the S-parameter measurement. I don't see that it is defined for ERL nor incorporated by reference from COM.

SuggestedRemedy

Add a Delta f entry to all the ERL tables. I suppose the value can be the usual 10 MHz, although for small test fixtures, a larger value might work too.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
Clause 162.9.3.5 states: "Parameters that do not appear in Table 162-13 take values from Table 162-19. Table 162-19 specifies the delta f requirement, which addresses the concern raised by the comment.

162.9.3.5 Transmitter effective return loss (ERL)

ERL of the transmitter at TP2 is computed using the procedure in 93A.5 with the values in Table 162–13. The value of T_{fx} is twice the delay between the test fixture test connector and the test fixture host-facing connection minus 0.2 ns. Parameters that do not appear in Table 162–13 take values from Table 162–19.

Table 162–13—Transmitter and receiver ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.01	ns
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	—
Length of the reflection signal	N	800	UI
Equalizer length associated with reflection signal	N_{bx}	0	UI
Tukey window flag	tw	1	—

Table 162–19—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	53.125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz

162 TX ERL
177

Cl **162** *SC* **162.9.3.5** *P* **172** *L* **19** # I-177

Dawe, Piers J G NVIDIA

Comment Type **T** *Comment Status* **D** *TX ERL*

I wouldn't call this switch or option, a flag with a numerical value. I think it is a parameter, as in functional specifications, and as it is called in 93A.5.1.

SuggestedRemedy

Change flag to parameter, here and in tables 162-18 and 163-6, 163-7, 163-12 and 93A-4. Here and in tables 162-18 and 163-6, 163-7 and 163-12, change 1 to true.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The suggested remedy does not improve the accuracy or clarity of the specified method.
[Editor's note: CC: 93A, 162, 163]

Table 162–13—Transmitter and receiver ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.01	ns
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	—
Length of the reflection signal	N	800	UI
Equalizer length associated with reflection signal	N_{bx}	0	UI
Tukey window flag	tw	1	—

93A.5.1 Pulse time-domain reflection signal

Change the second paragraph of 93A.5.1 as follows:

The filtered return loss, $H_{ii}(f)$, is defined by Equation (93A–58). When the parameter tw is equal to 1, $H_{tw}(f)$ is defined by Equation (93A–58a). When the value of tw is 0 or is not provided by the clause that invokes this method, $H_{tw}(f) = 1$.

Replace Equation (93A–58) as follows:

$$H_{ii}(f) = H_t(f)s_{ii}(f)H_r(f)H_{tw}(f) \qquad (93A–58)$$

Insert new equations (93A–58a) and (93A–58b) after Equation (93A–58):

$$H_{tw}(f) = \begin{Bmatrix} 1 & f \le f_r \\ 0.5\left(1-\cos\left(\dfrac{2\pi(f-f_b)}{f_{per}}\right)\right) & f_r < f \le f_b \\ 0 & f_b < f \end{Bmatrix} \qquad (93A–58a)$$

$$f_{per} = 2(f_b - f_r) \qquad (93A–58b)$$

162 TX J3u
156, 171

Cl **162** *SC* **162.9.3** *P* **166** *L* **47** # I-171

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **D** *TX J3u*

It appears that measured J3u looks bad for measurement reasons. We can choose a different worst jitter corner so that the measurement issues are less important.

SuggestedRemedy

Change J3u max from 0.115 UI to 0.125 UI here, from 0.106 UI to 0.115 in Table 163-5, and from 0.118 UI to 0.128 UI in Table 120F-1. In all three COM tables, change A_dd from 0.02 to 0.0185, change Jrms from 0.1 to 0.115. Alternatively, change the measurement method.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
For task force discussiong, pending task force presentation.
Resolve in conjunction with comment #156.

Cl **162** *SC* **162.9.3** *P* **166** *L* **47** # I-156

Rysin, Alexander NVIDIA

Comment Type **TR** *Comment Status* **D** *TX J3u*

J3u is strongly affected by limitations of measurement equipment. A performance metric that is less subject to measurement issues should be explored. Presentation will follow.

SuggestedRemedy

J3u max from 0.115 UI to 0.125 UI here, from 0.106 UI to 0.115 in 163 and 120F. In COM tables, change A_dd from 0.02 to 0.0185, change Jrms from 0.1 to 0.115. Alternatively, change the measurement method.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
For task force discussiong, pending task force presentation.

Table 162-10

0.125

Output jitter (max)			
J_{RMS}	162.9.3.4	0.023	UI
J3u	162.9.3.4	0.115	UI
Even-odd jitter, pk-pk	162.9.3.4	0.025	UI

0.0115?

Table 162-19

Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI

0.185

Table 163-5

0.115

Jitter (max)[c]			
J_{RMS}	162.9.3.4	0.023	UI
J3u	162.9.3.4	0.106	UI
Even-odd jitter, pk-pk	162.9.3.4	0.025	UI

Table 120F-1

0.115

Output jitter			
J_{RMS} (max)	120F.3.1.3	0.023	UI
J4u (max)	120F.3.1.3	0.118	UI
Even-odd jitter (max)	120F.3.1.3	0.025	UI

Note: Cross-clause with 163 and 120F.

https://www.ieee802.org/3/ck/public/adhoc/jan19_22/rysin_3ck_adhoc_01_011922.pdf

162 TX Jitter
173

Cl **162** *SC* **162.9.3.4** *P* **170** *L* **49** # I-173

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **D** *TX jitter*

Something as vague and open-ended as "may be set lower than 4 MHz" isn't acceptable in a standard. How much lower, how close should the frequency points be? How many attempts must the tester try before he can fail a bad part?
Also, lowering the CRU corner frequency is not needed if PRBS9Q is used, because PRBS9Q is 16 times shorter than PRBS13Q.

SuggestedRemedy

Change
The corner frequency of the clock recovery unit (CRU) may be set lower than 4 MHz.
to
If the test pattern is PRBS13Q, the corner frequency of the clock recovery unit (CRU) is set to 4 MHz as in 120D.3.1.8.2, or 1 MHz.
Add informative NOTE saying that the measured even-odd jitter is expected to be the same or lower with 1 MHz than with 4 MHz.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient justification to support the proposed changes.
For task force discussion.

Clause 162.9.3.4, p 170

Even-odd jitter is calculated using the measurement method specified in 120D.3.1.8.2. with the following exceptions:

a) The test pattern is either PRBS13Q or alternatively PRBS9Q. PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only one pattern is sufficient.

b) The corner frequency of the clock recovery unit (CRU) may be set lower than 4 MHz. Meeting the even-odd jitter requirement with only one CRU bandwidth is sufficient.

NOTE—If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter may not be correctly observed.

Suggested remedy

b) If the test pattern is PRBS13Q, the corner frequency of the clock recovery unit (CRU) is set to 4 MHz as in 120D.3.1.8.1, or 1 MHz.

NOTE—The measured even-odd jitter is expected to be the same or lower with.1 MHz than 4 MHz..

162 TX Jitter
174, 175

Cl **162** *SC* **162.9.3.4** *P* **170** *L* **52** # I-174

Dawe, Piers J G NVIDIA

Comment Type **T** *Comment Status* **D** *TX jitter*

This says "NOTE—If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter may not be correctly observed." If the measurement sees the wrong EOJ, the reported J3u and Jrms will be off, too.

SuggestedRemedy

Delete "even-odd"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
EOJ is a sub-component of J3u and Jrms so it makes sense that with the wrong pattern the latter two would be different. The question is whether it is significant.
Also to address comment #175, change "may" to "might".
Replace the note with the following:
"NOTE—If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter might not be correctly observed. As a result, the observation of J3u and Jrms might also be affected."
For task force disussion.

Cl **162** *SC* **162.9.3.4** *P* **170** *L* **52** # I-175

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **D** *TX jitter*

"may not be" is troublesome. As "The word may is used to indicate a course of action permissible within the limits of the standard (may equals is permitted to)", "may not" means is not permitted to.

SuggestedRemedy

Change "may not be correctly observed" to "might be incorrectly observed".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #174.

Clause 162.9.3.4, p 170

Even-odd jitter is calculated using the measurement method specified in 120D.3.1.8.2. with the following exceptions:

a) The test pattern is either PRBS13Q or alternatively PRBS9Q. PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only one pattern is sufficient.

b) The corner frequency of the clock recovery unit (CRU) may be set lower than 4 MHz. Meeting the even-odd jitter requirement with only one CRU bandwidth is sufficient.

NOTE—If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter may not be correctly observed.

Proposed response

NOTE—If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter might not be correctly observed. As a result, the observation of J3u and Jrms might also be affected..

162 TX Jitter
175

Clause 162.9.3.4, p 170

Even-odd jitter is calculated using the measurement method specified in 120D.3.1.8.2. with the following exceptions:

a) The test pattern is either PRBS13Q or alternatively PRBS9Q. PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only one pattern is sufficient.

b) The corner frequency of the clock recovery unit (CRU) may be set lower than 4 MHz. Meeting the even-odd jitter requirement with only one CRU bandwidth is sufficient.

NOTE—If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter may not be correctly observed.

Proposed response

NOTE—If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter might not be correctly observed. As a result, the observation of J3u and Jrms might also be affected..

162 TX Jitter
225

Cl 162 SC 162.9.3.4 P 170 L 46 # I-225

Zivny, Pavel Tektronix, Inc.

Comment Type **T** *Comment Status* **D** *TX jitter*

the statement "The test pattern is either PRBS13Q or alternatively PRBS9Q. PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only one pattern is sufficient" includes PRBS9Q only as a test equipment work-around. Clarify that PRBS13Q is preferred. Reasoning: allowing either of two different patterns increases compliance uncertainty. The PRBS9Q is not needed for equipment available in 2022.

SuggestedRemedy

repalce "The test pattern is either PRBS13Q or alternatively PRBS9Q. PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only one pattern is sufficient." with
"The test pattern is PRBS13Q or alternatively PRBS9Q (deprecating). PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only PRBS13Q pattern is sufficient; in cases when that fails due to do test equipment problems the PRBS9Q might be used."

Proposed Response *Response Status* **W**

PROPOSED REJECT.
[Editor's note: Changed clause/subclause from 166/166.9.3.4 to 162/162.9.3.4]
The comment does not provided sufficient justification for the proposed changes.
For task force discussion.

Clause 162.9.3.4, p 170

Even-odd jitter is calculated using the measurement method specified in 120D.3.1.8.2. with the following exceptions:

a) The test pattern is either PRBS13Q or alternatively PRBS9Q. PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only one pattern is sufficient.

b) The corner frequency of the clock recovery unit (CRU) may be set lower than 4 MHz. Meeting the even-odd jitter requirement with only one CRU bandwidth is sufficient.

NOTE—If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter may not be correctly observed.

Suggested remedy

a) The test pattern is PRBS13Q or alternatively PRBS9Q (deprecating). PRBS9Q is defined in 120.5.11.2.a. Meeting the even-odd jitter requirement with only PRBS13Q pattern is sufficient; in cases when that fails due to test equipment problems the PRBS9! Might be used..

162 Tx Measurement
224

Cl **162** *SC* **162** *P* **166** *L* **6** # I-224

Zivny, Pavel Tektronix, Inc.

Comment Type **T** *Comment Status* **D** *TX measurement*

The "using a test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth." allows for large range of result change depending on the end of B-T filter compliance. This can readily be corrected by specifying the roll-off, as has been done in optical standards for years - see e.g. 140.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ).
Reasoning: experiments show that for realistic signals the sensitivity (of measurment results) to roll-off compliance becomes insignificant past about 55 GHz. Presentation available.

SuggestedRemedy

Append "using a test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth" with "compliant (to the B-T response) to at least 58 GHz, and lower or the same level as the 58 GHz response thereafter".

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient evidence to support the suggested remedy. In particular, some analysis to support the comment is necessary.
For task force discussion.

162.9.3 Transmitter characteristics

The transmitter on each lane shall meet the specifications given in Table 162–10 and detailed in the referenced subclauses. Unless specified otherwise, all transmitter signal measurements are made for each lane separately, at TP2, utilizing the test fixtures specified in Annex 162B, using a test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth. The connection from TP2 to the test equipment is AC-coupled.

insert

compliant (to the B-T response) to at least 58 GHz, and lower or the same level as the 58 GHz response thereafter

162 TX Measurement 49

Cl **162** *SC* **162.9.3** *P* **166** *L* **9** # I-49

Ran, Adee Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **D** *TX measurement*

The 50 Ohm termination on each conductor is specified only for DC common mode measurement. I cannot find a requirement that differential signal measurement is also done with similar terminations.

It is important to specify the termination of each conductor separately, to avoid reflections from the test equipment, and to ensure the expected common mode termination (the scope cannot be isolated from signal ground).

SuggestedRemedy

Change "using a test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth" to "using a test system with 50 Ohm termination on each conductor of the differential pair, and a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
The suggested remedy addresses AC common-mode, as well as differential, signal measurements.
Implement the suggested remedy with editorial license.

162.9.3 Transmitter characteristics

The transmitter on each lane shall meet the specifications given in Table 162–10 and detailed in the referenced subclauses. Unless specified otherwise, all transmitter signal measurements are made for each lane separately, at TP2, utilizing the test fixtures specified in Annex 162B, using a test system with a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth. The connection from TP2 to the test equipment is AC-coupled.

Suggested remedy

The transmitter on each lane shall meet the specifications given in Table 162-10 and detailed in the referenced subclauses. Unless specified otherwise, all transmitter signal measurements are made for each lane separately, at TP2, utilizing the test fixtures specified in Annex 162B, using a test system with 50 Ohm termination on each conductor of the differential pair, and a fourth-order Bessel-Thomson low-pass response with 40 GHz 3 dB bandwidth. The connection from TP2 to the test equipment is AC-coupled.

162 TX Quiet Mode
48, 78, 121

Cl **162** *SC* **162.8.11** *P* **164** *L* **27** # I-48

Ran, Adee Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **D** *TX QUIET mode*

When we defined the addition of QUIET state to the PMD control function in 136.8.11, it had the text "This variable is always set to FALSE for 50 Gb/s per lane PHYs, otherwise it is set to TRUE". Now that this change has been implemented in 802.3dc D3.0 and clause 136 removed from 802.3ck, we lost the requirement to set it to TRUE for the PHYs in clauses 162 and 163.

The suggested remedy is to add this requirement as another exception in 162.8.11.

An alternative solution is to amend the updated 136.8.11.7.1 (as of 802.3dc D3.0), specifically the definition of use_quiet_in_training, to be optional only in 50 Gb/s. This could be done as follows:

"Boolean variable that is TRUE if the PMD control function (see Figure 136–7) can enter the QUIET state. The value of this variable is implementation dependent for 50 Gb/s per lane PHYs, and TRUE for all other PHYs"

And amend the PICS of clause 136 accordingly.

SuggestedRemedy

Add exception to the list in 162.8.11:
h) The value of use_quiet_in_training (see 136.8.11.7.1) is TRUE.

Add a corresponding PICS item in 163.13.4.2.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.8.11** *P* **164** *L* **42** # I-121

Healey, Adam Broadcom Inc.

Comment Type **T** *Comment Status* **D** *TX QUIET mode*

In IEEE P802.3ck/D2.2, the definition of the variable use_quiet_in_training included the statement that "this variable is always set to FALSE for 50 Gb/s per lane PHYs, otherwise it is set to TRUE." When the modifications to 136.8 were moved to the IEEE P802.3 (IEEE 802.3dc) revision project, the statement was modified to state that "the value of this variable is implementation dependent." Since there is no superseding statement in 162.8.11, the value of use_quiet_in_training is implementation dependent as defined in the base document and not required to be TRUE for 100G/lane as it was in IEEE P802.3ck/D2.2.

SuggestedRemedy

If the intent is require use_quiet_in_training to be TRUE for 100G/lane PHYs, then add the following item to the list: "f) The variable use_quiet_in_training is set to TRUE."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #48.

Cl **162** *SC* **162.8.11** *P* **164** *L* **42** # I-78

Slavick, Jeff Broadcom Inc

Comment Type **TR** *Comment Status* **D** *TX QUIET mode*

In D2.2 the use_quiet_in_training variable found in Cl136 is set to TRUE for non-50Gbps PHYs. In the current baseline draft use_quiet_in_training being set to TRUE is implementation dependent.

SuggestedRemedy

In the list of exceptions add:

h) The variable use_quiet_in_training is set to TRUE (see 136.8.11.7.1)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #47.

Note: Cross-clause with 163

162 TX Quiet Mode
48, 78, 121

The PMD shall implement one instance of the PMD control function described in 136.8.11 for each lane with the following exceptions:

a) The control field structure is specified in Table 162–9.
b) The terminal count of max_wait_timer as specified in 136.8.11.7.3 is 12 s.
c) For k_list as specified in 136.8.11.4.4, the set of valid transmitter equalizer coefficient indices is {–3, –2, –1, 0, +1}.
d) For the initial condition request as described in 136.8.11.2.1 five predefined transmitter equalizer settings are specified in 162.9.3.1.3.
e) The coefficient select bits in the control field (Table 136–9) and the coefficient select echo bits in the status field (Table 136–10) have an additional combination, 1 0 1, for selecting $c(-3)$.
f) The "No equalization" value (see 136.8.11.2.4) of $c(-3)$ is 0.
g) A receiver is expected to assert local_tf_lock within 275 ms from entry into the AN_GOOD_CHECK state in Figure 73–11 provided that there is a compliant signal containing valid training frames at the PMD input.

The PMD control functions operate independently on each lane.

Suggested remedy

h) The value of use_quiet_in_traning (see 136.8.11.7.1) is TRUE.

162 TX Quiet Mode
48, 78, 121

163.13.4.2 PMD control function

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	PMD control function	162.8.11	Implemented as specified, one instance for each lane, operating independently	M	Yes [ ]
PC2	Training pattern	136.8.11.1.3	Each lane implements four generator polynomials defined in Table 136–8	M	Yes [ ]
PC3	Training pattern	136.8.11.1.3	State set to the value of seed_*i* at the start of the training pattern	M	Yes [ ]
PC4	Control field structure	162.8.11	As shown in 162.8.11	M	Yes [ ]
PC5	Receiver frame lock bit	136.8.11.3.3	Initially set to zero, not set to 1 until local_tf_lock is true	M	Yes [ ]
PC6	Initial condition setting	136.8.11.4.1	When requested, set according to the request, with values per Table 162–11	M	Yes [ ]
PC7	Handshake timing	136.8.11.6	When the transmitted frame lock bit is 1, acknowledge requests within less than 2 ms	M	Yes [ ]
PC8	Transmit precoded data	136.8.11.7.5	PMD causes adjacent PMA to use or not use precoding on transmitted data according to modulation and precoding status bit	M	Yes [ ]
PC9	Receive precoded data	136.8.11.7.5	PMD informs adjacent PMA about precoding of received data according to modulation and precoding request bit	M	Yes [ ]

Suggested remedy: add corresponding PICS item in 163.13.4.2

162 TX Quiet Mode
47, 79

Cl **162** *SC* **162.8.2** *P* **162** *L* **34** # I-47

Ran, Adee Cisco Systems, Inc.

Comment Type **T** *Comment Status* **D** *TX QUIET mode*

The transmit function operating modes listed are DATA and TRAINING, but with the change of the PMD control state diagram we also need a QUIET mode, as in clause 136 (in 802.3dc).

SuggestedRemedy

In the first paragraph change "The PMD transmit function has two operating modes, DATA and TRAINING" to "The PMD transmit function has three operating modes: DATA, TRAINING, and QUIET".

Add the following paragraph at the end of 162.8.2:
"When operating in QUIET mode the PMD transmit function shall turn off the transmitter such that the transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max) with Tx disabled in Table 162–10."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The suggested remedy is good except the transmitter does not necessarily "turn off"; "disable" is a better term.

In the first paragraph change "The PMD transmit function has two operating modes, DATA and TRAINING" to "The PMD transmit function has three operating modes: DATA, TRAINING, and QUIET"

Add the following paragraph at the end of 162.8.2:
"When operating in QUIET mode the PMD transmit function shall disable the transmitter such that the transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max) with Tx disabled in Table 162–10."

Cl **162** *SC* **162.8.2** *P* **162** *L* **35** # I-79

Lusted, Kent Intel Corporation

Comment Type **TR** *Comment Status* **D** *TX QUIET mode*

The IEEE P802.3dc revision project made a change to the PMD control state diagram referenced in the P802.3ck draft. The PMD transmit function now has three operating modes, DATA, TRAINING and QUIET. (see IEEE P802.3dc D3.0 Cl 136.8.2 on p5315, line 49). The 3ck text does not specify the QUIET mode nor it's use.

SuggestedRemedy

Change the first sentence of Cl 162.8.11 to include the QUIET state by changing the sentence to "The PMD transmit function has three operating modes: DATA, TRAINING, and QUIET."

Add a second sentence to the first paragraph in Cl 162.8.11: "Support for the QUIET operating mode is required and implementations shall set the variable use_quiet_in_training (see 136.8.11.7.1) to TRUE."

Add a new paragraph to the end of Cl 162.8.11 that describes the QUIET mode: "When operating in QUIET mode the PMD transmit function shall turn off the transmitter such that the transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max) with Tx disabled in Table 136–11."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the responses to comments #47 and #48.

162 TX Quiet Mode
47, 79

The PMD transmit function has three operating modes: DATA, TRAINING, and QUIET.

Replace

162.8.2 PMD transmit function

The PMD transmit function has two operating modes, DATA and TRAINING. The operating mode is controlled by the PMD control state diagram (Figure 136–7).

When operating in DATA mode, the PMD transmit function shall convert the symbol stream requested by the PMD service interface message PMD:IS_UNITDATA_*i*.request(tx_symbol) of each lane into an electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical specifications in 162.9.3. The differential output voltage (SL_i<p> minus SL_i<n>) meets the specifications in 162.9.3.1.1 where the PAM4 symbol values 0, 1, 2, and 3 correspond to the tx_symbol values zero, one, two, and three, respectively, with the highest differential output voltage corresponding to tx_symbol = three and the lowest differential output voltage corresponding to tx_symbol = zero.

When operating in TRAINING mode, the PMD transmit function shall convert the symbol stream generated by the PMD control function of each lane into an electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical specifications in 162.9.3. The differential output voltage (SL_i<p> minus SL_i<n>) meets the specifications in 162.9.3.1.1, with the highest differential output voltage corresponding to the PAM4 symbol 3 and the lowest differential output voltage corresponding to the PAM4 symbol 0.

When operating in QUIET mode the PMD transmit function shall disable the transmitter such that the transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max) with Tx disabled in Table 162–10.

Add

162 TX Rpeak
51, 136, 172

Cl **162** *SC* **162.9.3.1.2** *P* **169** *L* **8** # I-51

Ran, Adee — Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **D** *TX Rpeak*

"The linear fit pulse peak ratio shall be greater than 0.397" - but there is no definition of that parameter.

163.9.2.5 has a related parameter "Difference linear fit pulse peak ratio" calculated using a procedure in 163A.3.2.1, where Equation (163A–9) defines R_peak(meas). A similar calculation should be used here, but for this clause there is only a measured parameter without a reference parameter, so it can't point to 163A.

SuggestedRemedy

Insert a paragraph after the first paragraph of 162.9.3.1.2:
"The linear fit pulse peak ratio R_peak is defined as the ratio between the maximum value of p(k) and the steady-state voltage v_f."

{where _ indicates subscript}

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.9.3.1.2** *P* **169** *L* **8** # I-136

Hidaka, Yasuo — Credo Semiconductor

Comment Type **E** *Comment Status* **D** *TX Rpeak*

The minimum value of the linear fit pulse peak ratio should not be described in the body text. The text is inconsistent with Table 162-10, because the text says "greater than" but Table 162-10 implicates "greter than or equal to". 0.397 is allowed in Table 162-10 as the minimum value, but not allowed in the body text. Avoid the minimum value in the text and the text should refer to the table.

SuggestedRemedy

Change "The linear fit pulse peak ratio shall be greater than 0.397 after the transmit equalizer initial condition has been set to preset 1 (no equalization)." to "The linear fit pulse peak ratio shall meet the requirements specified in Table 162-10 after the transmit equalizer initial condition has been set to preset 1 (no equalization)."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.9.3.1.2** *P* **169** *L* **1** # I-172

Dawe, Piers J G — NVIDIA

Comment Type **T** *Comment Status* **D** *TX Rpeak*

Table 162-10 says "Linear fit pulse peak ratio" and refers to this subclause whose title is "Steady-state voltage and linear fit pulse peak", and does not say what "pulse peak ratio" means. Nor does 162.9.3.1.1.

SuggestedRemedy

Change the title to "Steady-state voltage and linear fit pulse peak ratio". Define linear fit pulse peak ratio.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #51.

D3.0

162.9.3.1.2 Steady-state voltage and linear fit pulse peak

The steady-state voltage v_f is defined as the sum of the linear fit pulse $p(1)$ through $p(M \times N_v)$ divided by M, measured with transmit equalizer set to preset 1 (no equalization). N_v is set equal to 200. The linear fit procedure for obtaining p and the values of M and N_p are defined in 162.9.3.1.1. The steady-state voltage shall meet the requirements specified in Table 162–10.

The linear fit pulse peak ratio shall be greater than 0.397 after the transmit equalizer initial condition has been set to preset 1 (no equalization).

Suggested remedies

162.9.3.1.2 Steady-state voltage and linear fit pulse peak

The steady-state voltage v_f is defined as the sum of the linear fit pulse $p(1)$ through $p(M \times N_v)$ divided by M, measured with transmit equalizer set to preset 1 (no equalization). N_v is set equal to 200. The linear fit procedure for obtaining p and the values of M and N_p are defined in 162.9.3.1.1. The steady-state voltage shall meet the requirements specified in Table 162–10.

The linear fit pulse peak ratio R_peak is defined as the ratio between the maximum value of p(k) and the steady-state voltage v_f.

The linear fit pulse peak ratio shall meet the requirements specified in Table 162-10 after the transmit equalizer initial condition has been set to preset 1 (no equalization)

162 TX Control
52

Cl **162** *SC* **162.9.3.1.5** *P* **170** *L* **23** # I-52

Ran, Adee Cisco Systems, Inc.

Comment Type **T** *Comment Status* **D** *TX control*

'A coefficient may be set to zero by asserting a coefficient request of “no equalization” for that coefficient' - but c(0) will be set to 1 this way.

The requirements to set to zero are only for c(-3), c(-2), c(-1) and c(1).

SuggestedRemedy

Change the quoted sentence to:
'Any of the coefficients c(-3), c(-2), c(-1), or c(1) may be set to zero by asserting a coefficient request of “no equalization” for that coefficient'.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

162.9.3.1.5 Coefficient range

When sufficient “increment” or “decrement” requests have been received for a given coefficient, the coefficient reaches a lower or upper bound based on the range of that coefficient or the combination of coefficients.

With $c(-3)$, $c(-2)$, and $c(-1)$ set to zero and both $c(0)$ and $c(1)$ having received sufficient “decrement” requests so that they are at their respective minimum values, $c(1)$ shall be less than or equal to −0.2.

With $c(-3)$, $c(-2)$, $c(-1)$, and $c(1)$ set to zero and having received sufficient “decrement” requests so that it is at its minimum value, $c(0)$ shall be less than or equal to 0.5.

With $c(-3)$, $c(-2)$, and $c(1)$ set to zero and both $c(-1)$ and $c(0)$ having received sufficient “decrement” requests so that they are at their respective minimum values, $c(-1)$ shall be less than or equal to −0.34.

With $c(-3)$, $c(-1)$, and $c(1)$ set to zero, $c(0)$ having received sufficient “decrement” requests so that it is at its minimum value, and $c(-2)$ having received sufficient “increment” requests so that it is at its maximum value, $c(-2)$ shall be greater than or equal to 0.12.

With $c(-2)$, $c(-1)$, and $c(1)$ set to zero and both $c(-3)$ and $c(0)$ having received sufficient “decrement” requests so that they are at their respective minimum values, $c(-3)$ shall be less than or equal to −0.06.

NOTE—A coefficient may be set to zero by asserting a coefficient request of “no equalization” for that coefficient, using the control function specified in 162.8.11, or by implementation specific means.

Suggested remedy (replace the note)

Note—Any of the coefficients c(-3), c(-2), c(-1), or c(1) may be set to zero by asserting a coefficient request of “no equalization” for that coefficient using the control function specified in 162.8.11, or by implementation specific means.

162 TX RITT
179

Cl **162**	*SC* **162.9.4.3.4**	*P* **178**	*L* **11**	# I-179

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **D** *RITT*

Please help the reader understand the relation between the normalized NSD limits and Hhp

SuggestedRemedy

Please add the plot of Hhp, squared and normalized, to Figure 162-5, NSD(f) constraints. See example in attached file.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient justification to support the proposed changes.
The proposed change does not improve the clarity or accuracy of the standard. In fact, the proposed change detracts from the intent of the figure.
For task force discussion.

D3.0

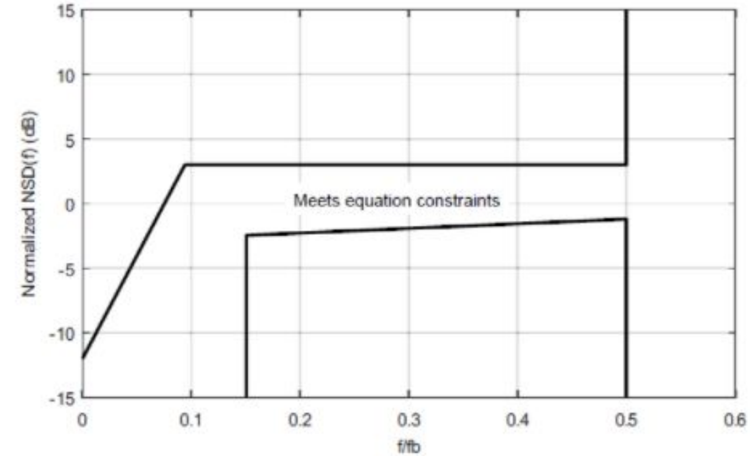
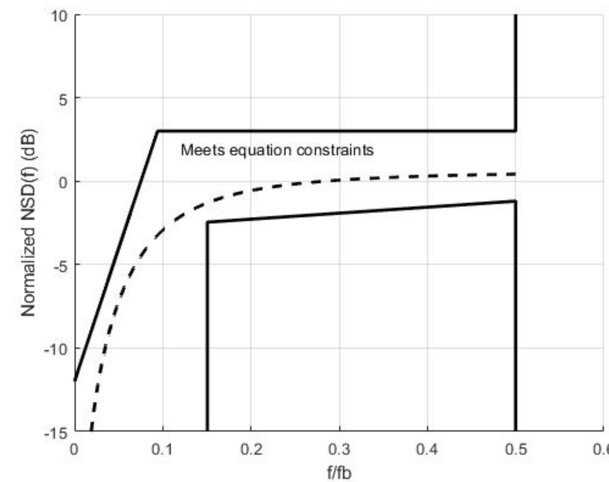


Figure 162–5—NSD(f) constraints

Suggested Remedy



162 RX RITT
54, 124

Cl **162** *SC* **162.9.4.3.3** *P* **175** *L* **39** # I-54

Ran, Adee Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **D** *RITT cal*

Item e in the list is very difficult to understand, and the referenced equations have some parameters defined in Annex 93A which may be unclear. Also, the value of f_hp in equation 162-11 is not provided anywhere.

The phrasing should be improved to enable implementing this procedure.

SuggestedRemedy

A presentation proposing a rewrite is planned.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The suggested remedy as written does not provide sufficient detail to implement. Pending planned TF presentations.
For task force discussion.

Cl **162** *SC* **162.9.4.3.3** *P* **176** *L* **23** # I-124

Calvin, John Keysight Technologies

Comment Type **T** *Comment Status* **D** *RITT cal*

ADD formula (162-78) has a discriminant which under many legitimate conditions can be negative, causing the expression to fail. The accompanying Note 2 asserts "If this does not hold, a different transmitter should be used in the test setup." This TE tool provider is seeing a jump in customer complaints that the BERT they purchased for receiver testing can regularly trigger this negative discriminant condition. Something more constructive than "a different transmitter should be used" needs to be considered here.

SuggestedRemedy

Consider the following contribution :
https://www.ieee802.org/3/ck/public/adhoc/apr14_21/hidaka_3ck_adhoc_01_041421.pdf
which speaks to this exact issue. Note pages 4 and 5 outline the conditions whereby this discriminant can be negative with instrument grade test tools.
Note 2 in subclause 162.9.4.3.3 should be revised to say the following:
"The Calculation of ADD may, under certain conditions pose a negative discriminant. If this condition occurs, the recommended solution is to increase DJ to increase the ADD parameter till the discriminant is positive"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The following presentation was reviewed by the task force at previous ad hoc meetings:
https://www.ieee802.org/3/ck/public/22_01/calvin_3ck_01a_0122.pdf
https://www.ieee802.org/3/ck/public/adhoc/jan19_22/rysin_3ck_adhoc_01_011922.pdf

Straw poll #1 at the 01/12/2022 interim meeting showed support for increasing ADD to address the negative descriminant issue. The results of the straw poll are recorded in the meeting minutes:
https://www.ieee802.org/3/ck/public/adhoc/jan12_22/minutes_011222_3ck_adhoc.pdf

Implement the suggested remedy.

D3.0

NOTE 2—Calculation of A_{DD} requires that $(Q3d^2 + 1) \times J_{RMS}^2 \ge \left(\frac{J3u}{2}\right)^2$. If this does not hold, a different transmitter should be used in the test setup.

Suggested Remedy

Note-2—The calculation of ADD may, under certain conditions, pose a negative discriminant. If this condition occurs, the recommended solution is to decrease DJ to increase the ADD parameter until the discriminant is positive.

162 CR Loss Budget 170, 180

Cl **162** *SC* **162.9.3** *P* **166** *L* **32** # I-170

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **D** *CR loss budget*

The draft CR loss budget wastes 3 dB in nearly every case. The relative range of host losses, 6.875/2.3 = 3:1, is too small for switch layout yet not needed for NICs.
The recommendation for the host traces plus BGA footprint and host connector footprint, 6.875 dB, compares very poorly with C2M's host insertion loss up to 11.9 dB, making passive copper to this draft expensive and unattractive for a switch, yet a full range of NICs can be made with only 3.75 dB.
C2M already has short and long ports.
Server-switch links are asymmetric in form factor (e.g. QSFP-DD to 2 x QSFP) and will get made with an asymmetric loss budget, so it would be better for the standard to regularise what will happen anyway with industry-standard registers.
This change would also benefit CR switch-switch links because the low loss of the shortest ports would be recognised, so more of the ports in a switch (with higher loss) could be used for CR switch-switch links.
The symmetric budget is used for some designs under way and may be useful in future for LOM, so it is kept here as "B", and the better way (A and C) added.

SuggestedRemedy

As in dawe_3ck_01a_0721.pdf:
3 classes of CR ports, host loss allocations of A 9.5, B 6.875, C 3.75 dB. B is as D2.1.
A connects to C, B to B or C, C to A, B or C.
Use 2 bits in the training control field to advertise A, B or C to the other end.
In Table 162-10, add limits A and C for linear fit pulse peak ratio (min). Change text in 162.9.3.1.2 to refer to the table.
In Table 162-14, add columns for Test 2 (high loss), A and C, with test channel insertion loss: A: 6.875-3.75 = 3.125 dB lower (20.5 dB to 21.5 dB), and C: 9.5-6.875 = 2.625 dB higher (26.25 dB to 27.25 dB). No change needed for Test 1.
In 162A.4, add equations for IL_PCBmax and ILHostMax A and B and show them in Fig 162A-1 and 2. In 162A.5, add Value columns A, C in Table 162A-1 (ILCh min and ILMaxHost differ). Adjust figures 162A-3 and 4.
Add MDIO registers to report local and remote host ability to station management, for inventory and diagnostics.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient justification to support the proposed changes.
For task force discussion.

Cl **162** *SC* **162.11** *P* **181** *L* **31** # I-180

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **D** *CR loss budget*

The poor max cable loss makes CR unattractive, while all NICs and some ports on any switch have host loss budget going to waste. Enabling longer cables on a minority of links is needed.
In the remedy, each host knows the other host's loss class through the training protocol and the cable's loss class from its I2C compliance code, so no extra management features needed in the spec for the long cable class.

SuggestedRemedy

2 classes of cable, which could be called "short" (19.75 dB, as today) and "long", 19.75+2*(6.875-3.75) - 0.5 = 19.75+6.25 - 0.5 = 25.5 dB max (achievable cable length 3 m). Long cables connect port types C (see another comment) at both ends, short cables connect a valid combination of A, B, C.
In 162.11.2, cable assembly insertion loss, change text "less than or equal to 19.75 dB" to refer to Table 162-17 instead.
In 162.11.7.1.1, add zp = 30.7 mm for the "short" cable.
In Table 162A-1, add a column for the A-short-A scenario (ILCamax is 25.5 dB).
Illustrate in figures 162A-3 and 162A-4.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient justification to support the proposed changes.
The suggested remedy is predicated on the adoption of comment #170.
For task force discussion.

162 RLcc
178, 181, dawe_04

Cl **162** *SC* **162.9.3.6** *P* **172** *L* **27** # I-178

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **D** *TX RLcc*

As for the mated test fixtures and the cable, this common mode return loss spec RLcc becomes useless at the frequency when the MCB loss is 2/2 dB, which is only 10 GHz. The spec should trend down with the MCB trace loss at 0.1 dB/GHz.

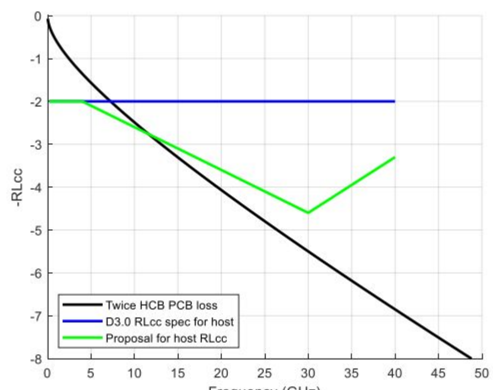
SuggestedRemedy

Use a frequency-dependent mask 2 dB 0.2 <= f <= 4, 1.6+0.1*f dB 4 < f <= 30, 8.5-0.13f 30 < f <= 40. f is in GHz. See another comment for cable RLcc, 162.11.6.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The suggested remedy does not provide data or analysis to demonstrate that the proposed mask is sufficient.
For task force discussion.

Proposed
Host RLcc



Cl **162** *SC* **162.11.6** *P* **185** *L* **28** # I-181

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **D** *CA RLcc*

We need a common mode return loss spec RLcc to stop large common-mode voltages building up through multiple low-loss reflections. As we know, this common mode return loss spec RLcc becomes useless at the frequency when the MCB loss is 1.8/2 dB, which is only 8.5 GHz. The impedance the cable presents is mostly related to the connector, so it's much like the mated test fixtures' RLcc, except at the very lowest frequencies where the cable loss is very small and both connectors can be seen by the measurement. This proposal allows for that.

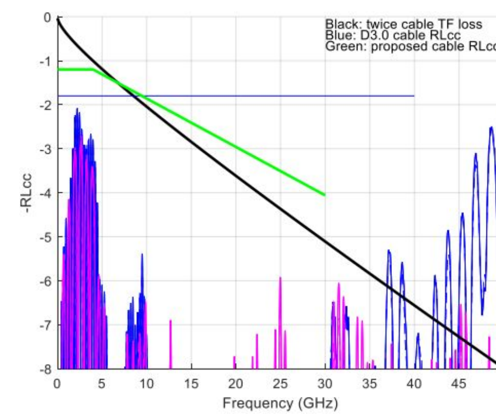
SuggestedRemedy

Use a frequency-dependent mask 1.2 dB 0.05 <= f <= 4, 0.76+0.11*f dB 4 < f <= 30 GHz. f is in GHz. See another comment for Tx, Table 162-11, 162.9.3.6.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE. Although the comment does not provide sufficient evidence to support the proposed remedy. It does provides a better fit to posted CA measurements and merits consideration on that basis. For committee discussion.

Proposed
CA RLcc



162 COM Parameter 183

Dawe_3ck_01a_0921 addresses potential impact of tighter limits for tap positions 13-24.

Cl **162** *SC* **162.11.7** *P* **187** *L* **31** # I-183

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **D** *Rx bgmax*

Cable channels' reference receiver tap weights are less -ve than -0.02, and taps 13 to 40 are less than +0.025. The tap weight limits are not hard cable or channel limits, but they let cables that go outside the envelope pay a price in COM for it (see dawe_3ck_01a_0921).

The normalized DFE coefficient minimum limit bbmin for taps 3 to 12 is -0.03 and for taps 13 to 40 it is -0.05 (bgmax 0.05) but the receiver is protected from bad taps 25-40 by the tail RSS limit. But the receiver is not protected so well for taps 13 to 24.

We can expect cable channels to be better for reflections than backplane channels because hosts must be designed for maximum-loss performance, and cable technology will also be adequate for maximum-loss performance. As a cable can have worse tap weights than the headline numbers for a very small COM penalty (see dawe_3ck_01a_0921 slide 5), this remedy leaves margin for the cable.

SuggestedRemedy

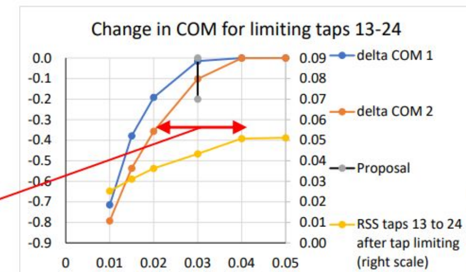
For CR, in Table 162-19, change Normalized coefficient magnitude limit for DFE floating taps, bgmax, from 0.05 to 0.03.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Tap limit should be tighter than unconstrained taps observed

•



Spec allows *channel* to have one tap more than 0.02 beyond *reference Rx* tap limit

This channel -0.0405, could pass easily with -0.06

For limits of 0.02 to 0.01, one then two +ve taps respectively were truncated too, so the roll-off for –ve tap limit as proposed would be a little less than shown

We should: tighten bbmin(13-24) to reduce COM slightly, at -0.03
Or: set it tighter to reduce COM for worst reference channel to 3 dB
Or: align –ve limit for taps 13 to 40 to limit for taps 3 to 12, at -0.03

802.3ck Sep 2021 Tighter tail tap limit and backplane channel Bch2_b2p5_7 5

Comment #57

Cl **162** *SC* **162.11.5** *P* **184** *L* **33** # I-57

Ran, Adee Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **D** *CA ILcd*

Equation 162-19 lets the difference between ILcd and ILdd be 10 dB up to half of (an old Nyquist frequency) and then linearly lower at higher frequencies. This does not make sense physically, and open the door to poor cables. The Tx output common mode noise problem is exacerbated by strong conversion from common mode to differential signal.

Note that COM does not cover the conversion loss term, so we should strive to make it negligible, rather than allowing it to be large.

At low frequencies we expect low ILdd and high ILcd, and the difference is much larger than 10 dB. Even at high frequencies up to 40 GHz, channels submitted to 802.3ck do not exceed 10 dB. We should not allow less than 10 dB difference across the upper half of the spectrum.

Based on samples of submitted channels and some measured channels it is suggested to tighten this specification to be 24 dB at the lowest frequency, linear slope to 10 dB at Nyquist/2, and constant 10 dB at maximum frequency.

This also holds for the specification in clause 163 (channel construction may be different but the arguments above still hold and the effect on the link budget is the same).

A presentation of some contributed data compared to the proposed limit is planned. Any contradictory data would be welcome.

SuggestedRemedy

Change equation 162-19 limit to be
24 - 13.56/f *14 | 0.05 <= f <= 13.56
10 | 13.56 <= f <= 40

Change Figure 162–9 accordingly.

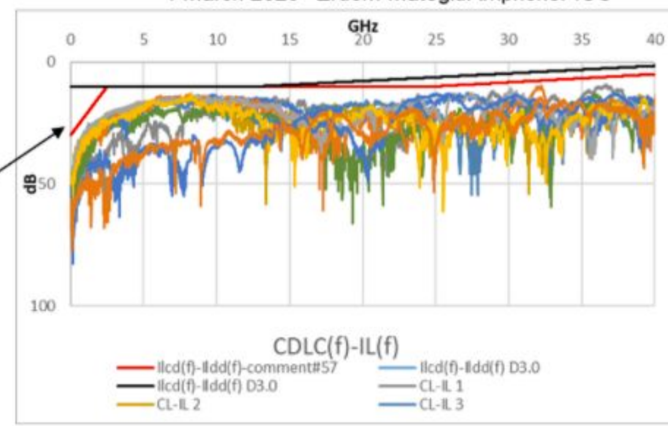
Proposed Response *Response Status* **W**

PROPOSED REJECT.
Commenter has requested to update suggested remedy to:
Change equation 162-19 limit to be
30 – 8f |0.05 </= f </= 2.5
10 |2.5 </= f </= 25
10 – (f-25)/3 |25 </= f </= 40
Change Figure 162–9 accordingly.
For committee discussion to consider basis for revision to suggested remedy.

100 Gbps Copper Cable Measurement
and S-Parameter File
8 Channel Cable Measurement

https://www.ieee802.org/3/ck/public/tools/cucable/matoglu_3ck_adhoc_01_030420_channels.zip

Cu Cable Channels
OSFP112G 2m Cable Assembly Measurements
Update
Measured OSFP 2m 25awg Cable
4-March-2020 Erdem Matoglu Amphenol ICC



$$ILcd(f) - ILdd(f) \ge \left\{ \begin{array}{ll} 10 & 0.05 \le f < 12.89 \\ 14 - 0.3108f & 12.89 \le f \le 40 \end{array} \right\} \quad \text{162-19}$$

Comment #218

Cl **162B** *SC* **162B.4.1** *P* **293** *L* **1** # I-218

Dawe, Piers J G NVIDIA

Comment Type **T** *Comment Status* **D** *MTF ILdd*

The reference differential-mode to differential-mode insertion loss of the mated test fixture is a scaled version of Eq 120E-3 and it doesn't align well to kocsis_3ck_01_0719, slide 4. This causes a problem when constructing the lossy channel for the module stressed input test (in dawe_3ck_01a_1121 slide 8, the green line is straighter than the black line at low frequencies).
The new equation has the same loss at Nyquist as the existing one.
See new presentation.

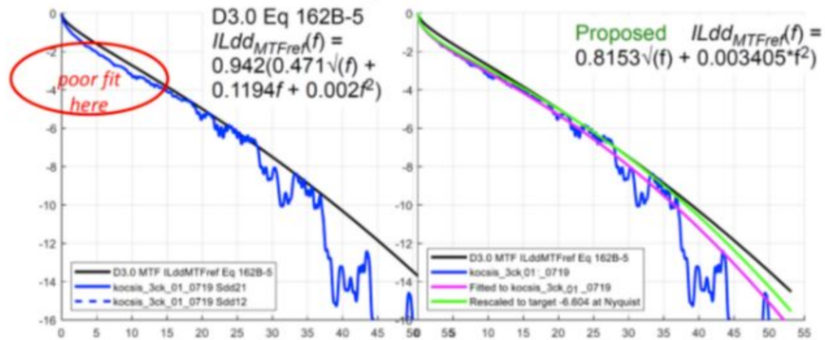
SuggestedRemedy

Change equation 162B-5 from:
ILddMTFref(f) = 0.942(0.471sqrt(f) + 0.1194f + 0.002f2)
to
ILddMTFref(f) = 0.8153*sqrt(f) + 0.003405*f^2)
Update Figure 162B-3, Mated test fixtures differential-mode to differential-mode insertion loss

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
For committee discussion of presentation

Comment 218 Real compliance boards



- We don't expect that compliance board traces will get shorter
  - Possibly the opposite as we go from 4 to 8 to maybe 16-wide modules
- But they might use better dielectric, and tolerancing and detailed improvements
- So the low frequency loss will improve less than the high frequency loss https://ieee802.org/3/ck/public/19_07/kocsis_3ck_01_0719.pdf

dawe_3ck_02_0122.pdf

Comment #1, 120

Cl **162C** *SC* **162C.1** *P* **302** *L* **3** # I-1

Lusted, Kent — Intel Corporation

Comment Type **TR** *Comment Status* **D** *MDI table*

For D2.2 comment resolution, there was contribution for an improved MDI connector mapping that was not accepted by the comment resolution group (CRG). see https://www.ieee802.org/3/ck/public/21_09/ghiasi_3ck_01_0921.pdf One key feedback point on the contribution from the CRG was that the Ground pins should remain in the specification.

QSFP-DD800: For the TX2n/TX2p pair, note that GND pin #1 is closest to TX2n and GND pin #4 is closest to TX2p. Also, GND pin #4 is closest to TX4n and GND pin #7 is closest to TX4p.

For the OSFP TX2n/TX2p pair, note that GND pin #1 is closest to TX2p and GND pin #4 is closest to TX2n. Also, GND pin #4 goes with TX4p and GND pin #7 goes with TX4n.

The issue now comes from having both the OSFP and QSFP-DD800 pins in the same table.
For the QSFP-DD800 column, GND pin #1 is the physical pin next to SL1n (TX2n in the connector spec) and GND pin #4 is the physical pin next to SL1p (TX2p). However, in the OSFP column, the physical GND pin next to SL1n (TX2n) is pin #4, not pin #1 as shown above, and the physical GND pin next to SL1p (TX2p) is pin #1, not #4. Then the table becomes very messy on subsequent rows because the GND pin number can be one of two values in the OSFP case; for example, GND pin #1 is next to SL1p (TX2p) but GND pin #7 is next to SL3n (TX4n).

The GND pins are useful information, keep them in the table(s)

SuggestedRemedy

Replace Table 162C-3 with three tables:
QSFP/QSFP-DD800 table
OSFP table
SFP/SFP-DD/DSFP table

see accompanying presentation.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
A proposal to address this comment is provided in the following presentation:
https://www.ieee802.org/3/ck/public/22_01/lusted_3ck_01_0122.pdf
Implement the proposal in lusted_3ck_01_0122.
For task force discussion.

Cl **162C** *SC* **162C.1** *P* **303** *L* **10** # I-120

Ghiasi, Ali — Ghiasi Quantum LLC,Marvell Semiconductor, Inc.

Comment Type **TR** *Comment Status* **D** *MDI table*

Table 162C-3 has number of error due to lack of pin alignment between OSFP and QSFP/QSFP-DD800

SuggestedRemedy

These need to be broken in to three tables: SFP112/SFP-DD112/DSFP, QSFP112/QSFP-DD800, and the 3rd table for OSFP. Plesae see Lusted-Ghiasi presentation.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #1.

https://www.ieee802.org/3/ck/public/22_01/lusted_3ck_01_0122.pdf

Comment #1, 120

https://www.ieee802.org/3/ck/public/22_01/lusted_3ck_01_0122.pdf

- *Replace Table 162C-3 with three tables:*
- *QSFP/QSFP-DD800 table*
- *OSFP table*
- *SFP/SFP-DD/DSFP table*

QSFP/QSFP-DD800 table

QSFP112	QSFP-DD800	Connector signal name	Description
1	1	GND	Ground
2	2	SL1n	Transmitter Inverted Data Input
3	3	SL1p	Transmitter Non-Inverted Data Input
4	4	GND	Ground
5	5	SL3n	Transmitter Inverted Data Input
6	6	SL3p	Transmitter Non-Inverted Data Input
7	7	GND	Ground
13	13	GND	Ground
14	14	DL2p	Receiver Non-Inverted Data Output
15	15	DL2n	Receiver Inverted Data Output
16	16	GND	Ground
17	17	DL0p	Receiver Non-Inverted Data Output
18	18	DL0n	Receiver Inverted Data Output
19	19	GND	Ground
20	20	GND	Ground
21	21	DL1n	Receiver Inverted Data Output
22	22	DL1p	Receiver Non-Inverted Data Output
23	23	GND	Ground
24	24	DL3n	Receiver Inverted Data Output
25	25	DL3p	Receiver Non-Inverted Data Output
26	26	GND	Ground
32	32	GND	Ground
33	33	SL2p	Transmitter Non-Inverted Data Input
34	34	SL2n	Transmitter Inverted Data Input
35	35	GND	Ground
36	36	SL0p	Transmitter Non-Inverted Data Input
37	37	SL0n	Transmitter Inverted Data Input
38	38	GND	Ground
—	39	GND	Ground
—	40	SL5n	Transmitter Inverted Data Input
—	41	SL5p	Transmitter Non-Inverted Data Input
—	42	GND	Ground
—	43	SL7n	Transmitter Inverted Data Input
—	44	SL7p	Transmitter Non-Inverted Data Input
—	45	GND	Ground
—	51	GND	Ground
—	52	DL6p	Receiver Non-Inverted Data Output
—	53	DL6n	Receiver Inverted Data Output
—	54	GND	Ground
—	55	DL4p	Receiver Non-Inverted Data Output
—	56	DL4n	Receiver Inverted Data Output
—	58	GND	Ground
—	59	DL5n	Receiver Inverted Data Output
—	60	DL5p	Receiver Non-Inverted Data Output
—	61	GND	Ground
—	62	DL7n	Receiver Inverted Data Output
—	63	DL7p	Receiver Non-Inverted Data Output
—	64	GND	Ground
—	70	GND	Ground
—	71	SL6p	Transmitter Non-Inverted Data Input
—	72	SL6n	Transmitter Inverted Data Input
—	73	GND	Ground
—	74	SL4p	Transmitter Non-Inverted Data Input
—	75	SL4n	Transmitter Inverted Data Input

OSFP table

OSFP	Connector signal name	Description
1	GND	Ground
2	SL1p	Transmitter Non-Inverted Data Input
3	SL1n	Transmitter Inverted Data Input
4	GND	Ground
5	SL3p	Transmitter Non-Inverted Data Input
6	SL3n	Transmitter Inverted Data Input
7	GND	Ground
8	SL5p	Transmitter Non-Inverted Data Input
9	SL5n	Transmitter Inverted Data Input
10	GND	Ground
11	SL7p	Transmitter Non-Inverted Data Input
12	SL7n	Transmitter Inverted Data Input
13	GND	Ground
18	GND	Ground
19	DL6n	Receiver Inverted Data Output
20	DL6p	Receiver Non-Inverted Data Output
21	GND	Ground
22	DL4n	Receiver Inverted Data Output
23	DL4p	Receiver Non-Inverted Data Output
24	GND	Ground
25	DL2n	Receiver Inverted Data Output
26	DL2p	Receiver Non-Inverted Data Output
27	GND	Ground
28	DL0n	Receiver Inverted Data Output
29	DL0p	Receiver Non-Inverted Data Output
30	GND	Ground
31	GND	Ground
32	DL1p	Receiver Non-Inverted Data Output
33	DL1n	Receiver Inverted Data Output
34	GND	Ground
35	DL3p	Receiver Non-Inverted Data Output
36	DL3n	Receiver Inverted Data Output
37	GND	Ground
38	DL5p	Receiver Non-Inverted Data Output
39	DL5n	Receiver Inverted Data Output
40	GND	Ground
41	DL7p	Receiver Non-Inverted Data Output
42	DL7n	Receiver Inverted Data Output
43	GND	Ground
48	GND	Ground
49	SL6n	Transmitter Inverted Data Input
50	SL6p	Transmitter Non-Inverted Data Input
51	GND	Ground
52	SL4n	Transmitter Inverted Data Input
53	SL4p	Transmitter Non-Inverted Data Input
54	GND	Ground
55	SL2n	Transmitter Inverted Data Input
56	SL2p	Transmitter Non-Inverted Data Input
57	GND	Ground
58	SL0n	Transmitter Inverted Data Input
59	SL0p	Transmitter Non-Inverted Data Input
60	GND	Ground

SFP/SFP-DD/DSFP table

SFP112	SFP-DD112	DSFP	Connector signal name	Description
11	11	11	GND	Ground
12	12	12	DL0n	Receiver Inverted Data Output
13	13	13	DL0p	Receiver Non-Inverted Data Output
14	14	14	GND	Ground
17	17	17	GND	Ground
18	18	18	SL0p	Transmitter Non-Inverted Data Input
19	19	19	SL0n	Transmitter Inverted Data Input
20	20	20	GND	Ground
—	31	10	GND	Ground
—	32	9	DL1n	Receiver Inverted Data Output
—	33	8	DL1p	Receiver Non-Inverted Data Output
—	34	7	GND	Ground
—	37	3	GND	Ground
—	38	2	SL1p	Transmitter Non-Inverted Data Input
—	39	1	SL1n	Transmitter Inverted Data Input
—	40	22	GND	Ground