TRANSMIT EQUALIZER STEP SIZE SENSITIVITY ANALYSIS

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February 2020

Background

- Tx equalization maximum step size specification was 5% in 50G electrical PMDs (clauses 136, 137, also annex 120D)
  - c(-2) was specified as 2.5%.
- In 802.3ck:
  - COM tool versions up to 2.53 (November 2018) used 2.5% step for precursor coefficients
    - 5% for c(+1)
  - hidaka_3ck_adhoc_01_120518 and sun_3ck_adhoc_01a_120518 compared multiple configurations including 3 FFE tap granularities: 2.5% (labeled “coarse”), 2% (labeled “medium”), and 1.5% (unlabeled)
    - Channels analyzed were mostly backplane, but there were some cable backplanes and CR channels
    - Based on the results, recommended 2% or finer step (see backup)
  - In COM tool version 2.57 (contributed December 2018) it was changed to 2%, and is unchanged since then
  - Baseline proposal heck_3ck_03b_0319 used 2%
  - This is what we have in D1.1.

What's the problem?

Cl **162** *SC* **162.9.3** *P* **140** *L* **10** # 249

Ran, Adee Intel

Comment Type **T** *Comment Status* **D**

The maximum step size of 2% for a PAM4 equalizer creates a significant increase in complexity for a DAC-based transmitter implementation, compared to the step size allowed in the 802.3cd specs.

A PAM4 DAC with the 2.5% specification in 802.3cd is required to be able of outputting 6/0.025=240 possible values, while with a 2% step size it is requires 6/0.02=300 possible values. This means an additional bit should be used in the logic implementing the FFE and DAC control, and the analog circuits should enable more combinations.

The estimated cost in power consumption of the FFE+DAC logic and analog circuits from this small change in resolution, with a non-naive design, is about 0.3-0.4 pJ/bit. This additional power is going to be consumed regardless of the channel in question.

The benefit from this finer resolution has not been analyzed thoroughly enough to justify such an increase in implementation burden and power consumption.

SuggestedRemedy

Change the (max.) values for c(-3) to c(0) to 0.024 (which can be met with a DAC capable of 256 output values).

Proposed Response *Response Status* **W**

PROPOSED REJECT.

All analysis to date has used 2% step size. The commenter proposes increasing step size to 2.5% but does not provide evidence that it does not adversely affect the performance of contributed channels.

- In a nutshell: for a digital FFE implementation, tap resolution affects output resolution.
- Moving from 2.5% to 2% requires an additional DAC bit
  - Otherwise some steps will have no measurable effect.
- Estimated effect on power is an increase of ~0.4 pJ/bit
  - About 40 mW/lane!
- What benefit do we get?

New analysis

- Objective: Assess the impact of transmit equalizer step size on COM results
  - For checking the benefit of the 2% step size specification
- Method: COM simulations with version 2.76 using the set of “critical” backplane channels
  - Sweep step size: from 2.0% to 3.0% in 0.1% steps, plus 4.0%, 5.0%, to establish trend.
  - Step size applied for c(-3), c(-2), c(-1). c(+1) kept at 5%.

Channels & Conditions

Chan #	Name	IL (dB)	Contribution	Channel
14	Heck1	28.8	heck_3ck_01_1118	28dB_Cable_Backplane/Cable_BCP_28dB_0p575_more_isi
53	Mellitz1	26.3	mellitz_3ck_adhoc_02_081519	24,28,30dB including BGA Via/CaBP_BGAVia_Opt2_28d
21	Tracy1	15.7	Tracy_3ck_01_0119	Traditional Backplane Channels/Std_BP_12inch_Meg7
17	Tracy2	12.2		Orthogonal Backplane Channels/DPO_IL_12dB
96	Kareti1	27.7	kareti3ck_01a_1118	Measured Orthogonal Backplane Channels/OAch4
89	Kareti3	28.5		Measured Cabled Backplane Channels/CAch3_b2
70	Kareti5	28.9		Measured_Traditional_Backplane_Channels/Bch2_b7p5_7

Conditions

Pkg trace	12mm Tx/Rx, 31/29mm Tx/RxRx
TxEQ step	2%-5% in 0.1% increments from 2%-3%, 1% increments from 3%-5%
RxEQ	KR reference Rx (21 fixed +3x3 floating to 40UI)

COM 2.76

COM Spreadsheet

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.415	V	
A_fe	0.415	V	
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.2		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

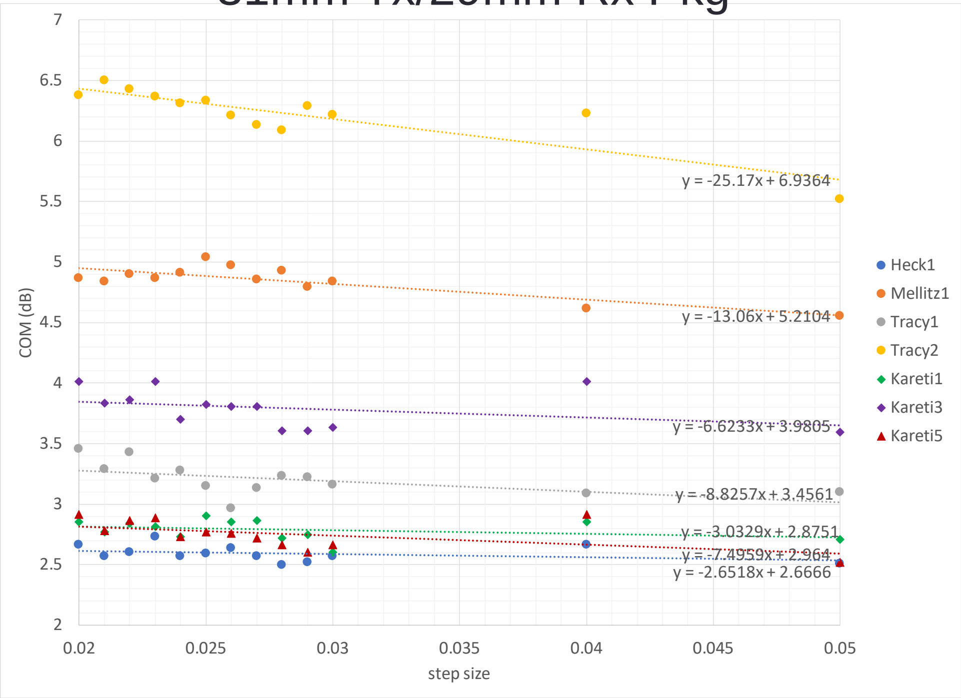
values swept (c(-1), c(-2), c(-3))

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.3407E+09	
rho_x	0.19	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	12	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.2E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

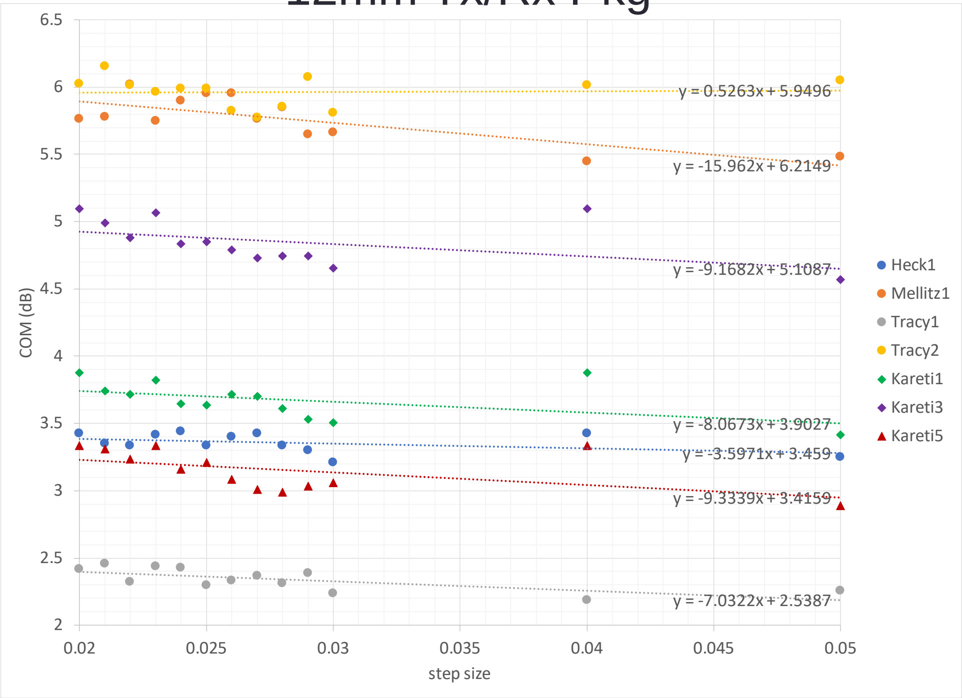
Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
benartsi_3ck_01_0119 & mellitz_3ck_01_0119		
Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*110.3*	mm
z_bp (NEXT)	*110.3*	mm
z_bp (FEXT)	*110.3*	mm
z_bp (RX)	*110.3*	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**0**	**logical**
Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	40	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B_float_RSS_MAX	**0.03**	rss tail tap limit
N_tail_start	**25**	(UI) start of tail taps limit
ICN parameters		
f_v	0.723	*Fb
f_f	0.723	*Fb
f_n	0.723	*Fb
f_2	39.844	GHz
A_ft	0.600	V
A_nt	**0.600**	V
heck_3ck_03b_0319	**Adopted Mar 2019**	**kasapi_3ck_02_1119**
walker_3ck_01d_0719	**Adopted July 2019**	**Adopted Nov 2019**
result of R_d=50		under consideration
benartsi_3ck_01a_0719	**no used for KR**	
mellitz_3ck_03_0919		

Results

31mm Tx/29mm Rx Pkg



12mm Tx/Rx Pkg



In both cases, COM vs. step size trend is very small in all channels
Effect of 2% to 2.5% is between ~0.05 dB (for low COM channels) and 0.13 dB (for the high COM channel)
Results are very “noisy” and inconclusive even at relatively large steps (R^2 maximum value was only ~0.75; most were much worse)

Why does Tx step size have such little effect?

- Tx equalizer is convolved with the channel and CTLE to create a pulse response
- Sampling phase selection and DFE zero-force most of the ISI
  - ISI after the DFE range is practically unaffected by FFE step size
  - The only possible effect is on h(0) (signal), and on h(-2), h(-3), h(-4) (ISI)
  - The residual precursor ISI is likely not a strong contributor to bottom line COM
- The optimal COM may not be exactly on the search grid
- Changing the grid of c(-1), c(-2) may cause a different point of CTLE grid to become “optimal”.

- This represents reality! Not just a tool artifact.

Summary and recommendations

- Moving from 2.5% (max c(-2) step in the 50G PMDs) to 2% (as in D1.1) would require an additional bit in a digital FFE implementation
  - Estimated power impact of ~0.4 pJ/bit
- The Tx FFE coefficient step size has small and inconsistent effect on COM for the analyzed “critical” channels, even in the range of 2% to 5%
- Recommendation: restore the maximum step sizes of c(-3), c(-2), and c(-1) to 2.5%
  - For both KR and CR.

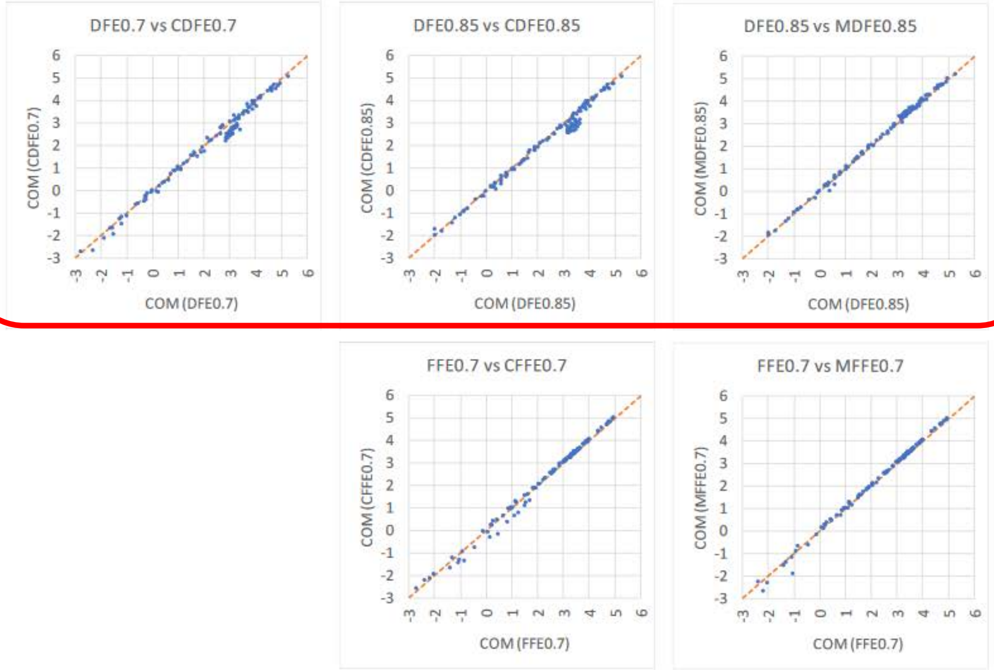
BACKUP

What was the 2% recommendation based on?

TX Resolution Impact

DFE vs [CM]DFE

FFE vs [CM]FFE



- 2.5% (CDFE and CFFE) are often much worse than 1.5% (DFE and FFE)
- 2.0% (MDFE and MFFE) are close to 1.5% (DFE and FFE)

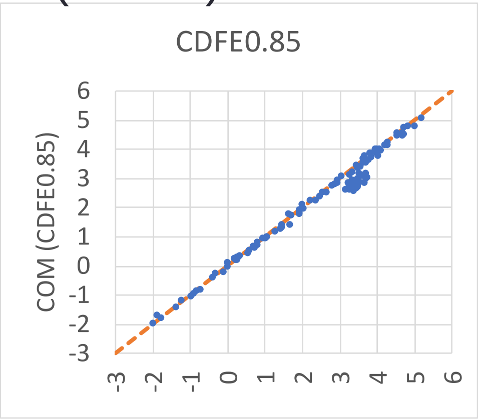
CredŐ

Source:
sun_3ck_adhoc_01a_120518
Slide 8

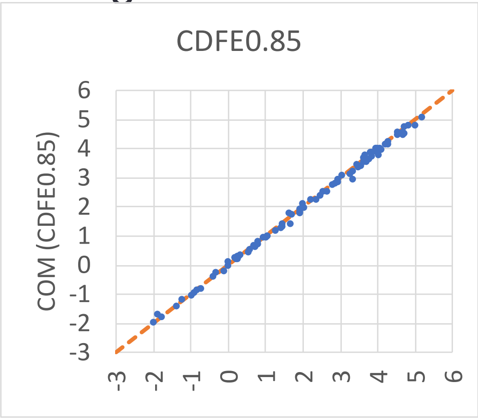
Digging into the data

Full data set provided in hidaka_3ck_adhoc_02_120518 to enable further analysis

Coarse DFE (0.25%) vs. medium DFE (0.2%)



Same, excluding the “AZ1” and “AZ2” Data



16	AZ1	Orthogonal Backplane Channel	zambell_100GEL_01a_0318.pdf
89-115	AZ2	Measured Orthogonal Backplane with Varied Impedances	zambell_3ck_01_1118.pdf

Source: sun_3ck_adhoc_01a_120518 slide 4

Eventually we chose a subset of channels for analysis

The Highlighted Channels

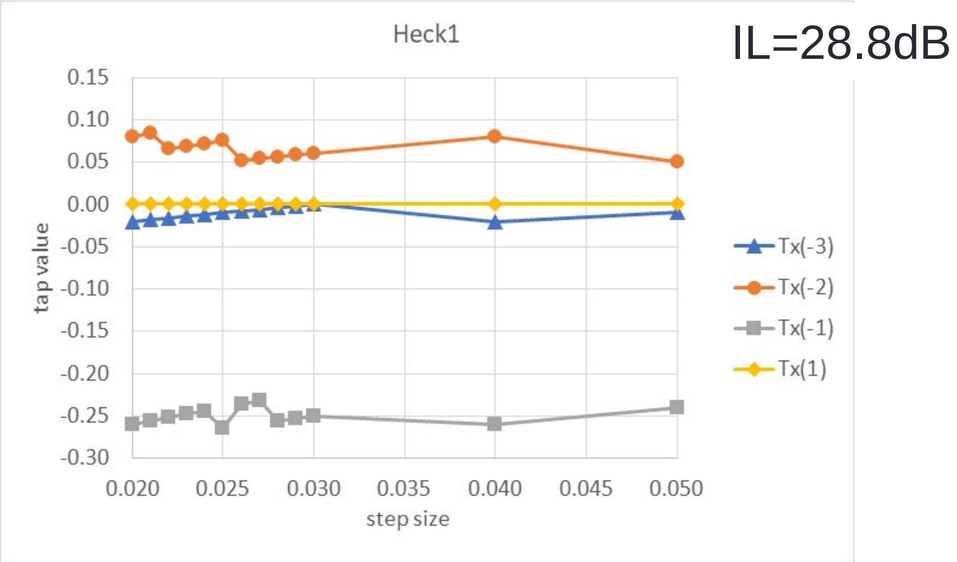
Contribution	Channel
heck_3ck_01_1118	28dB Cabled Backplane/Cable_BKP_28dB_0p575m_more_isi
	16dB Cabled Backplane/Cable_BKP_16dB_0p575m_more_isi
mellitz_3ck_adhoc_02_081518	24,28,30dB including BGA Via/CaBP_BGAVia_Opt2_28dB
tracy_3ck_01_0119	Traditional Backplane Channels/Std_BP_12inch_Meg7
	Orthogonal Backplane Channels/DPO_IL_12dB
kareti_3ck_01a_1118	Measured Orthogonal Backplane Channels/OAch4
	Measured Orthogonal Backplane Channels/Och4
	Measured Cabled Backplane Channels/CAch3_b2
	Measured Traditional Backplane Channels/Bch2_a7p5_7

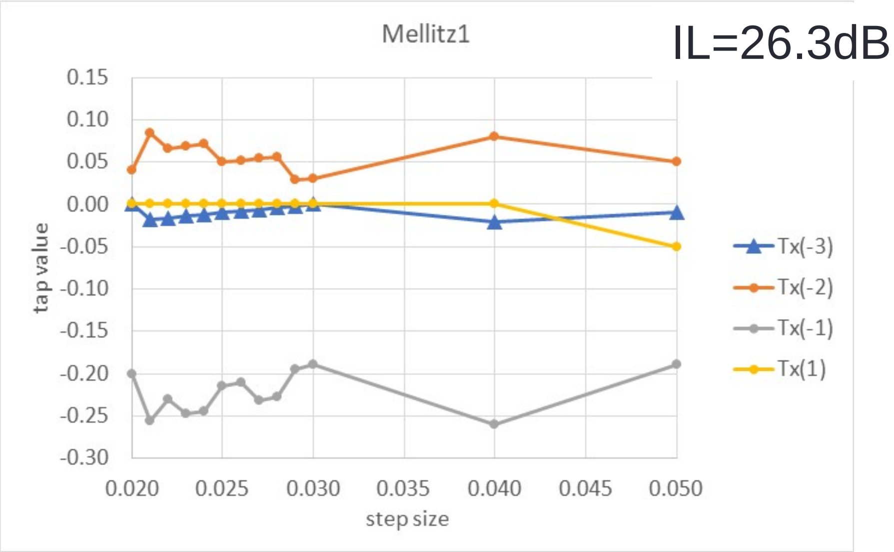
“AZ” channels not in the list

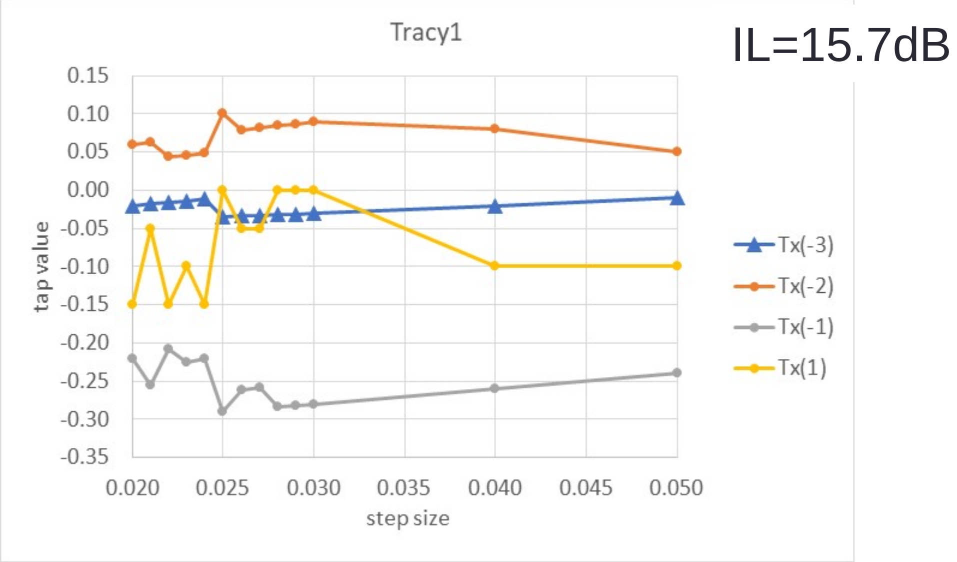
Source: kochuparambil_3ck_01c_0119 slide 5

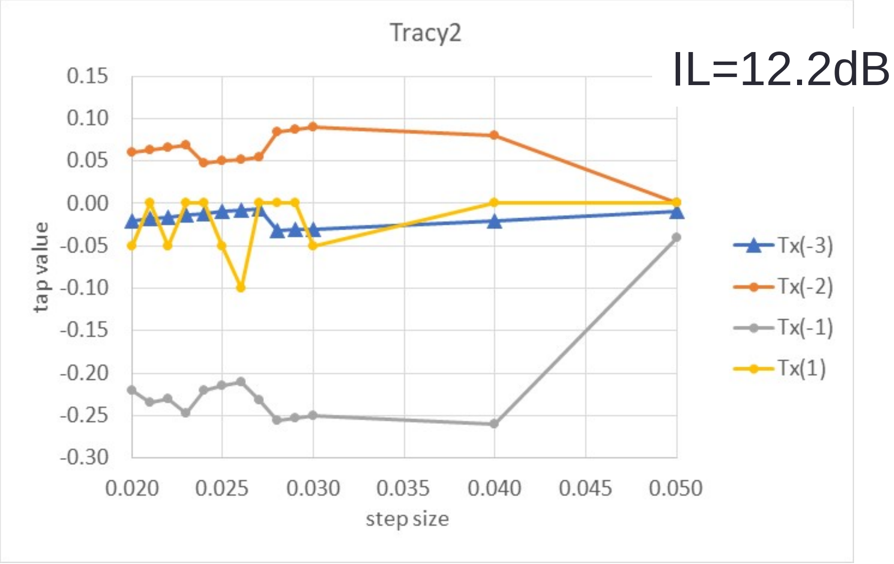
Tap Values By Channel

31/29mm Tx/Rx Package









Tap Values By Channel

31/29mm Tx/Rx Package