In-Depth Analysis of System Impacts of Interleaved FEC for 100G-KR/CR and Potential Solutions

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Background

To mitigate potential burst error issues of multi-tap DFE receivers, a new interleaved RS(544,514) FEC for 100G-KR/CR systems has been proposed in gustlin_3ck_01_0119.

With the new interleaved FEC introduced in 100G-KR/CR, the interoperability and compatibility issues emerge between new and legacy modules as well as between the new defined C2C and C2M interfaces. The FEC converter and 100G MII Extender layer has been proposed to solve the compatibility issue in gustlin_3ck_01_0119.

However, latency concerns have been raised on the interleaved FEC design for 100G KR/CR in lyubomirsky_3ck_01a_0119. However, a system level analysis of this design is still missing.

Besides, another symbol muxing option was also discussed in gustlin_3ck_01_0718. The symbol based solution can also relief the performance concern equivalently. Constrains of DFE Taps are also proposed in lyubomirsky_3ck_01a_0119.

This contribution will provide in-depth analysis of the impacts of interleaved FEC (Cost vs. Gain analysis) from the system perspective and summarize current potential solutions for further study.

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Introduction

- **Robust, stable and simple architecture is always preferred in Ethernet:** Hierarchical governance (MAC, PCS/PMA, PMD), support long-term evolution (LTE). Compatible to legacy MAC & PCS and legacy module when defining new PMDs.
  1. MAC was always preserved;
  2. **PCS (FEC) conformity was always guaranteed.**
  3. PMA (Bit mux) architecture was reserved.
  4. **Keep the module as simply as possible.**

4 golden rules for IEEE 802.3 Ethernet standard development.

- **Impact on the Ethernet standard architecture**: Interleaved FEC for 100G KR/CR will affect the PCS conformity and introduce interoperability and compatibility issues not only for legacy 100G modules, but also for the potential new 100G/lane modules (newly defined C2C and C2M interfaces).
- **Impact on the system design**: Interleaved FEC for 100G KR/CR will introduce system issues.
  1. Mandatory CDR with FEC converter even for unnecessary scenarios.
  2. Complicated CDR will be introduced, more severe in the active copper cable (ACC) modules.
  3. Introduce more latency which may not be tolerable for latency sensitive applications.
  4. May not solve the performance issue, only ~0.2dB SNR gain @1e-15 can be obtained.
- **Potential solutions and summary**

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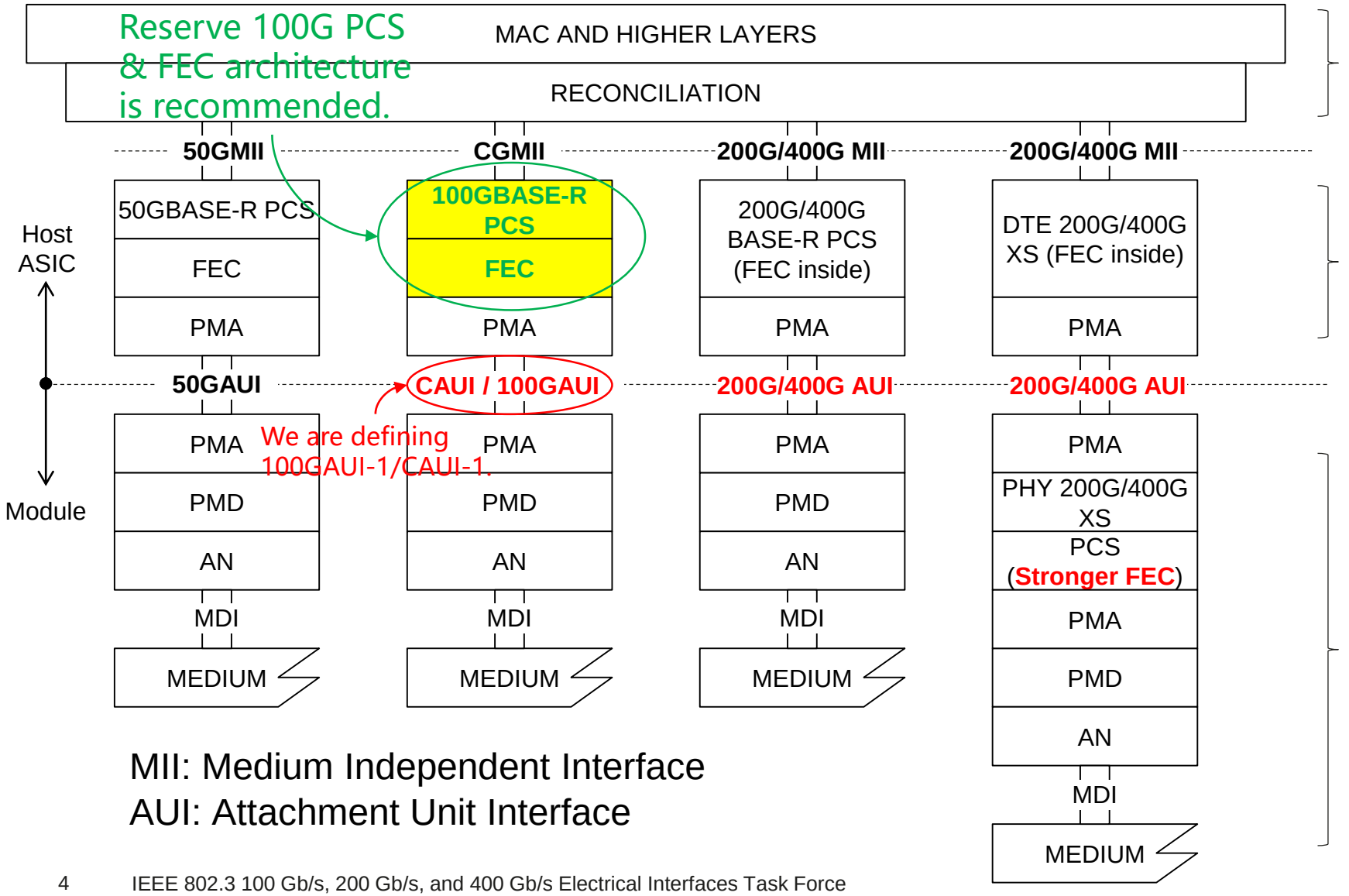
Impact on the Ethernet Standard Architecture



MII: Medium Independent Interface
AUI: Attachment Unit Interface

MAC was always preserved

PCS (FEC) Conformity was always guaranteed

C2M defined by new IEEE 802.3 Task Forces.

Defined by new IEEE 802.3 Task Forces. New PMD

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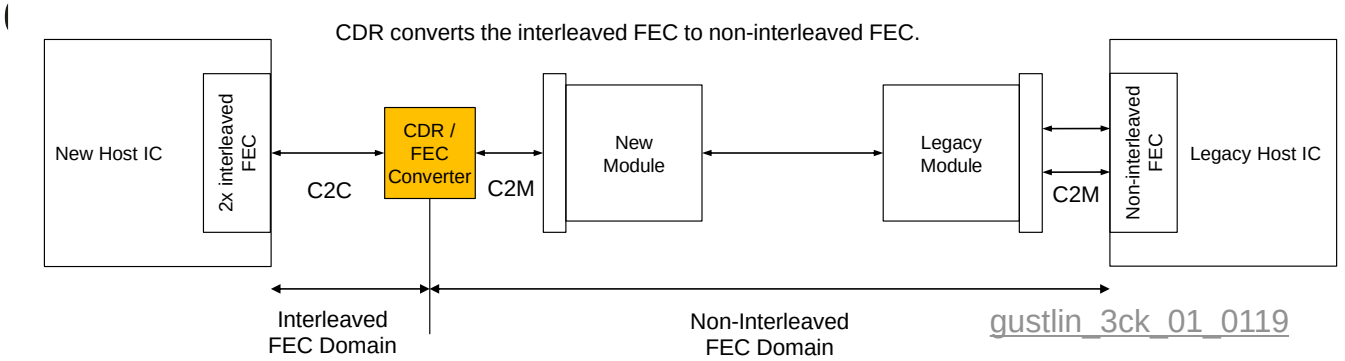
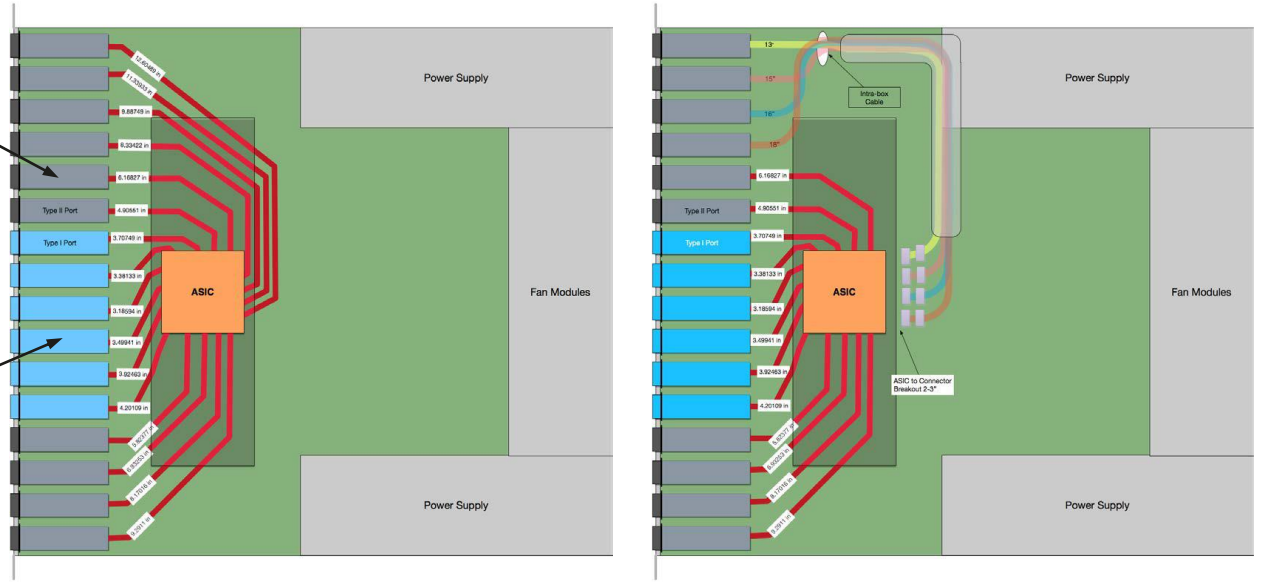
System Concern #1: CDR is neither universal nor preferred for each port in ToR



Type II

Type I



Example ToR board placement from lim_3ck_01b_0718, it is a CDR free design.
Type I: Universal port for both Optics and DAC cables
Type II: Optics/AOC/ACC, no DAC cables

1. The major scenario of 100G KR/CR is the ToR and server interconnection.
2. Interoperability and compatibility issue with the legacy 100G module makes the CDR and FEC converter mandatory.
3. CDR is neither universal nor preferred in ToR design.
4. In real ToR board design, mandatory CDR/FEC converter for each port may not be feasible. The channels using CDRs are probably not difficult channels.
5. Therefore, mandatory “Interleaved FEC" for 100G KR/CR means difficult compatibility with legacy modules. The ‘beauty’ of Ethernet architecture will be lost.

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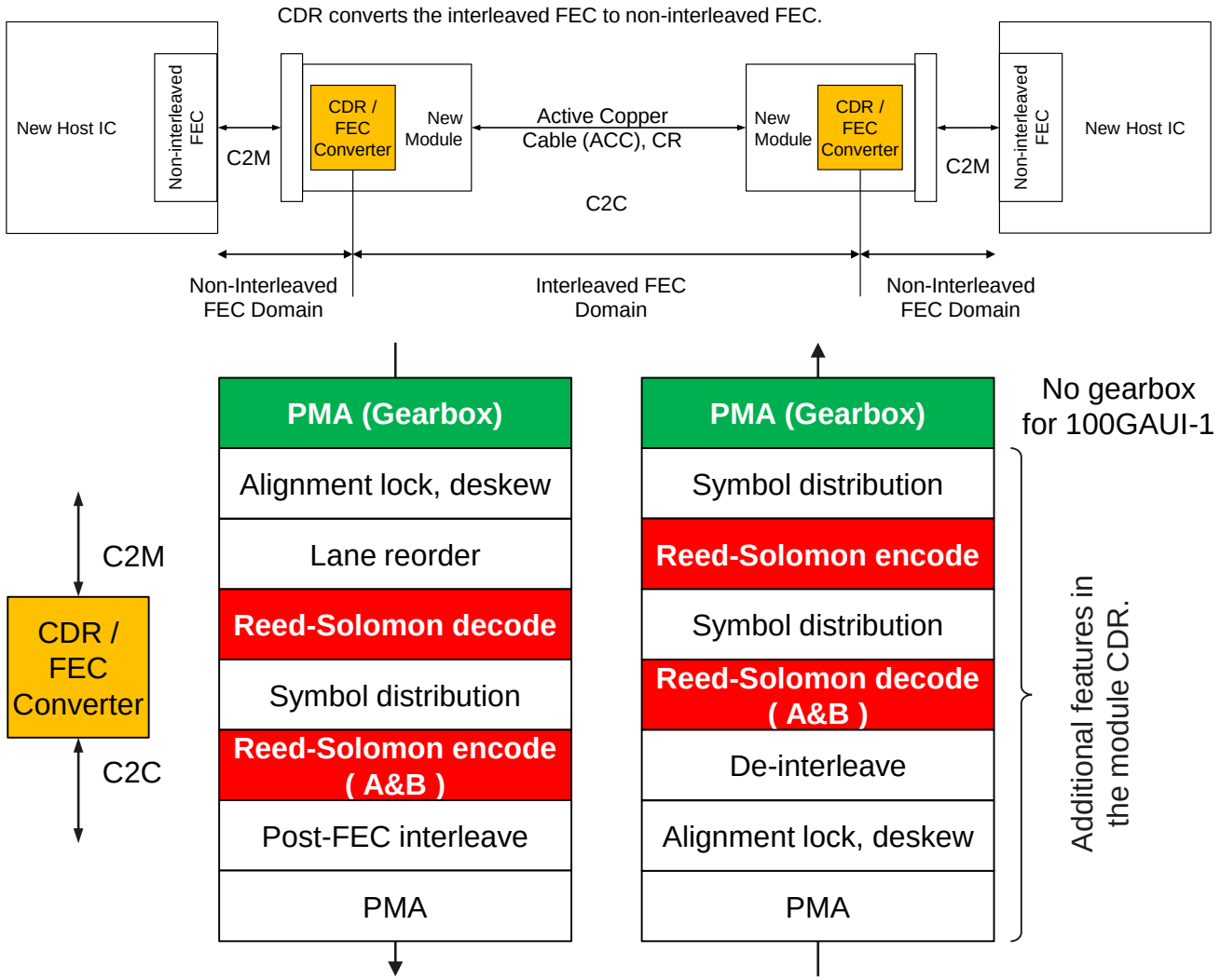
System Concern #2: Interleaved FEC complicates CDR



1. Interoperability and compatibility issue exists between the new defined C2C and C2M for the Active Copper Cable (ACC) scenario.

2. Mandatory 1x FEC to 2x interleaved FEC converter is required in CDR inside the ACC module. (The complexity is the same when CDR is on board.)

3. Gearbox is not needed in 100GAUI-1. (**Do nothing, if current 100G PCS/FEC is reserved.**)

4. FEC converter need 2x 50G RS(544, 514) codec and 1x 100G RS(544, 514) codec in the CDR. (**Introduce much work, if apply interleaved FEC for 100G KR/CR!**)

“Simple function in the module” was the golden rule in Ethernet design!

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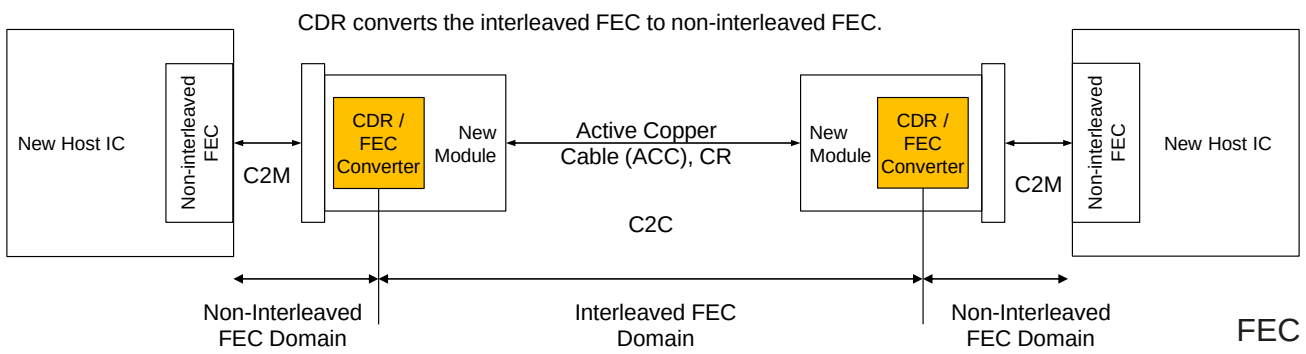
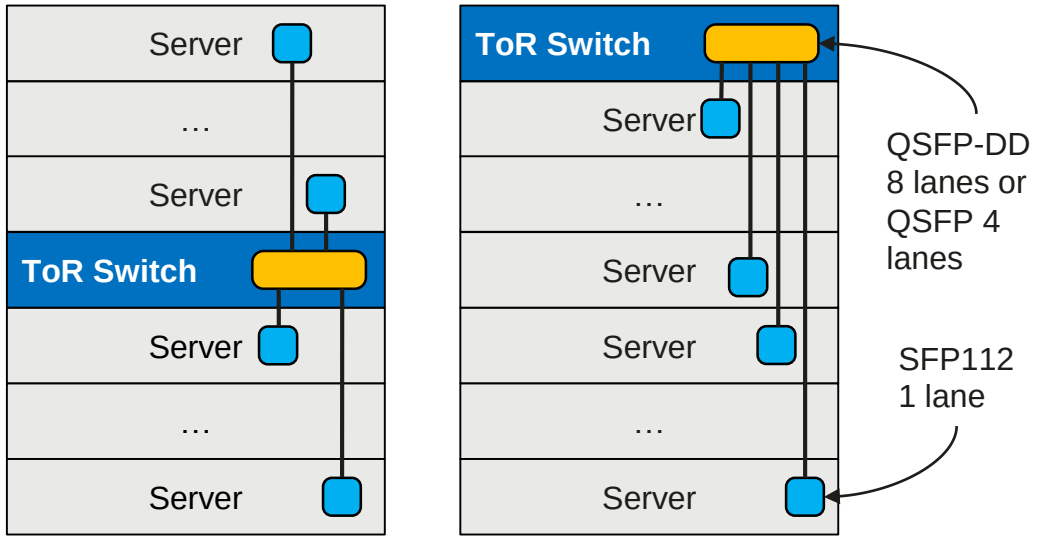
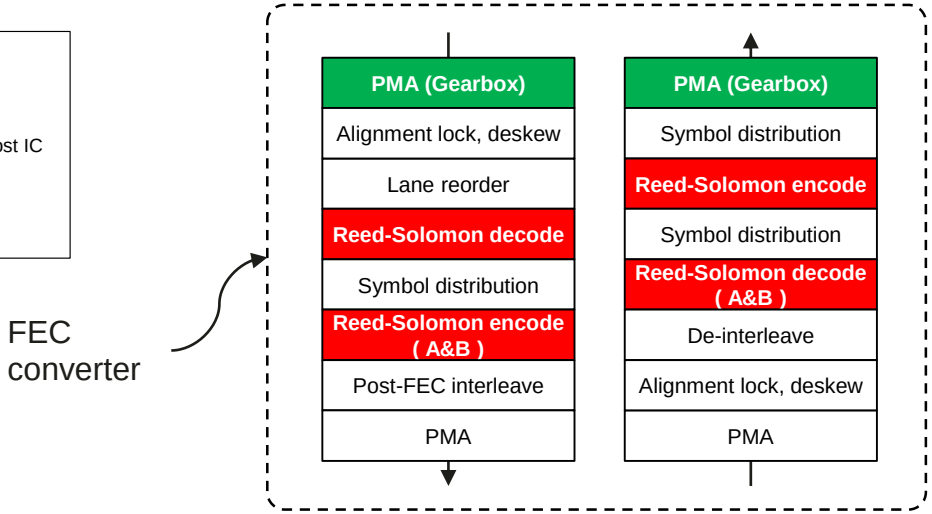
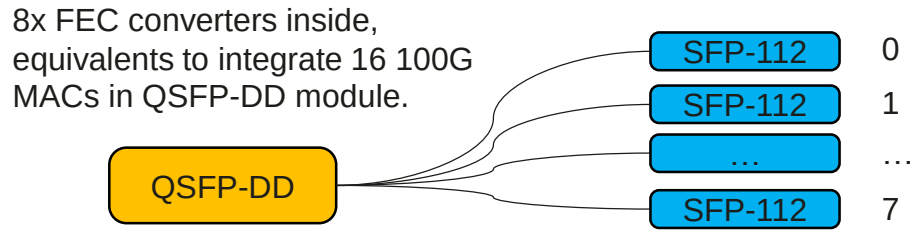
System Concern #2: Interleaved FEC complicates CDR (Cont'd)





Main application scenario of 100G-CR.





- 1x, 2x, 4x and 8x FEC converters are required in SFP112, SFP-DD, QSFP and QSFP-DD ACC module.
- It will make the ACC application less attractive and less competitive compared with active optical cable (AOC)!

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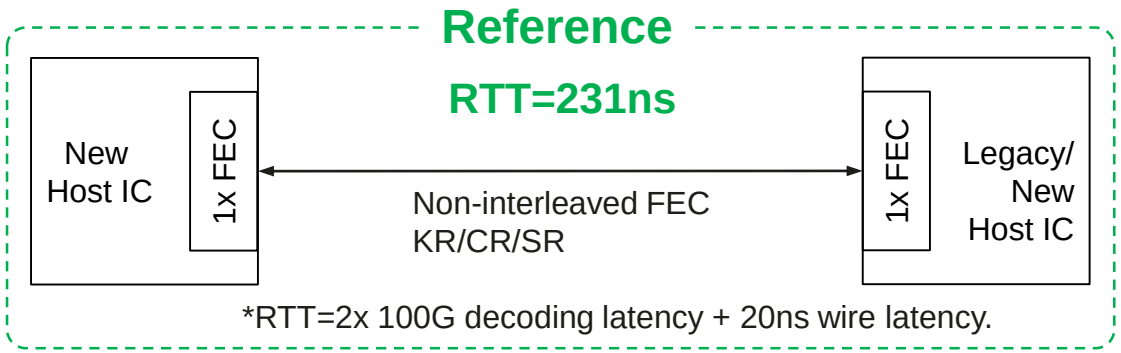
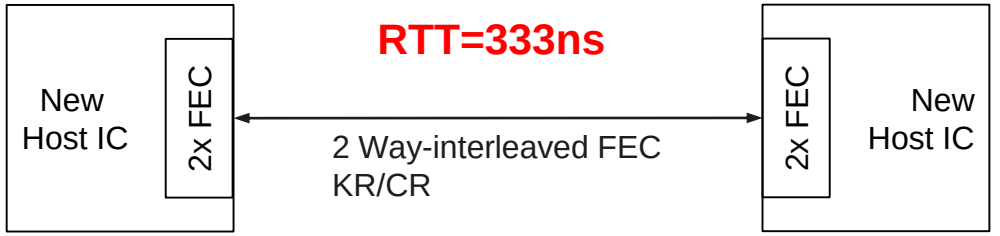
System Concern #3: Interleave FEC introduces more latency

(a)



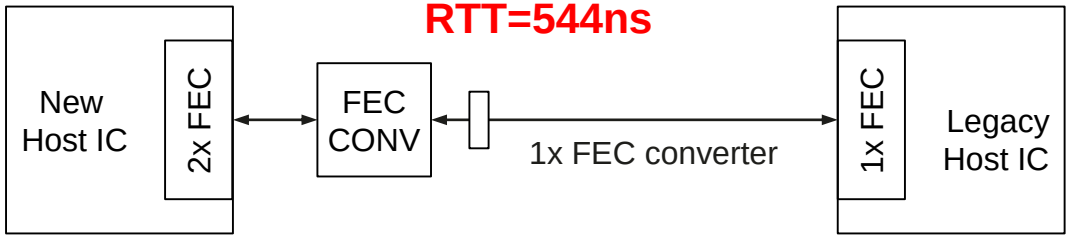
*RTT=2x 100G decoding latency + 20ns wire latency.

(b)



*RTT=2x 50G decoding latency + 20ns wire latency.

(c)



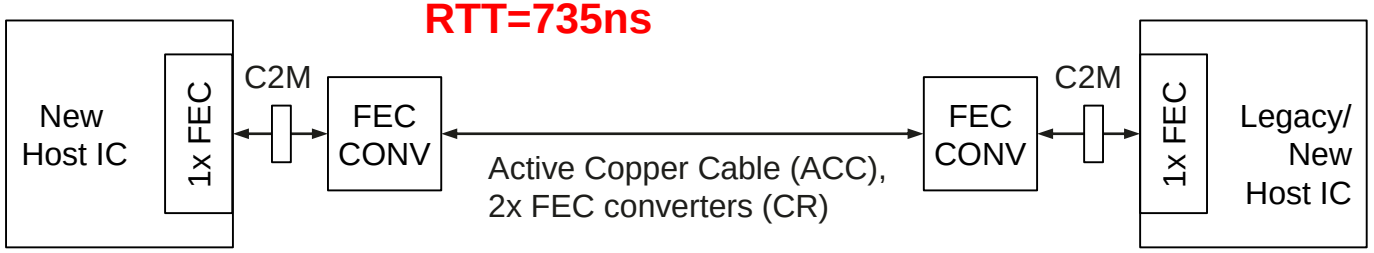
*RTT=2x 50G decoding latency + 2x 100G decoding latency + 20ns wire latency.

RS(544, 514) Decoding Latency

Line Rate (Gbps)	FEC bus width	Clock Period (ns)	Decoding Latency (ns)
106.25	160	1.51	105.41
53.125	80	1.51	156.61

2T+1 cycles are assumed for key equalization solving.
1 cycles is assumed for Chien Search and Forney (Optimistic estimate).

(d)



*RTT=2x 50G decoding latency + 4x 100G decoding latency + 20ns wire latency.

Cases	RTT (ns)	RTT Scale	RTT Delta (ns)
(a)	230.82	1.00x	-
(b)	333.22	1.44x	102.4
(c)	544.04	2.36x	313.22
(d)	734.86	3.18x	504.04

The wire RTT latency is only 20ns for 2m cable. (5ns/meter)
FEC decoding latency is dominant for 100GE KR/CR.
Considering only the decoding delay, optimistic estimate.

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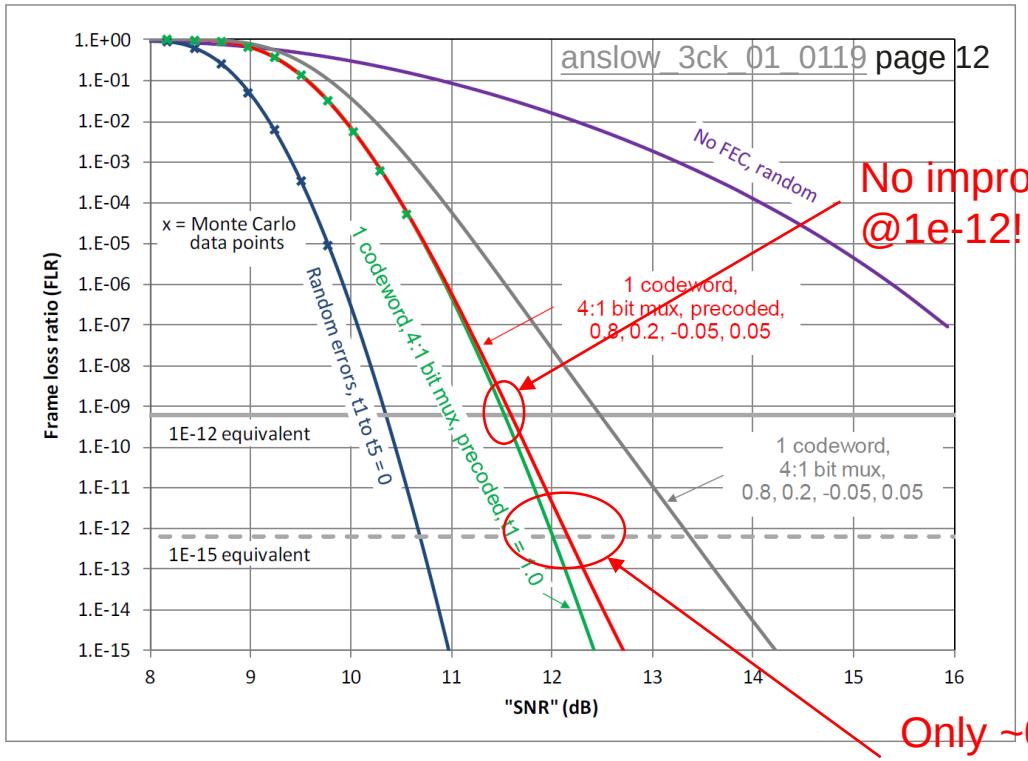
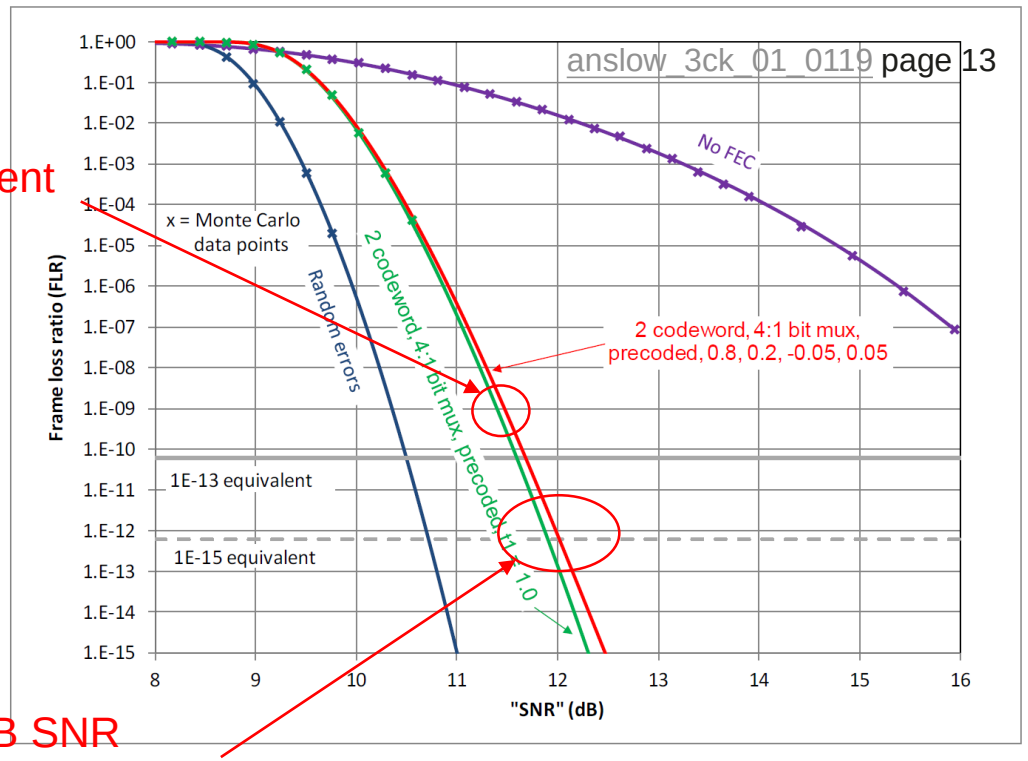
System Concern #4: Interleaved FEC may not solve the performance issue

Non-interleaved FEC + 4:1 bit mux.



2-way interleaved FEC + 4:1 bit mux.



No improvement @1e-12!

Only ~0.2dB SNR improvement @1e-15!

No obvious improvement (~0.2dB@1e-15) can be obtained by introducing 2-way interleaved FEC. We almost get nothing @1e-12, which is the raw BER requirement for 100GE.
If 0.2dB SNR loss still can be a concern, we should firstly look at the >1.2dB SNR loss due to the precoding.

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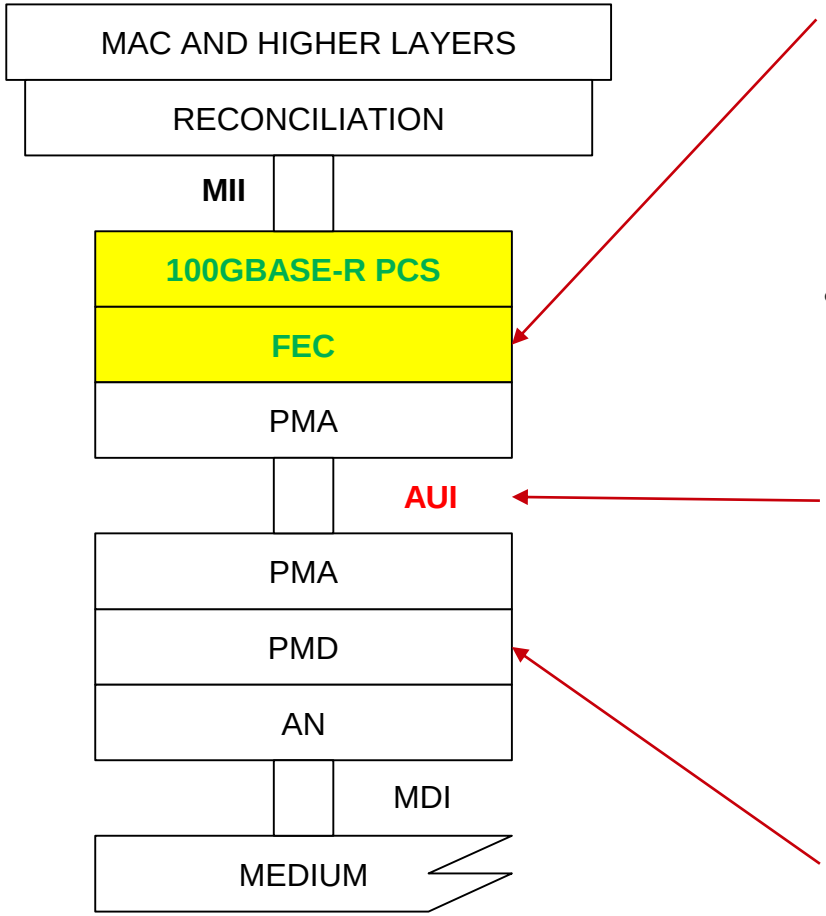
Potential solutions



- Use new FEC (e.g. interleaved FEC) to mitigate potential burst error issues of multi-tap DFE receivers.
  - Large impact on the standard and system.
  - Cost is high. Gain is minor, only 0.2dB@1e-15, almost nothing@1e-12.

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- Direct symbol mapping to the PMD lane will remove the impact of bit-mux PMA. In-depth cost analysis of symbol based solution is needed in further study.
  - Small impact on the standard and system.
  - May simply the complexity of module in some scenarios.

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- Apply constrains to on DFE taps or utilize receiver architectures which are prone to burst error problems.
  - No impact on the standard and system.

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Summary

- Introducing the interleaved FEC for 100G KR/CR brings some system concerns.
  1. Mandatory CDR and FEC converter to support compatibility with the legacy 100G modules and interoperability of new 100G per lane C2C and C2M interfaces.
  2. Complicated CDR are needed. More severe in active copper cable (ACC) modules.
  3. More latency for latency sensitive applications, 2.36x or 313ns more latency compared with non-interleaved FEC scheme (1 FEC CONV); 3.18x or 504ns more latency compared with non-interleaved FEC scheme (2 FEC CONVs).
  4. Gain is minor, only 0.2dB@1e-15, almost nothing@1e-12.

- The benefit of interleaved FEC is minor!
  1. ~0.2dB SNR gain @1e-15.
  2. almost zero SNR gain @1e-12.

- More work is needed to resolve this issue. More analysis of the symbol-based solutions and PMD based solutions e.g. constraining on DFE taps are needed before making a decision.

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