

Discussion on TBDs in Annex 120G

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For IEEE 802.3ck Ad-Hoc

Supporters

Outlines

- Background
- Target Transition Time Analysis
- Summary Table of C2M Test Specifications – Including C2M 50GAUI-1 & 100GAUI-1

Background

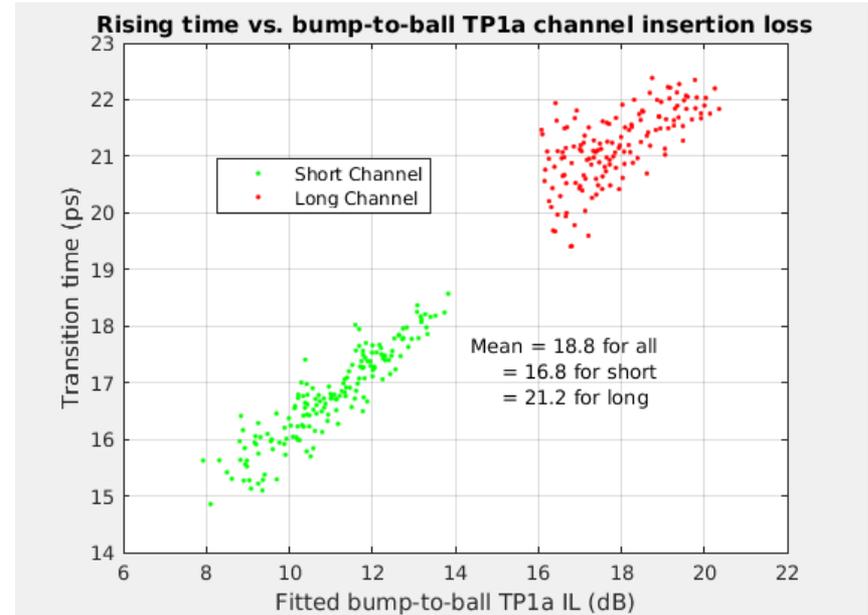
- There are still a lot of TBDs in Annex 120G
 - It requires to fill in those TBDs for technical completeness before D2.0
- Target transition time of Host/Module input stress test
 - Give some directions from experiments on IEEE C2M channels
- Collect specifications of C2M 50GAUI-1 & 100GAUI-1 (in D1.4) & compare
- Purpose: facilitate the discussion & consensus

Channel and Analysis

- Channel (crosstalk included)
 - TP1a analysis for total [nineteen IEEE C2M host-to-module channels](#)
 - Sweep host package trace length, $z_{p1}(TX)$
 - $z_{p1}(TX) = [5:0.5:10 \ 11:1:20 \ 22:2:36]$
 - Total $19 * 29 = 551$ CH+PKG test cases
- COM parameter settings [details in appendix]
 - COM 3.1
 - TP1a: TX Device/PKG + H2M Channels
 - Set 'zero' to related RX PKG & on-die settings
- Analysis
 - Take TP0 to TP1a through channel
 - Good channel only with $VEC \leq 12$ dB & $VEO \geq 8$ mV
 - Calculate 20% ~ 80% transition time (rising & falling times) at TP1a
 - By optimized TX FIR settings
 - Based on 802.3ck D1p4 & Annex 120E

Simulation Results & Target Transition Time

- Show ONLY passed channels here
- Transition time strongly depends on bump-to-ball TP1a insertion loss
- The purpose of ‘target transition time’ spec is to reflect the “real” transition time it may be under input stressed test
 - Taking the average of the transition time of “good” passed channels as “target”
- Due to their different channel IL ranges, short and long channels split into two groups
 - Mean of “short channel” = 16.8 ps
 - Mean of “long channel” = 21.2 ps
- Proposal: adopt 19 ps for target transition time in 120G.3.3.2.1



C2M Test Specs Summary – (Exc. ERL) 50GAUI-1 & 100GAUI-1 (1/2)

		Diff. p2p output voltage (mV, max.)		Slew time (target) or Transition time (min.)	
		50GAUI-1	100GAUI-1	50GAUI-1	100GAUI-1
Host output	Spec @ TP1a (max. volt.)	880	870	10 ps	7.5 ps (min.)
	Xtalk cal. @ TP4 (target)	900	TBD → 900	12 ps (+/- 0.27 V)	TBD ps (+/- TBD V) → ? ps (+/- 0.27 V)
Module output	Spec @ TP4 (max. volt.)	900	900	9.5 ps	7.5 ps (min.)
	Xtalk cal. @ TP1a (target)	880	TBD → 870	19 ps	TBD ps → 19 ps (20% ~ 80%)
Host input	In Spec @ TP4a	-	-	-	-
	Sig. cal. @ TP4 (min.)	900	900	-	-
	Xtalk cal. @ TP1a (target)	880	TBD → 870	19 ps (20% ~ 80%)	TBD ps → 19 ps (20% ~ 80%)
Module input	In Spec @ TP1	-	-	10.5 ps (20% ~ 80%)	9 ps (20% ~ 80%) (min.)
	Sig. cal. @ TP1a (min.)	900	900	-	-
	Xtalk cal. @ TP4 (target)	900	TBD → 900	12 ps (+/- 0.27 V)	TBD ps (+/- TBD V) → ? ps (+/- 0.27 V)

PS: The values in RED are the proposed values.

C2M Test Specs Summary – (Exc. ERL) 50GAUI-1 & 100GAUI-1 (2/2)

		EH (min)		VEC (max)	
		50GAUI-1	100GAUI-1	50GAUI-1	100GAUI-1
Host out	Out Spec @ TP1a	32 mV	15 mV → 8 mV *2	12 dB	9 dB → 12 dB *2
Module out	Out Spec @ TP4	Near-end: 70 mV Far-end: 30 mV	24 mV → ?? mV *3	-	7.5 dB → ?? dB *3
Host in	Sig. cal. @ TP4	Near-end: - Far-end: 30 mV	24 mV → ?? mV *3	-	7.5 dB → ?? dB *3
Module in	Sig. cal. @ TP1a	32 mV	15 mV → 8 mV *2	12 dB	9.0 ~ 9.5 dB *1 → 12 ~ 12.5 dB *2

PS: The values in RED are the proposed values.

1* This spec had been proposed by Mike Dudek by #10062 against D1.1 & adopted in D1.2. Due to VEC at TP1a is more critical for end to end performance than just the eye opening. Add VEC (max) & VEC (min) in the table.

2* The detailed analysis can be found in wu_3ck_01_0121.pdf

3* We may apply the similar analysis to derive the EH & VEC for module output & host input

Summary

- Propose to adopt slides 7 & 8 to modify 120G

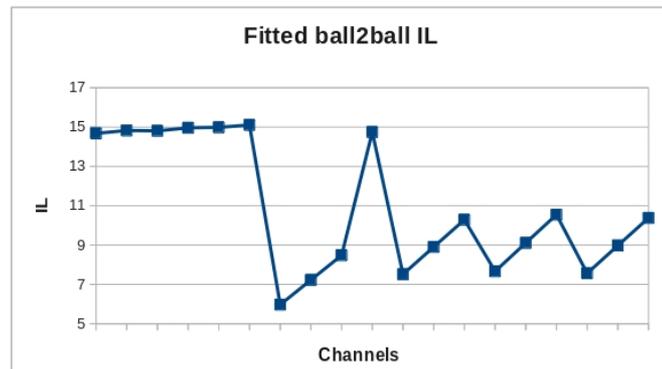
Thank You



C2M Host-to-Module Channels for Analysis

- Short Channel
- Long Channel

Contribution	Zip files	Channel	SxP Files		
lim_3ck_01a_0319	lim_3ck_01_0319_c2m.zip	Tx7_L10	112G_16dB_(QSPDD+module card)_TX7_L10	●	
		Tx7_L23	112G_16dB_(QSPDD+module card)_TX7_L23	●	
		Tx3_L10	112G_16dB_(QSPDD+module card)_TX3_L10	●	
		Tx3_L23	112G_16dB_(QSPDD+module card)_TX3_L23	●	
		Tx7_Asic	112G_16dB_(QSPDD+module card)_TX7_Asic	●	
		Tx3_Asic	112G_16dB_(QSPDD+module card)_TX3_Asic	●	
lim_3ck_adhoc_01_	073119 lim_3ck_adhoc_02_073119.zip	Ch5a_2"	Channel5a_Smaller_Pad_2inch_trace	●	
		Ch5b_3"	Channel5b_Smaller_Pad_3inch_trace	●	
		Ch5c_4"	Channel5c_Smaller_Pad_4inch_trace	●	
		Ch5d_9"	Channel5d_Smaller_Pad_9inch_trace	●	
akinwale_3ck_adhoc_01a_08282019	akinwale_3ck_C2M_channels_TP0a_100ohms_08222019.zip	2"100Ohm	C2M_2p0in_100Ohm_thru1.s4p	●	
		3"100Ohm	C2M_3p0in_100Ohm_thru1.s4p	●	
		4"100Ohm	C2M_4p0in_100Ohm_thru1.s4p	●	
		2"85Ohm	C2M_2p0in_85Ohm_thru1.s4p	●	
	akinwale_3ck_C2M_channels_TP0a_85ohms_08222019.zip	3"85Ohm	C2M_3p0in_85Ohm_thru1.s4p	●	
		4"85Ohm	C2M_4p0in_85Ohm_thru1.s4p	●	
		akinwale_3ck_C2M_channels_TP0a_93Ohms_08222019.zip	2"93Ohm	C2M_2p0in_93Ohm_thru1.s4p	●
			3"93Ohm	C2M_3p0in_93Ohm_thru1.s4p	●
		4"93Ohm	C2M_4p0in_93Ohm_thru1.s4p	●	



COM Settings – TP1a

Table 93A-1 parameters				I/O control			Table 93A-3 parameters			Floating Tap Control			
Parameter	Setting	Units	Information	Parameter	Setting	Units	Parameter	Setting	Units	Parameter	Setting	Units	Information
f_b	53.125	GBd		DIAGNOSTICS	1	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]		N_bg	0	0.12 or 3 groups	
f_min	0.05	GHz		DISPLAY_WINDOW	0	logical	package_tl_tau	6.14E-03	ns/mm	N_bf	3	taps per group	
Delta_f	0.01	GHz		RESULT_DIR	results100GEL_C2M_host_1\data		package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm	N_f	40	span for floating taps	
C_d	[1.2e-4 0]	nF	[TX RX]	SAVE_FIGURES	0	logical	ICN & FOM_ILD parameters			brmsq	0.2	FE value for floating taps	
L_s	[0.12 0]	nH	[TX RX]	Port Order	[1 3 2 4]		f_v	0.594	*Fb	for TP4-->			
C_b	[0.3e-4 0]	nF	[TX RX]	RUNTAG	C2M_eval		f_f	0.594	GHz f_r specified in first column	[1.2e-4 0]	nF	[TX RX]	
z_p select	[12]		[test cases to run]	COM_CONTRIBUTION	0	logical	f_n	0.594	GHz	[0.12 0]	nH	[TX RX]	
z_p (TX)	[12 16; 18 18]	mm	[test cases]	Local Search	2		f_2	40	GHz	[0.3e-4 0]	nF	[TX RX]	
z_p (NEXT)	[0.0 ; 0.0]	mm	[test cases]	Operational				A_ft	0.600	v	[12 3]		[test cases to run]
z_p (FEXT)	[12 16; 18 18]	mm	[test cases]	VEC Pass threshold	9	db	A_nt	0.600	v	[2 7 8]	mm	[test cases]	
z_p (RX)	[0.0 ; 0.0]	mm	[test cases]	EH_min	15	mV				[0 0 0]	mm	[test cases]	
C_p	[0.87e-4 0]	nF	[TX RX]	ERL Pass threshold	7.3	dB				[2 7 8]	mm	[test cases]	
R_0	50	Ohm		DER_0	0.00001					[0 0 0]	mm	[test cases]	
R_d	[50 50]	Ohm	[TX RX]	T_r	0.0075	ns				[0 0 87e-4]	nF	[TX RX]	
A_v	0.415	V	vpl/vfs: 694	FORCE_TR	1	5							
A_fe	0.415	V	vpl/vfs: 694	PMD_type	C2M								
A_ne	0.608	V		BREAD_CRUMBS	0	logical							
L	4			SAVE_CONFIG2MAT	1	logical							
M	32	Samp/UI		PLOT_CM	0	logical							
samples_for_C2M	100	Samp/UI		TDR and ERL options									
T_0	50	mUI		TDR	1	logical							
AC_CM_RMS	0	V	[test cases]	ERL	1	logical							
filter and Eq				ERL_ONLY	0	logical							
f_r	0.75	'yb		TR_TDR	0.01	ns							
cf(0)	0.54		min	N	800								
cf-1)	[-0.2,0.02,0]		[min:step:max]	beta_x	0								
cf-2)	[0.0,0.02,0.1]		[min:step:max]	rho_x	0.618								
cf-3)	[0]		[min:step:max]	fixtms delay time	[0 0.2e-9]	[port: port2]							
cf()	[-0.10,0.02,0]		[min:step:max]	TDR_V_TXPKG	1								
N_b	4	UI		N_bw	0	UI							
b_max(1)	0.4	As/dffe1		Tukey_window	1								
b_max(2..N_b)	[0.15 0.10 0.1]	As/dfez..N_b		Receiver testing									
b_min(1)	0.1	As/dffe1		RX_CALIBRATION	0	logical							
b_min(2..N_b)	[-0.15 - 0.05 - 0.05]	As/dfez..N_b		Sigma BBN step	5.00E-03	V							
g_DC	[-13:1:0]	dB	[min:step:max]	Noise, jitter									
f_z	12.58	GHz		sigma_RJ	0.01	UI							
f_p1	20	GHz		A_DD	0.02	UI							
f_p2	28	GHz		eta_0	4.10E-08	V^2/GHz							
g_DC_HP	[-30.5:0]		[min:step:max]	SNR_TX	32.5	dB							
f_HP_P2	1.378125	GHz		R_LM	0.95								
G_Qual	[-2 -9 ; -2 -12 ; -4 -12 ; 6 -12]	dB	ranges										
G2_Qual	[0 -1 -2 -3]	dB	ranges										