

# Suggested Packages for 100GEL

Liav Ben Artsi, Marvell Israel Ltd

Richard Mellitz, Samtec

07/25/2018

# Suggested PKG Model Cases

	Length	Ball Side Discontinuity	Xtalk (Suggest using random noise)	Suggested Decision & (Priority)
PHY <b>(WIP)</b>	8-12mm	Low Pitch BGA	High	A Must have for high reflections & Xtalk (1)
Typ Switch	20mm	1mm pitch BGA	Medium	Check if covered by any of the 30mm (2)
High Lane Count Switch up to 70x70mm <b>(WIP)</b>	30mm	1mm pitch BGA	Low	Provide an initial model to check for impact (1)
High Lane Count Switch > 70x70	30mm	LGA	Low	Discuss whether should be covered (3). if yes... How? If not... how to manage the impact?

# Future Large 100G/lane Devices

- Big packages will be one possible target implementation for 100Gbps/lane
- Need to consider the implications of a decision not to model future LGA
- [https://www.ectc.net/files/68/ECTC\\_2018\\_Luncheon\\_Keynote\\_BCOoi\\_Broadcom.pdf](https://www.ectc.net/files/68/ECTC_2018_Luncheon_Keynote_BCOoi_Broadcom.pdf)

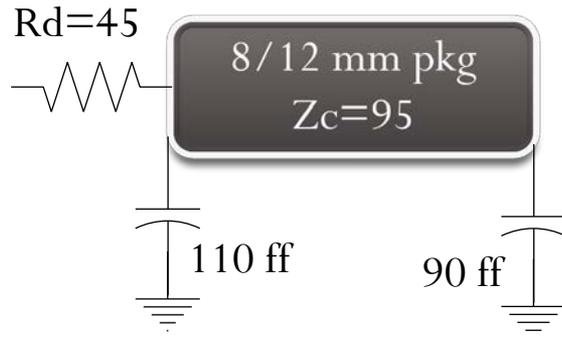
IC Package Need	2018	2022	Challenges
<b>Data Rate</b> 	56 Gbps	112 Gbps	<ul style="list-style-type: none"> <li>• Channel Insertion Loss &amp; Return Loss</li> <li>• Crosstalk</li> <li>• Power Integrity</li> </ul>
<b>Body Size</b> 	67.5mm x 67.5 mm	> 90mm x 90mm	<ul style="list-style-type: none"> <li>• Package Warpage</li> <li>• Board Level Reliability</li> <li>• Socket Cost &amp; Performance Penalty</li> </ul>
<b>2.5D Integration</b> 	Up to 5 dies	More/Larger dies (incl. Optical)	<ul style="list-style-type: none"> <li>• Interposer Reticule Size</li> <li>• Assembly challenges</li> <li>• More Memory BW</li> </ul>
<b>Micro-bump Pitch</b> 	40um	<=30um	<ul style="list-style-type: none"> <li>• Assembly challenges</li> <li>• Routing challenges</li> </ul>
<b>Power Dissipation</b> 	300 W	> 500 W	<ul style="list-style-type: none"> <li>• Thermal Interface Material</li> <li>• Heatsink Solutions</li> </ul>

# Nominal or WorstCase?

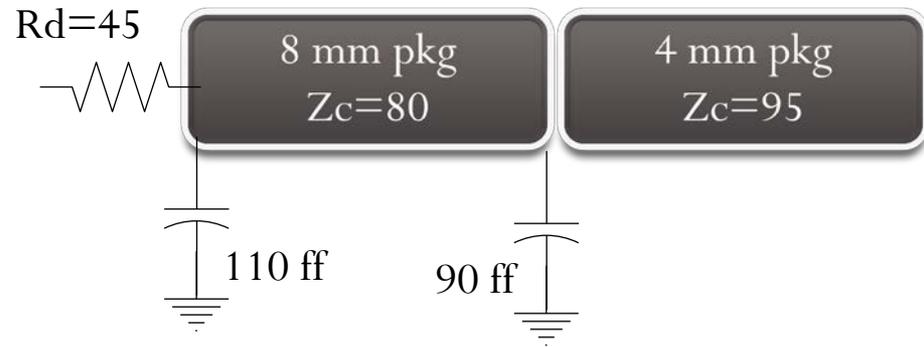
- We may consider starting with a nominal/slight worst case parameters package and evaluate the manufacturing/implementation variance COM impact
- Impact of model simplicity (for example having multiple discontinuities integrated into one) once proven should be:
  - Taken as a part of the COM margin
  - or
  - Suggest a model correction
- Crosstalk per PKG case suggested to be implemented as random noise with the applicable  $\sigma$

# Single Ended Package Model WIP

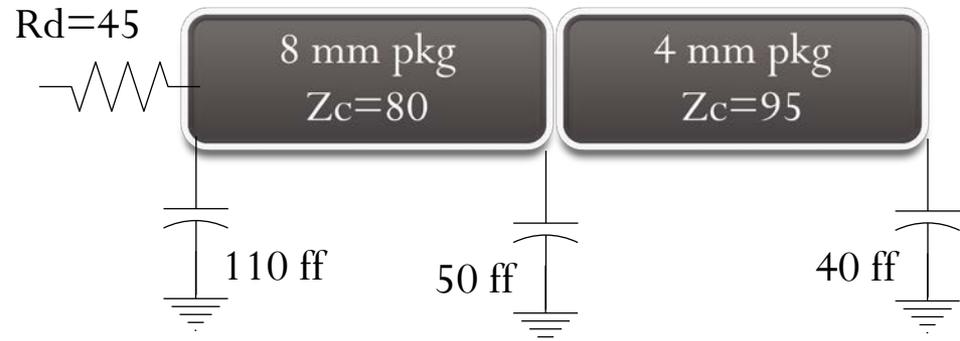
Option A  
Two Test Cases



Option B  
One Test Case



Option C  
One Test Case



- Should values for  $\alpha_1$ ,  $\alpha_2$ , and  $\tau$  be adjusted?
- What should the values for  $Z$ ,  $C$ , and lengths be for these?

Thank You!