TRANSMIT EQUALIZER STEP SIZE SPECIFICATIONS (COMMENTS #62, #63, #74, #10249)

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Background

- Tx equalization maximum step size specification was 5% in 50G electrical PMDs (clauses 136, 137, also annex 120D)
  - c(-2) was specified as 2.5%.
- In 802.3ck:
  - Following hidaka_3ck_adhoc_01_120518 and sun_3ck_adhoc_01a_120518 all analysis assumed a 2% step size for c(-3) through c(0), and this value was included in the baseline proposal heck_3ck_03b_0319.
    - 5% for c(+1)
  - The 2% step size can create an additional burden on DAC-based transmitters. Power impact estimated as ~0.5 pJ/bit.
  - In ran_3ck_adhoc_01_021920 we have shown that step size has small and very irregular effect on COM results.
  - Comments #62, #63, #74, #10249 against D1.1 address Tx equalization step sizes.

Goals of this presentation

- In ran_3ck_adhoc_01_021920 it was stated that "Moving from 2.5% to 2% requires an additional DAC bit, otherwise some steps will have no measurable effect."
  - Feedback received suggested that the additional bit may be required only in digital calculations, and not necessarily in the DAC, by rounding the calculated FFE output to 7 bits.
  - The claim about "no measurable effect" was indeed incorrect.
  - Rounding will be discussed in the following (spoiler: possible, but with increased Tx noise).
- Other comments suggest that having a 5% step size for c(+1) alone does not benefit Tx design and can create unexpected complexity for optimization algorithms.
  - This will be explained.

Possible designs choices

To meet a 2.5% step size specification

- 7-bit integer 2-tap FFE calculation can work as follows:
  - Input is {-3, -1, +1, +3}
  - Coefficients are 0:0.5:21 (42 values) for c(0), and -5:0.5:0 (11 values) for c(-1)
    - Normalized step size is 1/42 = 2.38%
  - Output range is 21*3 – 21*(-3)=126
  - Output is shifted to an unsigned range of 0 to 126 (so the value 63 corresponds to zero differential output)

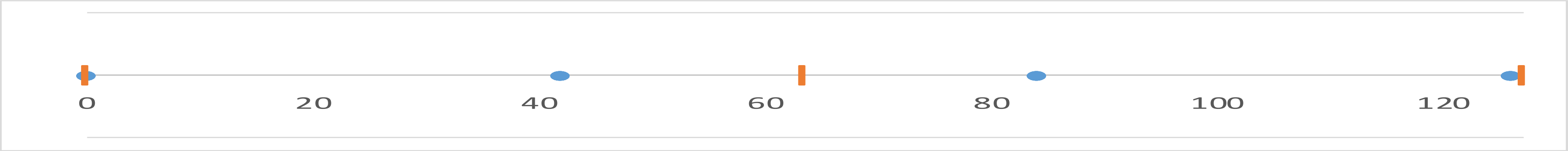
To meet a 2% step size specification

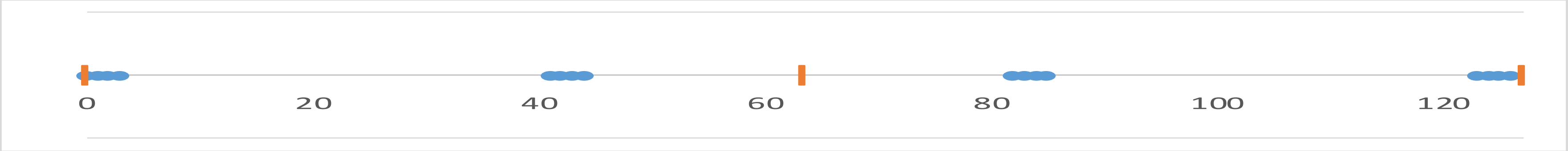
- 8-bit integer FFE calculation is required:
  - Input is {-3, -1, +1, +3}
  - Coefficients are 0:0.5:42.5 (85 values) for c(0), and -10:0.5:0 (21 values) for c(-1)
    - Normalized step size is 1/85 = 1.18%
  - Output range is 42.5*3 – 42.5*(-3)=255
  - Output is shifted to an unsigned range of 0 to 255 (so the value 127.5 corresponds to zero differential output)

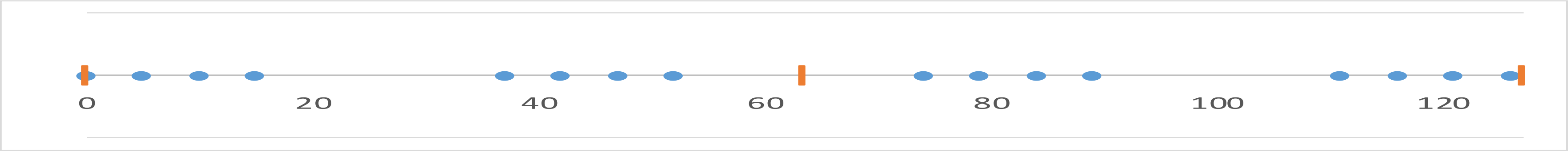
Results of 7-bit design

- Outputs for different coefficient combinations:

c(-1)	c(0)	NRZ outputs	PAM4 outputs
0	21	0; 126	0; 42; 84; 126
-0.5	20.5	0, 3; 123, 126	0, 1, 2, 3; 41, 42, 43, 44; 82, 83, 84, 85; 123, 124, 125, 126
-2.5	18.5	0, 15; 111, 126	0, 5, 10, 15; 37, 42, 47, 52; 74, 79, 84, 89; 111, 116, 121, 126



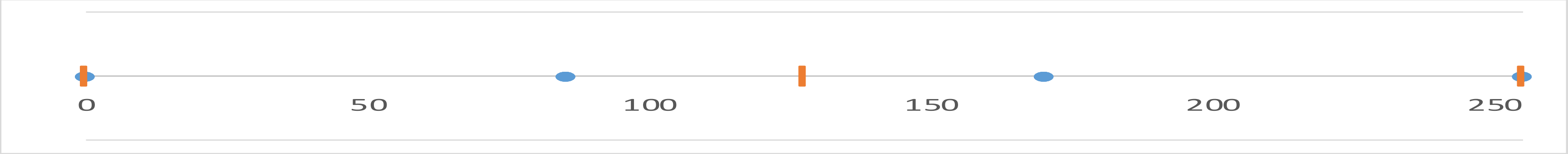


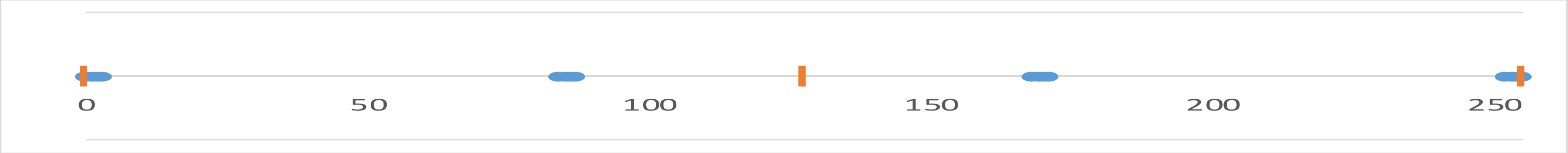


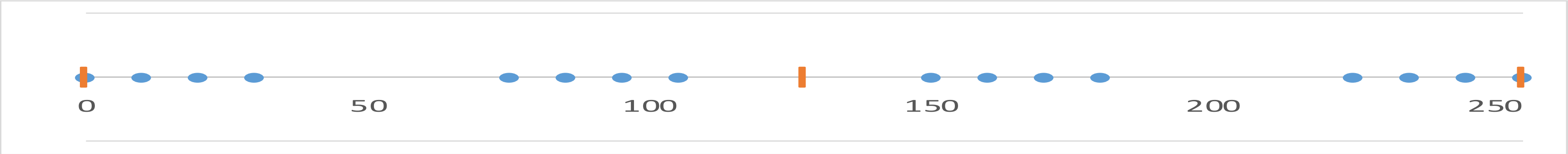
Results of 8-bit design

- Outputs for different coefficient combinations:

c(-1)	c(0)	NRZ outputs	PAM4 outputs
0	42.5	0; 255	0; 85; 170; 255
-0.5	42	0, 3; 252, 255	0, 1, 2, 3; 84, 85, 86, 87; 168, 169, 170, 171; 252, 253, 254, 255
-5	37.5	0, 6; 249, 255	0, 10, 20, 30; 75, 85, 95, 105; 150, 160, 170, 180; 225, 235, 245, 255







What if output DAC is 7 bits?

With 7-bit calculation

- FFE calculation is fed directly to DAC
  - Pure linear system, no additive noise
- Equalization control is more coarse than with 8 bits
  - But, as we have shown, with the Rx adaptive equalization the result may actually be better

With 8-bit calculation

- Outputs have to be divided by 2
  - Problem: some outputs are even, some are odd
  - Truncation error is either 0 or 1 LSB depending on input sequence ➔ additive quantization noise
  - With RMS=$\frac{1}{\sqrt{2}}$ LSB, effect on SNDR is small – but this quantization noise can't be mitigated by the Rx
- More refined equalization control is not necessarily beneficial
- More expensive digital calculations

What about c(+1)?

- If the max step size is >2x larger than the rest, implementations may actually apply double steps
- This creates complications for receivers trying to optimize Tx equalization
- Suppose the receiver wants to sweep possible values of c(+1) starting from preset 1:
  - Prior to decrementing c(1), c(0) must be decremented
    - In the Tx (unlike COM calculation) c(0) is not automatically determined from other coefficients
  - If step sizes are the same, one decrement of c(+1) requires one decrement of c(0)
  - If c(1) has 2x step size, one decrement of c(+1) requires two decrements of c(0)
  - Step sizes can vary even more… although there is no real design benefit.
- The Rx has no way to tell how the Tx is implemented
  - Uncertainty exists regardless of the “search” algorithm.
  - Planning for all possible combinations is difficult; validation is a nightmare.
- This could also be done with uniform step size limits… but is less “tempting”
  - We should add a recommendation to have uniform step sizes

Summary

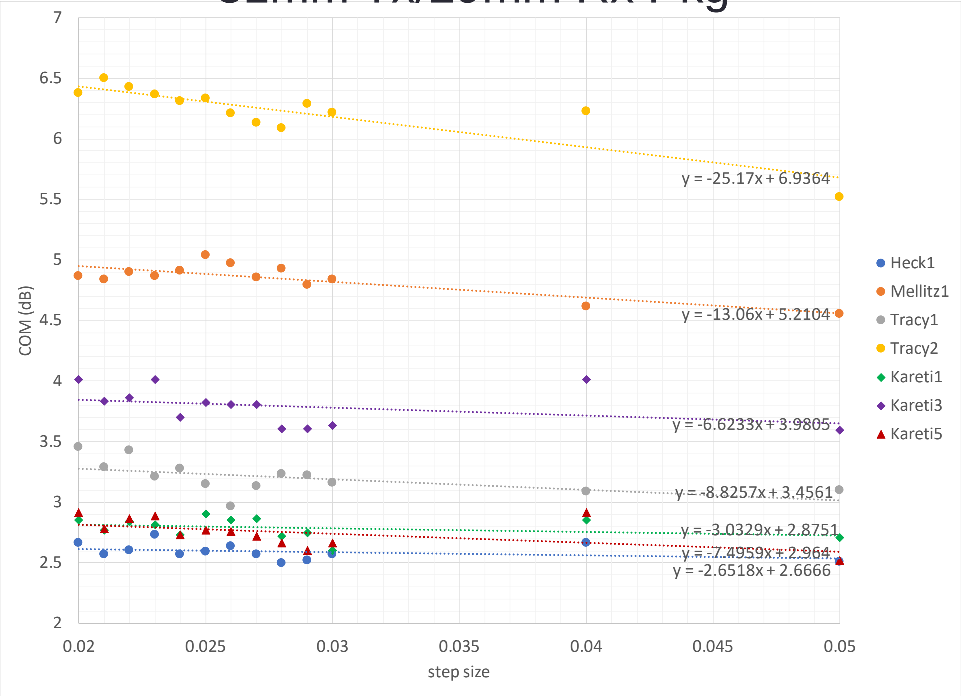
- Current max step size spec of 2% is overly aggressive
  - For a digital implementation, requires at least 8-bit calculations, if not 8-bit DAC
  - Changing to max 2.5% would enable full 7-bit design with negligible impact (if any) on Rx
  - Finer steps have no real benefit, and cost power
  - COM grid is not necessarily related, but run time can be reduced by changing to 2.5%
- Allowing c(+1) to have larger steps creates unexpected complexity in Rx optimization
  - COM grid is not related; can stay with a larger step to reduce run time
- Recommended changes in D1.1→D1.2:
  - In transmitter characteristics
    - Use uniform step size specs for all taps
    - Change absolute step size spec to min 0.005 and max 0.025
    - Add a recommendation to use nominally equal step sizes, to enable simple “step counting” logic
      - Use editorial license
  - In COM
    - Change search step to 2.5% for all precursor taps
  - Apply the above for clause 162, clause 163, and annex 120G

BACKUP

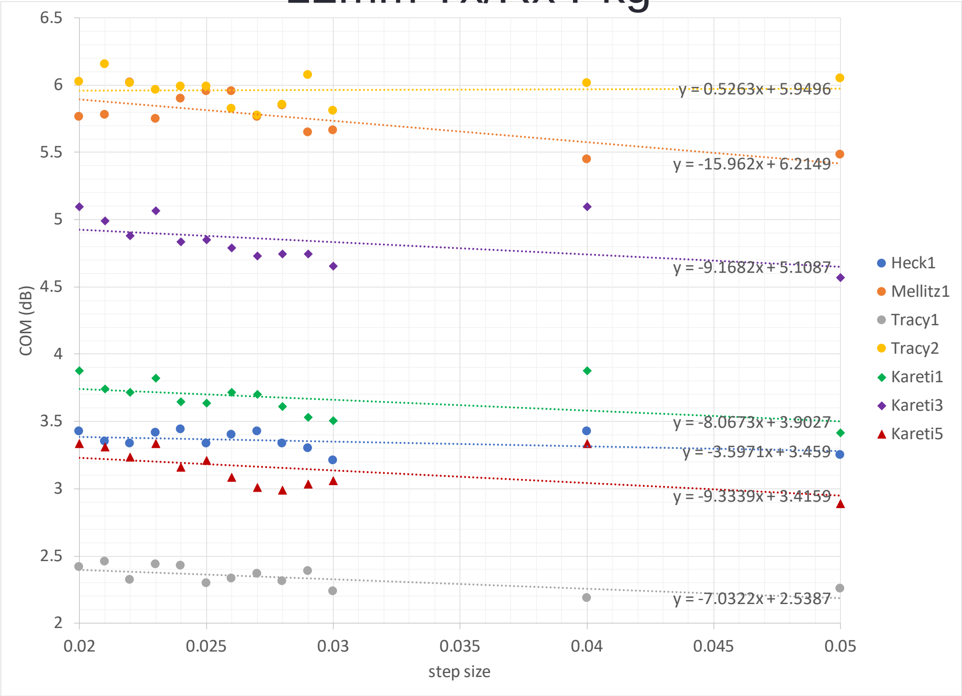
From ran_3ck_adhoc_01_021920

Results

31mm Tx/29mm Rx Pkg



12mm Tx/Rx Pkg



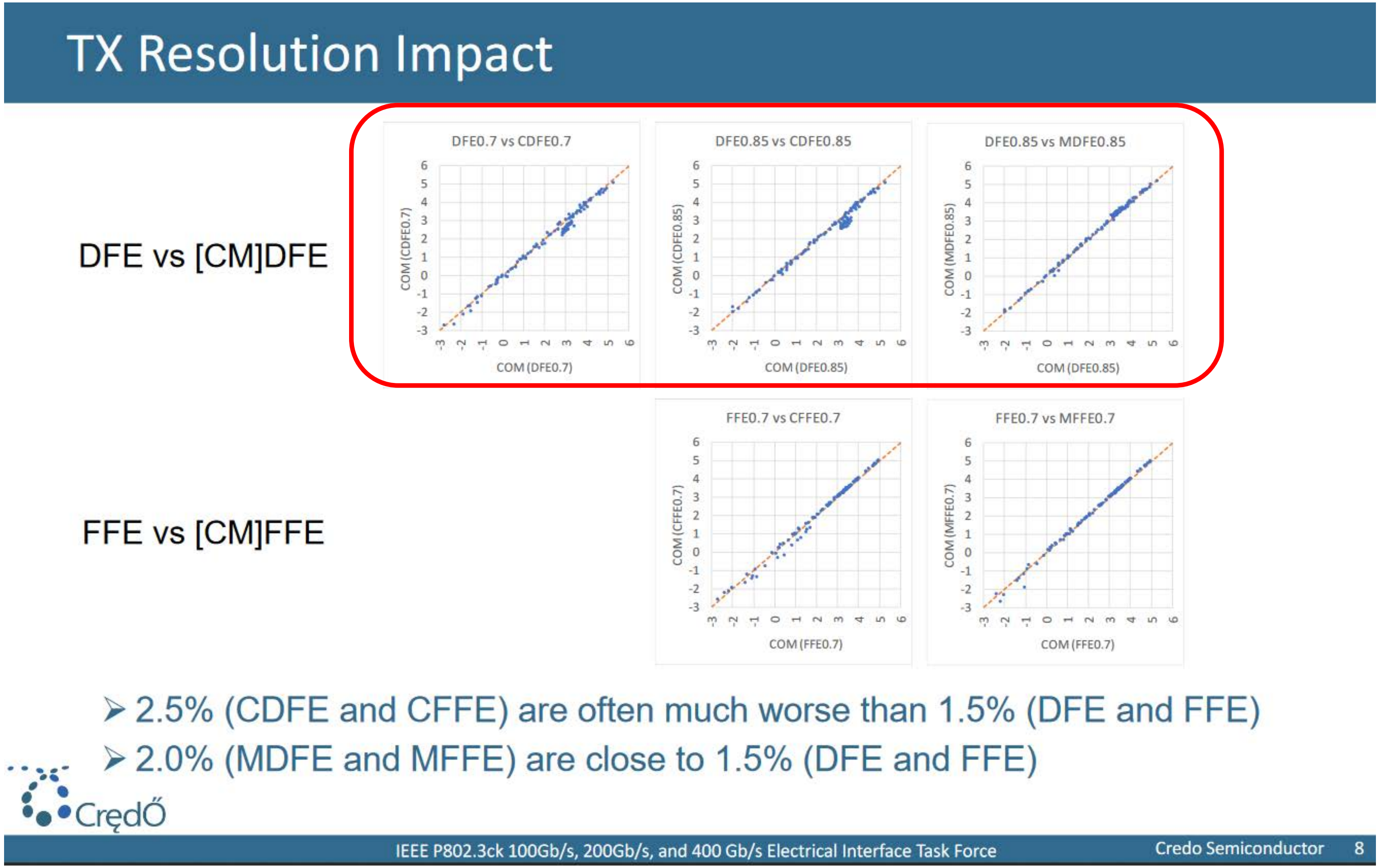
In both cases, COM vs. step size trend is very small in all channels

Effect of 2% to 2.5% is between ~0.05 dB (for low COM channels) and 0.13 dB (for the high COM channel)

Results are very “noisy” and inconclusive even at relatively large steps (R^2 maximum value was only ~0.75; most were much worse)

From ran_3ck_adhoc_01_021920

What was the 2% recommendation based on?



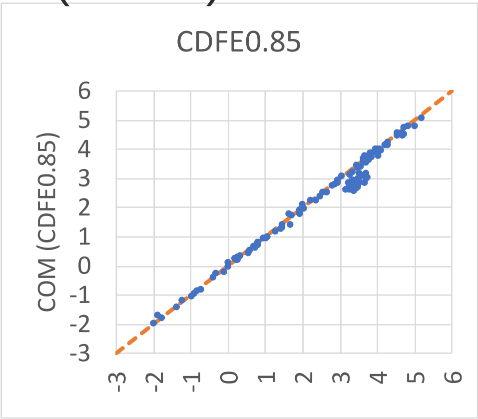
Source:
sun_3ck_adhoc_01a_120518
Slide 8

From ran_3ck_adhoc_01_021920

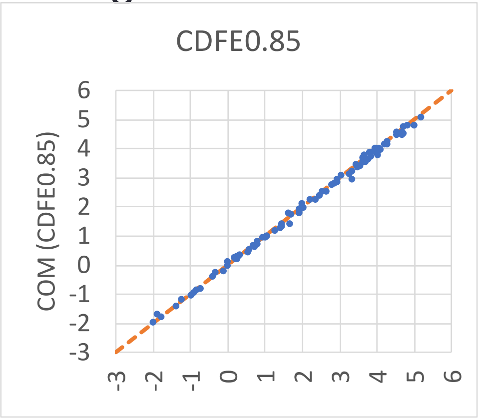
Digging into the data

Full data set provided in hidaka_3ck_adhoc_02_120518 to enable further analysis

Coarse DFE (0.25%) vs. medium DFE (0.2%)



Same, excluding the "AZ1" and "AZ2" Data



16	AZ1	Orthogonal Backplane Channel	zambell_100GEL_01a_0318.pdf
89-115	AZ2	Measured Orthogonal Backplane with Varied Impedances	zambell_3ck_01_1118.pdf

Source: sun_3ck_adhoc_01a_120518 slide 4

From ran_3ck_adhoc_01_021920

Eventually we chose a subset of channels for analysis

The Highlighted Channels

Contribution	Channel
heck_3ck_01_1118	28dB Cabled Backplane/Cable_BKP_28dB_0p575m_more_isi
	16dB Cabled Backplane/Cable_BKP_16dB_0p575m_more_isi
mellitz_3ck_adhoc_02_081518	24,28,30dB including BGA Via/CaBP_BGAVia_Opt2_28dB
tracy_3ck_01_0119	Traditional Backplane Channels/Std_BP_12inch_Meg7
	Orthogonal Backplane Channels/DPO_IL_12dB
kareti_3ck_01a_1118	Measured Orthogonal Backplane Channels/OAch4
	Measured Orthogonal Backplane Channels/Och4
	Measured Cabled Backplane Channels/CAch3_b2
	Measured Traditional Backplane Channels/Bch2_a7p5_7

“AZ” channels not in the list

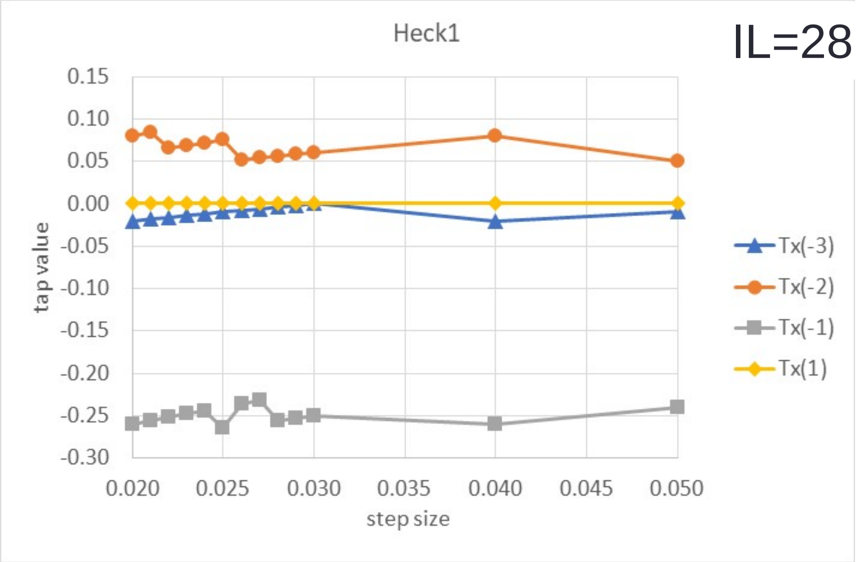
Source: kochuparambil_3ck_01c_0119 slide 5

From ran_3ck_adhoc_01_021920

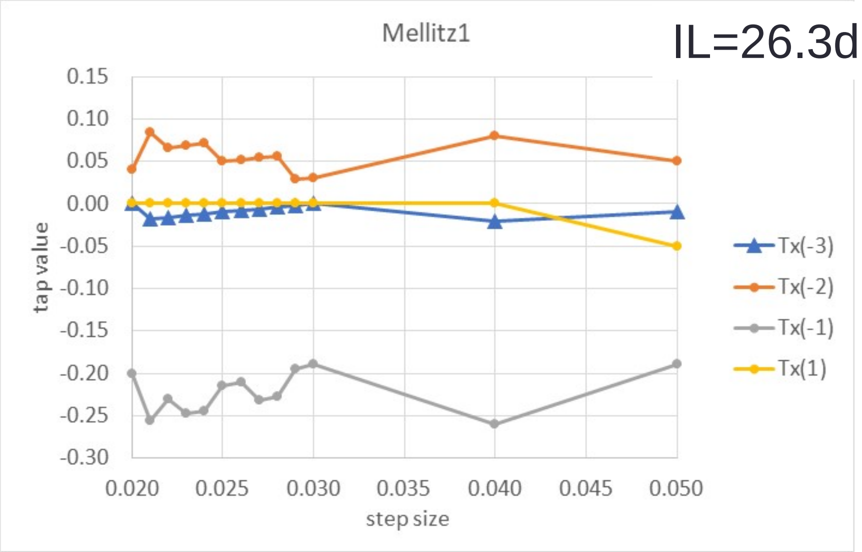
Tap Values By Channel

31/29mm Tx/Rx Package

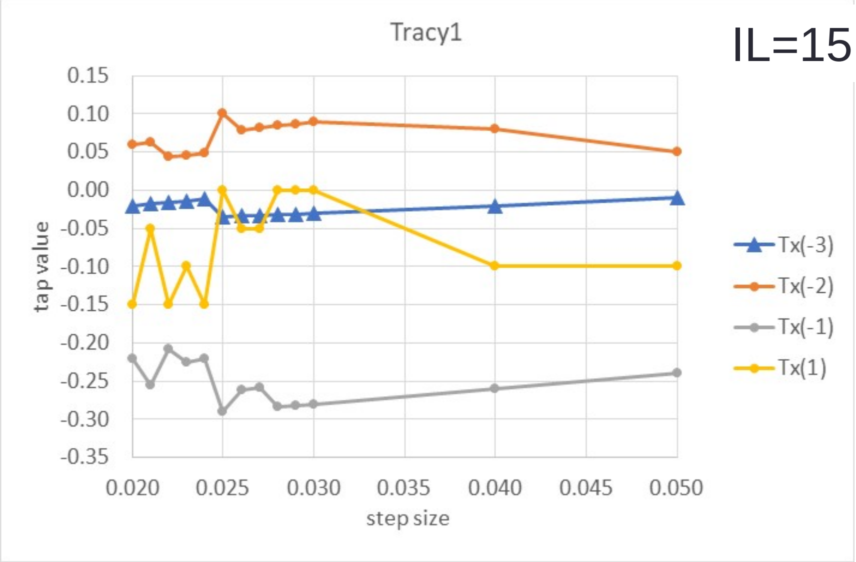
IL=28.8dB



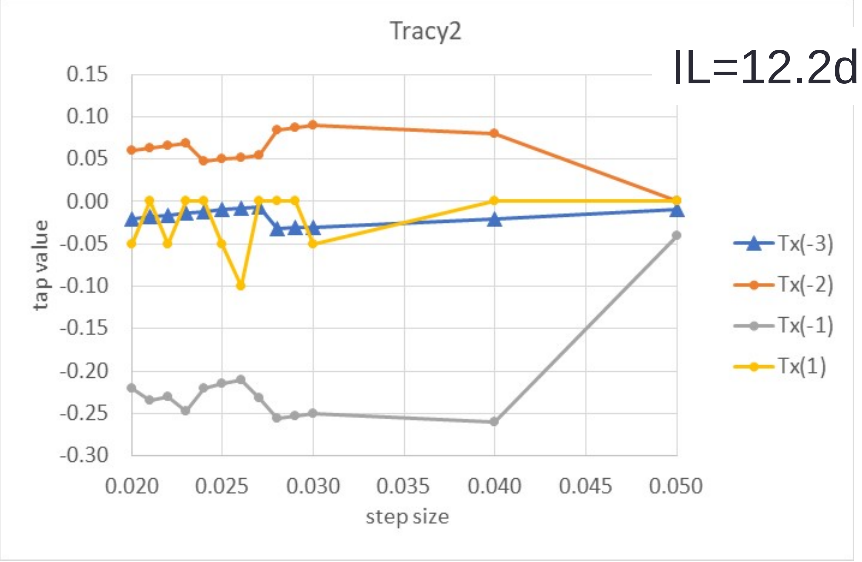
IL=26.3dB



IL=15.7dB



IL=12.2dB

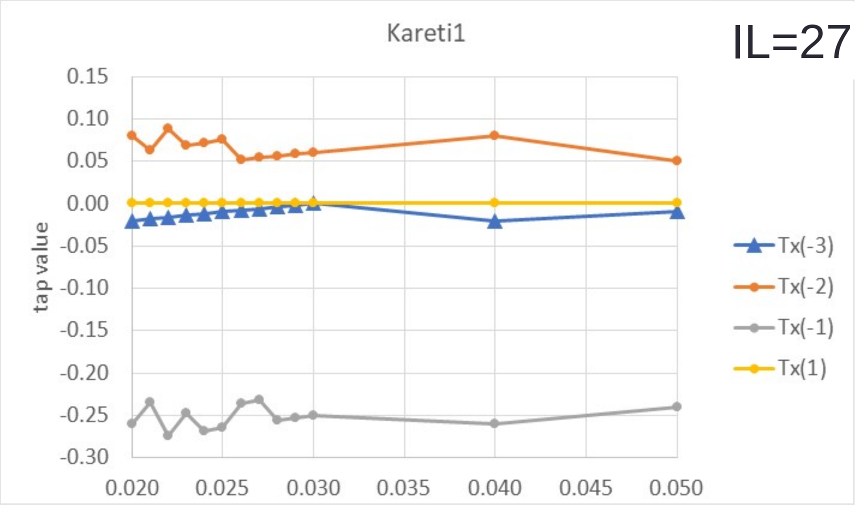


From ran_3ck_adhoc_01_021920

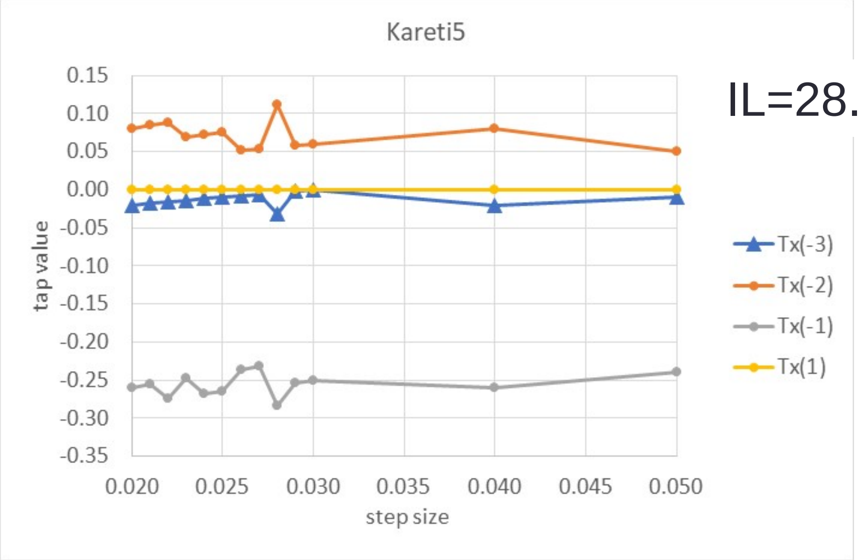
Tap Values By Channel

31/29mm Tx/Rx Package

IL=27.7dB



IL=28.9dB



IL=28.5dB