

Investigation into an Improved 100GbE FEC Sublayer

IEEE P802.3ck

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Mark Gustlin – Independent

Pete Anslow – Ciena

Gary Nicholl - Cisco

Shawn Nicholl – Xilinx

Dave Ofelt – Juniper

Kapil Shrikhande - Innovium

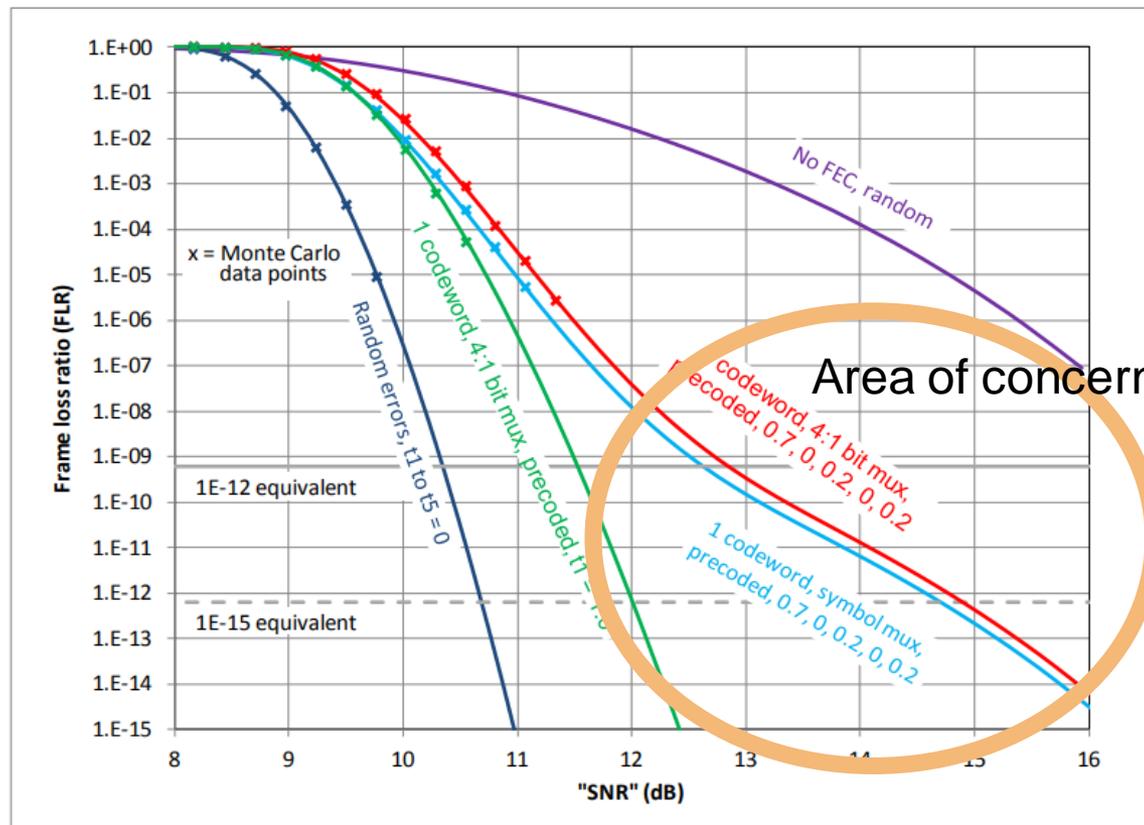
Introduction

- Pete Anslow showed in [anslow_3ck_01_0918.pdf](#) that there is some FEC performance concerns for 100GbE with multi-tap DFEs
- This presentation looks at a possible new FEC sublayer that can improve the performance for these cases

Burst Error Impact on 100G FEC Gain

- Pete Anslow showed in [anslow_3ck_01_0918.pdf](#) that there is concern with the 100G FEC performance with multi-tap DFE burst errors, even with precoding

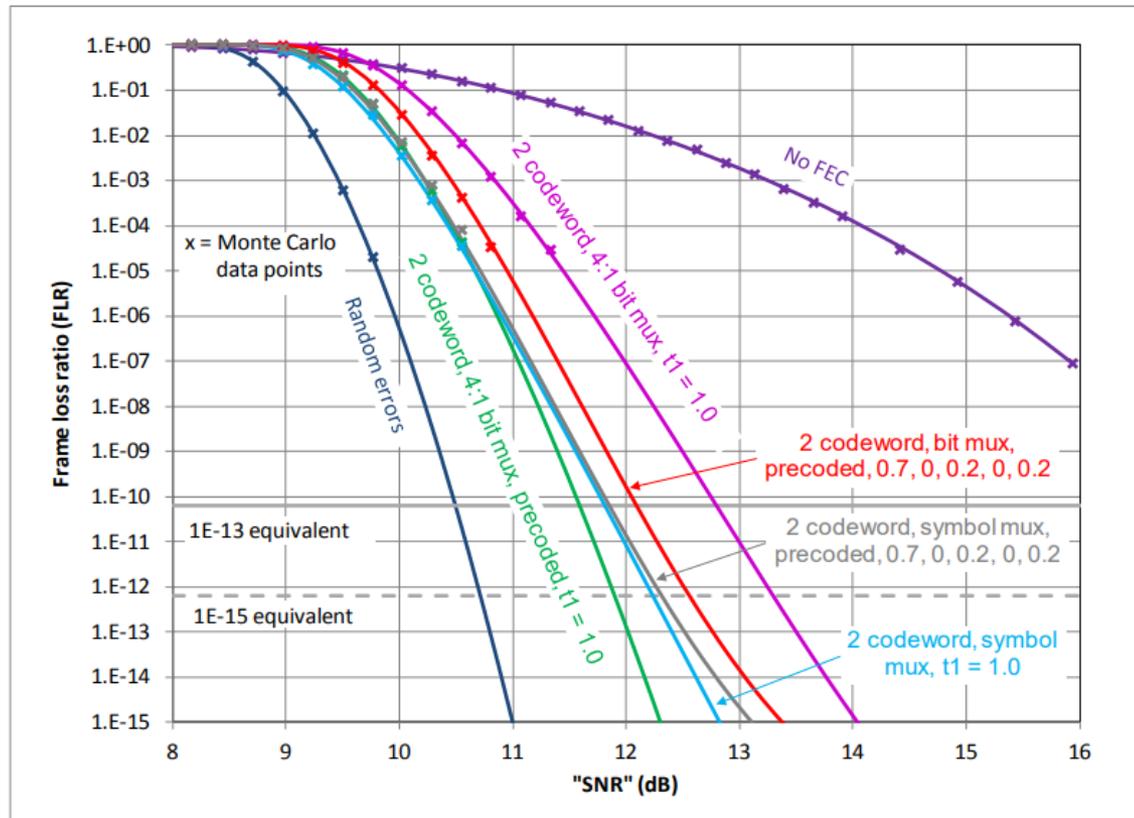
100G 5-tap DFE results (0.7, 0, 0.2, 0, 0.2) with precoding



Burst Error Impact on 400G FEC Gain

- Pete Anslow showed in [anslow_3ck_01_0918.pdf](#) that 400G does not have the same concern

400G 5-tap DFE results (0.7, 0, 0.2, 0, 0.2) with precoding



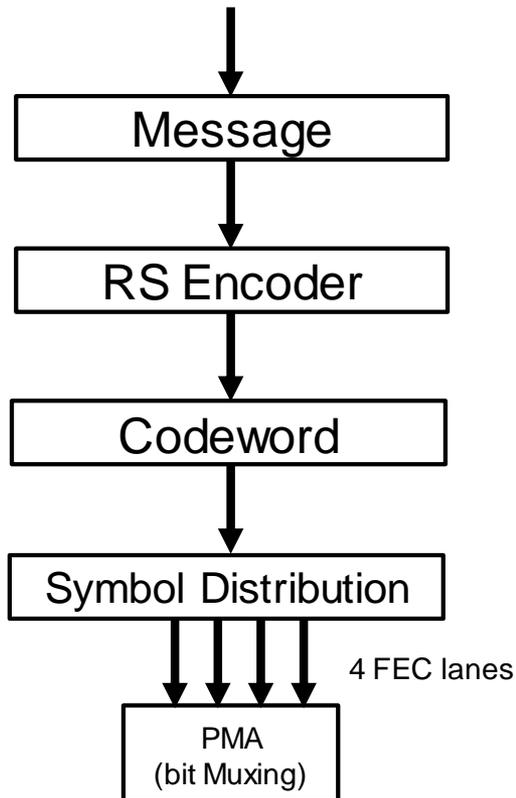
What to Do about it?

- Don't touch the 400/200G PCS/FEC
 - Symbol muxing is one tool we could use if needed to slightly improve the performance
- Look at modifications to the 100G FEC architecture, only for the longer more difficult channels
 - No changes for C2M, this preserves full link with 100GBASE-DR (and MSA optical links)
 - No changes to existing 100G per lane optical PMDs
 - Don't require PCS/FEC in optical modules
 - Look at changes for: 100GBASE-KR, 100GBASE-CR
 - C2C is a special case that needs more investigation
- Seems to be consensus that even if DFE is used for a C2M interface, the tap weights would be very low and not cause a problem with burst errors
 - Need to validate this assumption with sims, what tap weights should we assume??
- Explore this option in detail:
 - New FEC sublayer that does 2:1 FEC codeword interleaving

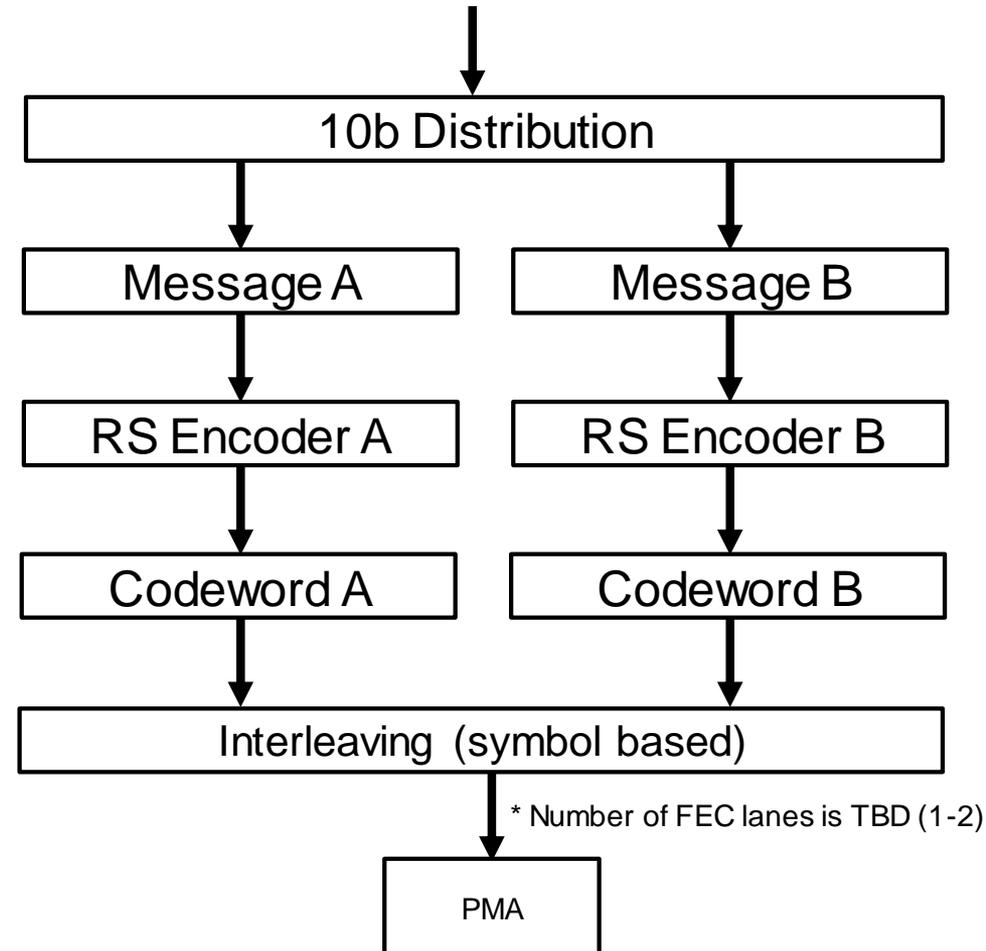
Possible New 100G FEC Sublayer

- Based on 2x50G RS(544,514) FEC interleaving

A portion of today's Clause 91 FEC



A portion of a possible new FEC sublayer



Assuming ABABAB ordering

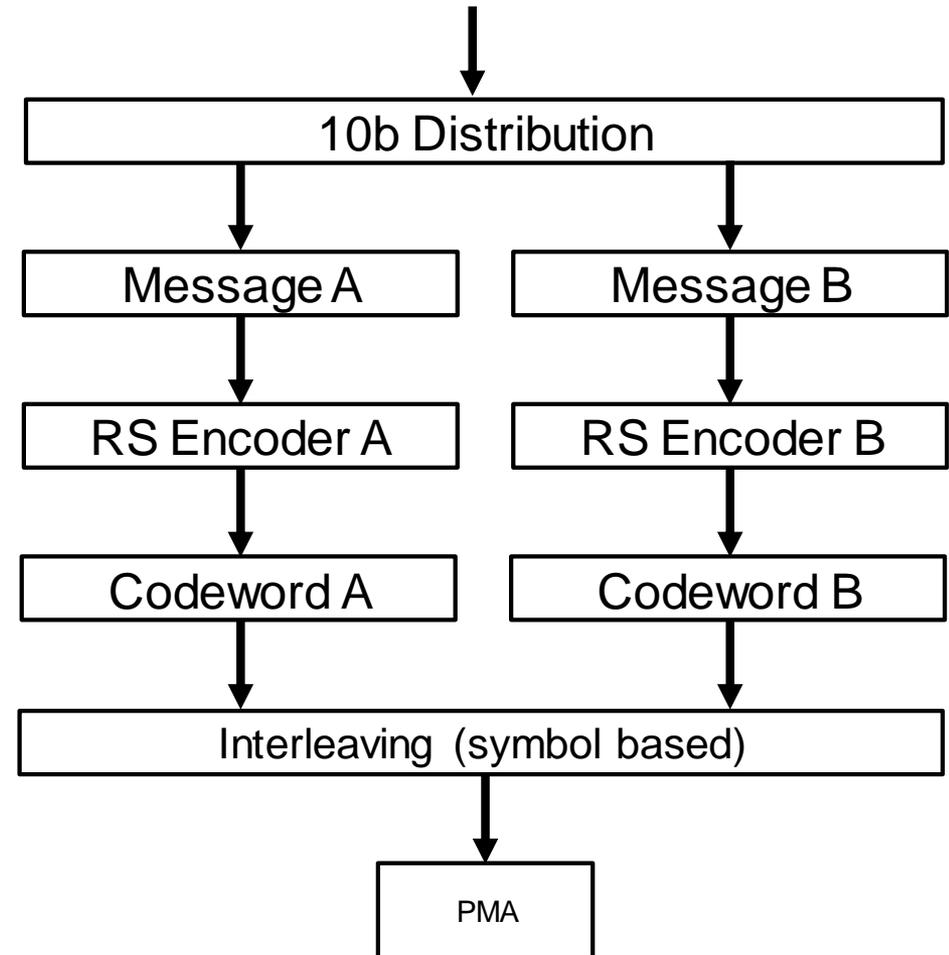
Latency for the 100G Interleaved FEC Sublayer

Current Clause 91 RS544

Latency	Contributor
51ns	Block time
50-100ns	Processing*
101-151ns	Total

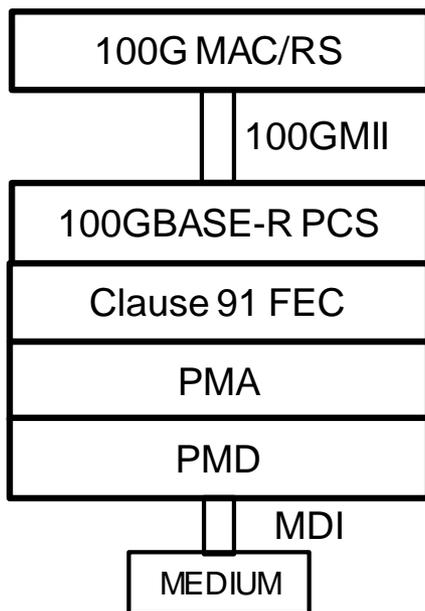
Potential RS544 Interleaved

Latency	Contributor
102ns	Block time
50-150ns	Processing*
152-252ns	Total

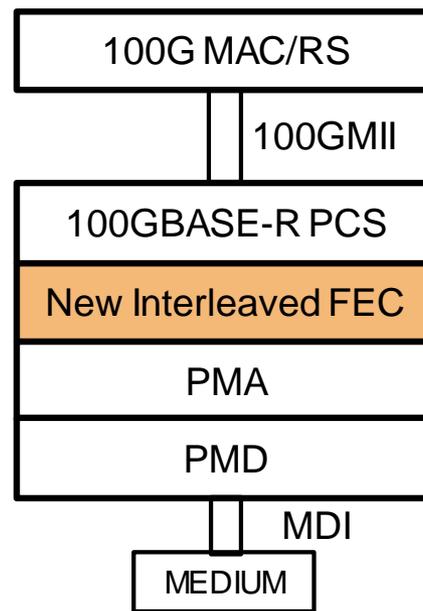


*depends on parallelism/latency tradeoffs

Architectural View

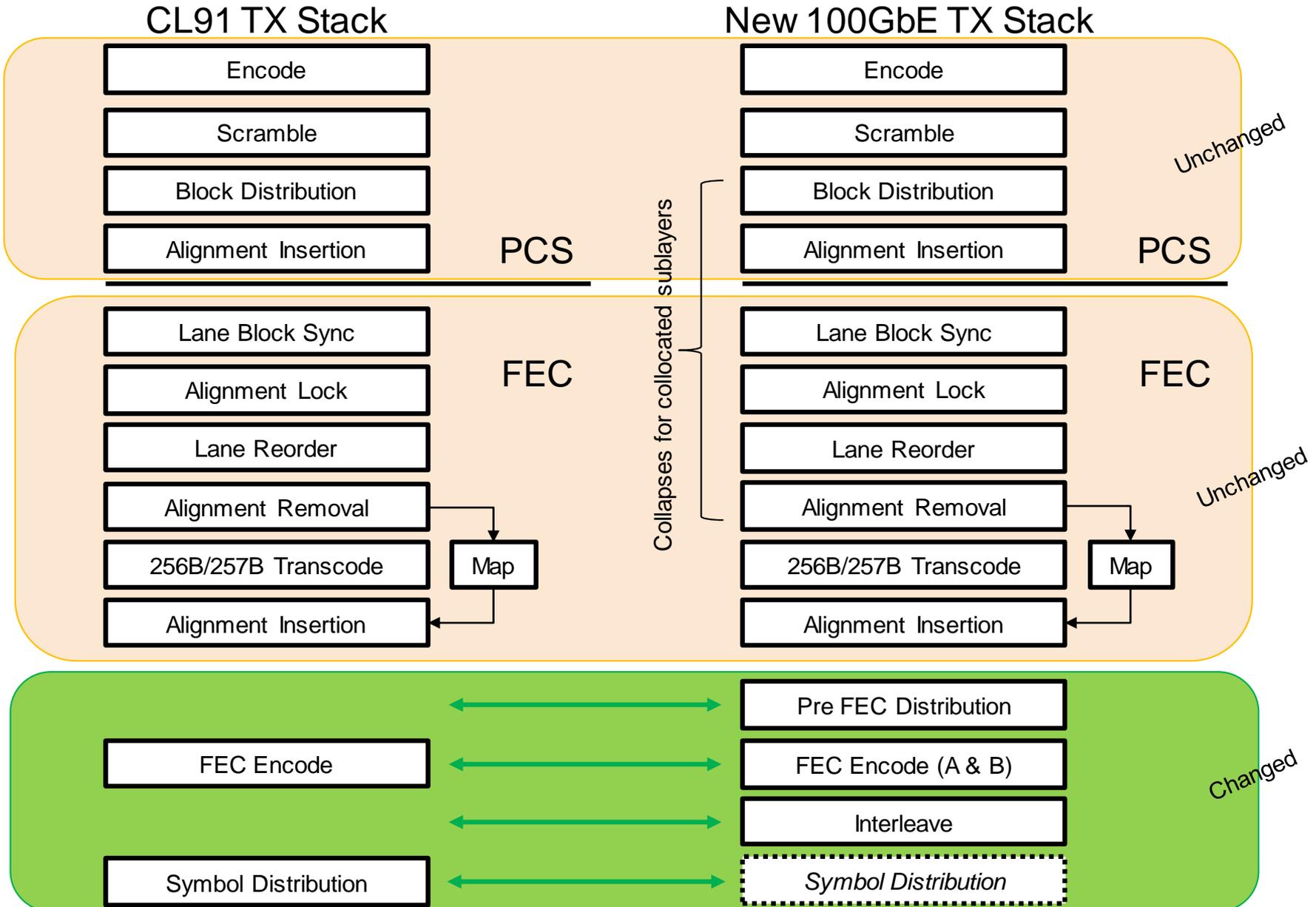


100GBASE-DR
100GAUI-1 C2M I/F

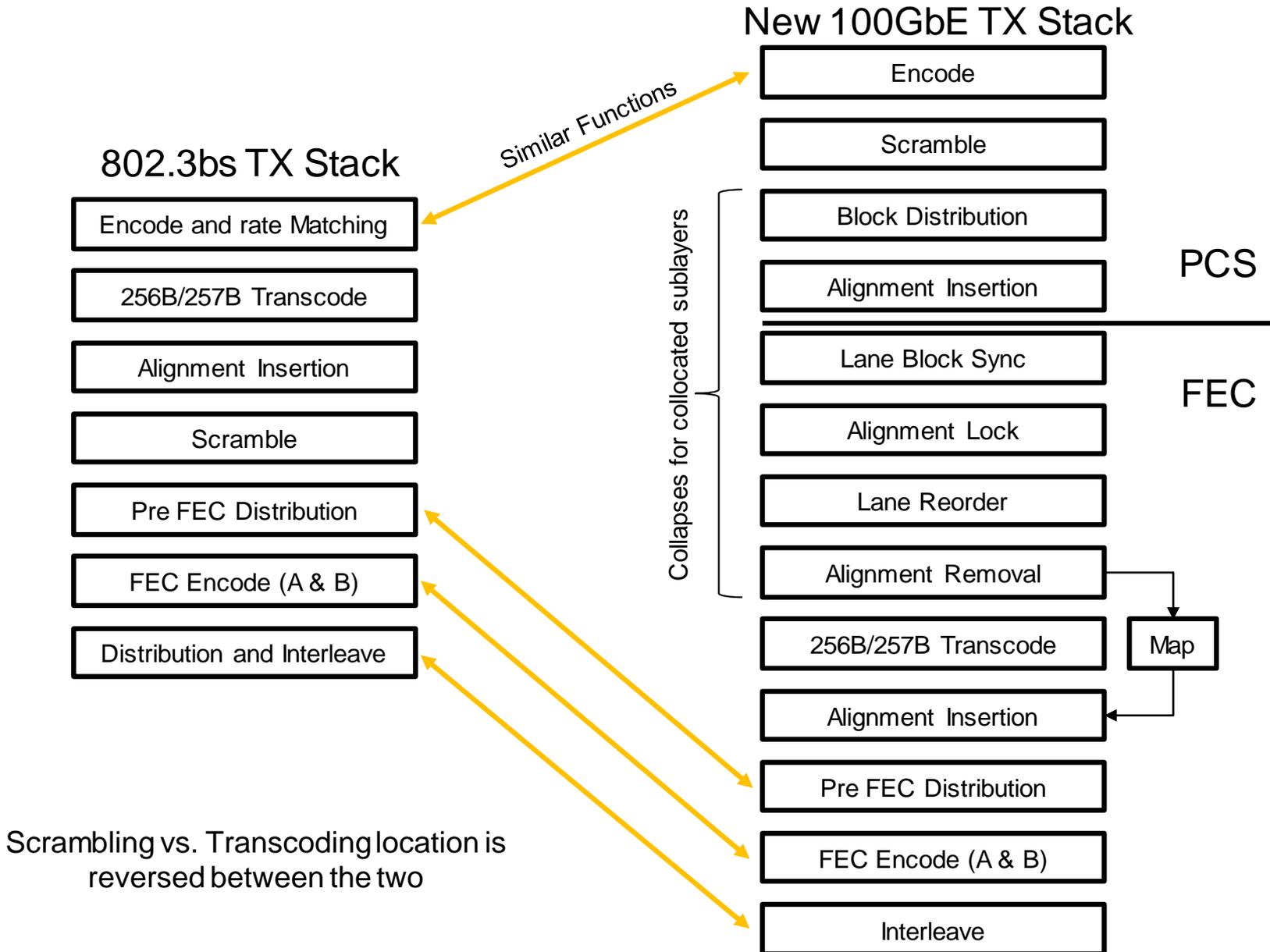


100GBASE-KR
100GBASE-CR
100GAUI-1 C2C I/F

Interleaved Protocol Stack Comparison with CL91

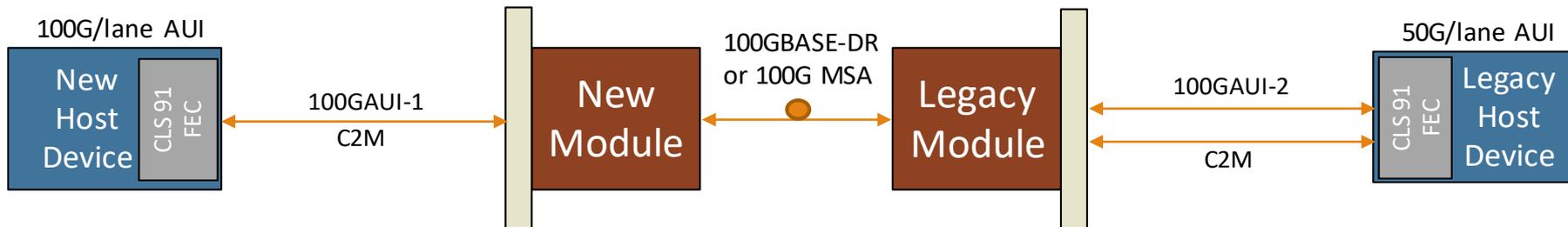


Interleaved Protocol Stack Comparison with 802.3bs

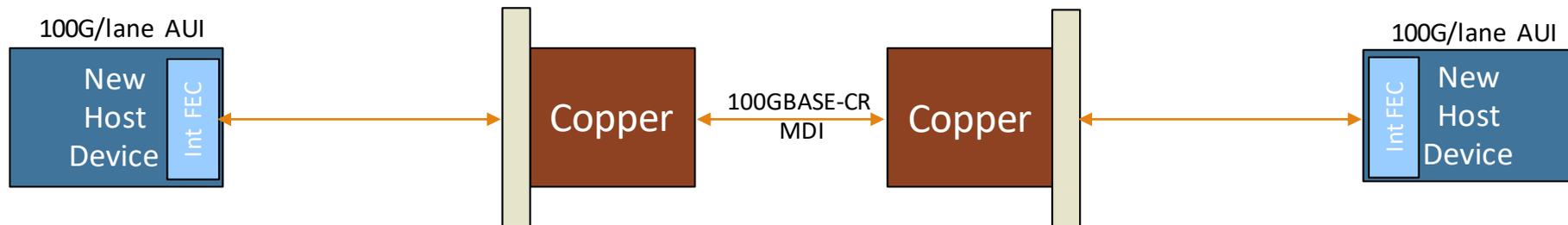


100GbE Example Use Cases

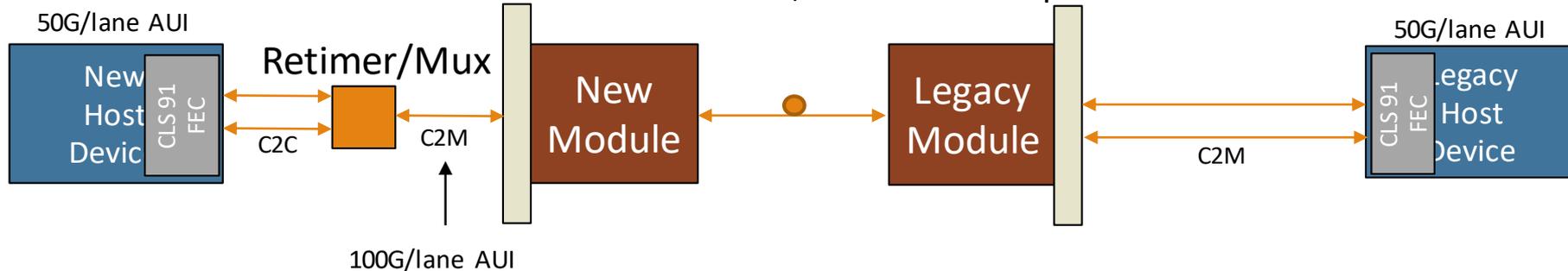
Seamless Clause 91 FEC end to end, backwards compatible



New Interleaved FEC end to end

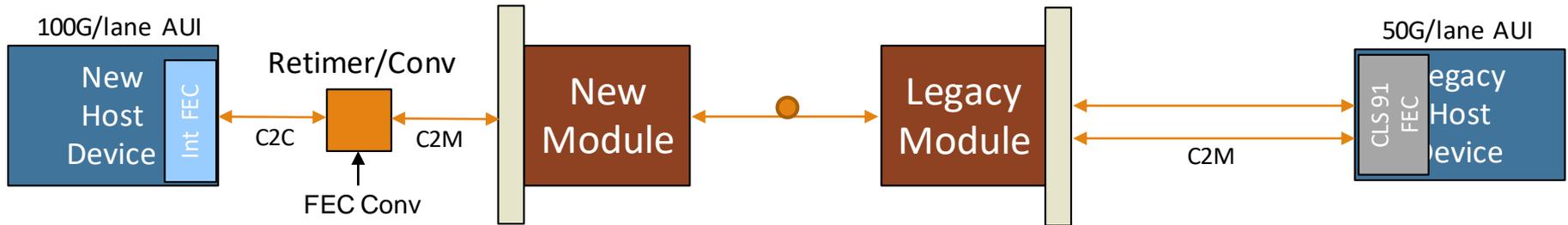


Retimer to 100G AUI-1, backwards compatible



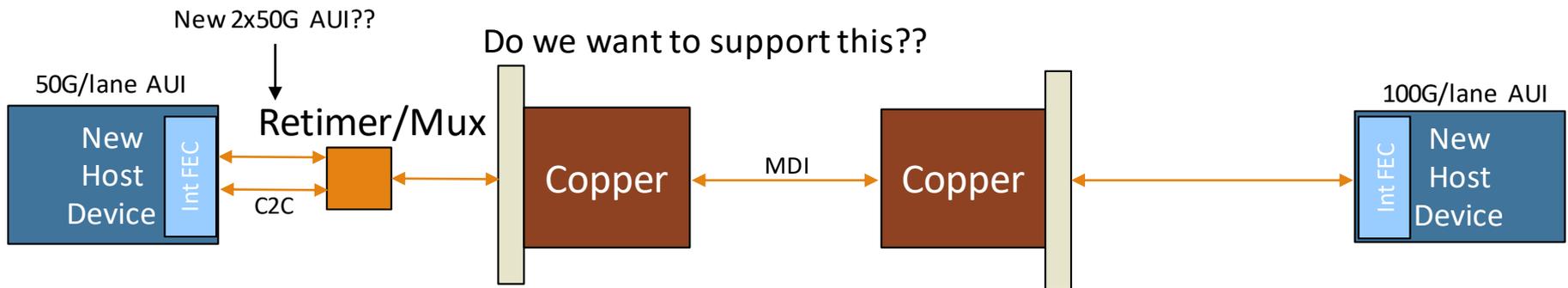
100GbE Example Use Cases – Needs More Work

Retimer converts from Interleaved FEC to Clause 91 FEC



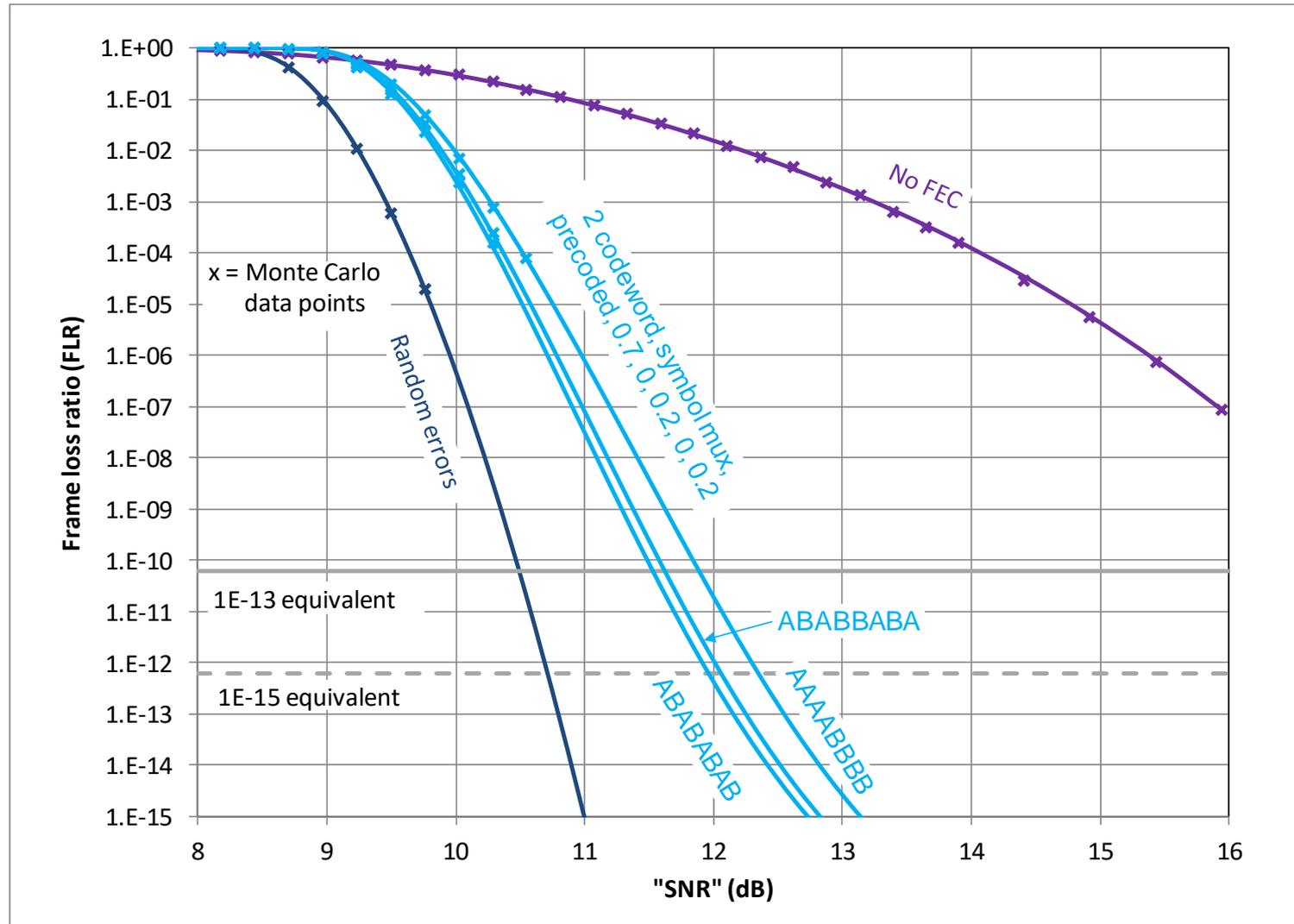
How to do this from a protocol stack point of view???

Do we want to support this??



How does this impact the architecture and performance?

100G Performance with Interleaved FEC



More Work to be Done

- Look in detail at how to handle C2C interfaces
- Investigate if we want to enable the new FEC sublayer over a 100GAUI-2 type of interface
- Agree to a model for DFE on a C2M, and run sims to see the performance
 - If DFE will be used for C2M
- Further flesh out the proposal with more details

Conclusion

- This presentation shows a possible interleaved FEC sublayer for the harder 100GbE single lane channels, as well as the performance improvement we expect to see
 - More work needs to be done to fully specify this sublayer

Thanks!