45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change Table 45–3 (as modified by IEEE Std 802.3cb-2018, IEEE Std 802.3cd-2018, and IEEE Std 802.3xx) as shown (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.34~~, 1.35~~	~~Reserved~~ BiDi PMA/PMD extended ability 1	45.2.1.27a
1.35	BiDi PMA/PMD extended ability 2	45.2.1.27b

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45–7 (as modified by IEEE Std 802.3cb-2018, IEEE Std 802.3cd-2018, and IEEE Std 802.3ct-YYYY) as shown (unchanged table rows and bit description lines not shown):

Editor's Note: code point 1100100 has been allocated to 400GBASE-ZR in P802.3ct.

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.6:0	PMA/PMD type selection	6 5 4 3 2 1 0 1 1 1 1 1 x x = reserved 1 1 1 1 0 1 x = reserved 1 1 1 1 0 0 1 = reserved 1 1 1 1 0 0 0 = 50GBASE-BER-U PMA/PMD 1 1 1 0 1 1 1 = 50GBASE-BMR-U PMA/PMD 1 1 1 0 1 1 0 = 50GBASE-BLR-U PMA/PMD 1 1 1 0 1 0 1 = 50GBASE-BER-D PMA/PMD 1 1 1 0 1 0 0 = 50GBASE-BMR-D PMA/PMD 1 1 1 0 0 1 1 = 50GBASE-BLR-D PMA/PMD 1 1 1 0 0 1 0 = 25GBASE-BER-U PMA/PMD 1 1 1 0 0 0 1 = 25GBASE-BMR-U PMA/PMD 1 1 1 0 0 0 0 = 25GBASE-BLR-U PMA/PMD 1 1 0 1 1 1 1 = 25GBASE-BER-D PMA/PMD 1 1 0 1 1 1 0 = 25GBASE-BMR-D PMA/PMD 1 1 0 1 1 0 1 = 25GBASE-BLR-D PMA/PMD 1 1 0 1 1 0 0 = 10GBASE-BER-U PMA/PMD 1 1 0 1 0 1 1 = 10GBASE-BMR-U PMA/PMD 1 1 0 1 0 1 0 = 10GBASE-BLR-U PMA/PMD 1 1 0 1 0 0 1 = 10GBASE-BER-D PMA/PMD 1 1 0 1 0 0 0 = 10GBASE-BMR-D PMA/PMD 1 1 0 0 1 1 1 = 10GBASE-BLR-D PMA/PMD 1 1 0 0 1 1 0 = reserved 1 1 0 0 1 0 1 = reserved 1 1 0 0 1 0 0 = reserved 1 1 0 0 0 x x = reserved ~~1 1 x x x x x = reserved~~ ...	R/W

[a]R/W = Read/Write, RO = Read only

Editor's Note: In Tables 45-9, 45-10, and 45-12 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 were added by 802.3cd, hence they are shown in these tables for clarity.

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.1 Transmit fault (1.8.11)

Change Table 45–9 (as modified by IEEE Std 802.3cb-2018 and IEEE Std 802.3cd-2018) as shown (additional unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
...	
5GBASE-KR	130.6.8
10GBASE-BLR, 10GBASE-BMR, and 10GBASE-BER	158.5.6
...	
10GBASE-KX4	71.6.10
25GBASE-BLR, 25GBASE-BMR, and 25GBASE-BER	159.5.6
...	
40GBASE-T	113.4.2.2
50GBASE-BLR, 50GBASE-BMR, and 50GBASE-BER	160.5.6
50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	137.8.9
...	

45.2.1.7.2 Receive fault (1.8.10)

Change Table 45–10 (as modified by IEEE Std 802.3cb-2018 and IEEE Std 802.3cd-2018) as shown (additional unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
...	
5GBASE-KR	130.6.9
10GBASE-BLR, 10GBASE-BMR, and 10GBASE-BER	158.5.9
...	
10GBASE-KX4	71.6.11
25GBASE-BLR, 25GBASE-BMR, and 25GBASE-BER	159.5.9
...	
40GBASE-T	89.5.9
50GBASE-BLR, 50GBASE-BMR, and 50GBASE-BER	160.5.9
50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	137.8.10
...	

45.2.1.8 PMD transmit disable register (Register 1.9)

45.2.1.8.1 PMD transmit disable 14 (1.9.15)

Change Table 45–12 (as modified by IEEE Std 802.3cb-2018 and IEEE Std 802.3cd-2018) as shown (additional unchanged rows not shown):

Table 45–12—Transmit disable description location

PMA/PMD	Description location
...	
5GBASE-KR	130.6.5
10GBASE-BLR, 10GBASE-BMR, and 10GBASE-BER	158.5.6
...	
10GBASE-KX4	71.6.6
25GBASE-BLR, 25GBASE-BMR, and 25GBASE-BER	159.5.6
...	
40GBASE-T	113.4.2.3
50GBASE-BLR, 50GBASE-BMR, and 50GBASE-BER	160.5.6
50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	137.8.10
...	

Insert 45.2.1.27a, 45.2.1.27b and associated subclauses after 45.2.1.27:

45.2.1.27a BiDi PMA/PMD extended ability 1 (Register 1.34)

The assignment of bits in the BiDi PMA/PMD extended ability 1 is shown in Table 45–31a.

Table 45–31a—25G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.34.14:15	Reserved	Value always 0	RO
1.34.13	25GBASE-BER-U ability	1 = PMA/PMD is able to perform 25GBASE-BER-U 0 = PMA/PMD is not able to perform 25GBASE-BER-U	RO
1.34.12	25GBASE-BER-D ability	1 = PMA/PMD is able to perform 25GBASE-BER-D 0 = PMA/PMD is not able to perform 25GBASE-BER-D	RO
1.34.11	25GBASE-BMR-U ability	1 = PMA/PMD is able to perform 25GBASE-BMR-U 0 = PMA/PMD is not able to perform 25GBASE-BMR-U	RO
1.34.10	25GBASE-BMR-D ability	1 = PMA/PMD is able to perform 25GBASE-BMR-D 0 = PMA/PMD is not able to perform 25GBASE-BMR-D	RO
1.34.9	25GBASE-BLR-U ability	1 = PMA/PMD is able to perform 25GBASE-BLR-U 0 = PMA/PMD is not able to perform 25GBASE-BLR-U	RO
1.34.8	25GBASE-BLR-D ability	1 = PMA/PMD is able to perform 25GBASE-BLR-D 0 = PMA/PMD is not able to perform 25GBASE-BLR-D	RO
1.34.7:6	Reserved	Value always 0	RO
1.34.5	10GBASE-BER-U ability	1 = PMA/PMD is able to perform 10GBASE-BER-U 0 = PMA/PMD is not able to perform 10GBASE-BER-U	RO
1.34.4	10GBASE-BER-D ability	1 = PMA/PMD is able to perform 10GBASE-BER-D 0 = PMA/PMD is not able to perform 10GBASE-BER-D	RO
1.34.3	10GBASE-BMR-U ability	1 = PMA/PMD is able to perform 10GBASE-BMR-U 0 = PMA/PMD is not able to perform 10GBASE-BMR-U	RO
1.34.2	10GBASE-BMR-D ability	1 = PMA/PMD is able to perform 10GBASE-BMR-D 0 = PMA/PMD is not able to perform 10GBASE-BMR-D	RO
1.34.1	10GBASE-BLR-U ability	1 = PMA/PMD is able to perform 10GBASE-BLR-U 0 = PMA/PMD is not able to perform 10GBASE-BLR-U	RO
1.34.0	10GBASE-BLR-D ability	1 = PMA/PMD is able to perform 10GBASE-BLR-D 0 = PMA/PMD is not able to perform 10GBASE-BLR-D	RO

[a]RO = Read only

45.2.1.27a.1 25GBASE-BER-U ability (1.34.13)

When read as a one, bit 1.34.13 indicates that the PMA/PMD is able to operate as a 25GBASE-BER-U PMA/PMD type. When read as a zero, bit 1.34.13 indicates that the PMA/PMD is not able to operate as a 25GBASE-BER-U PMA/PMD type.

45.2.1.27a.2 25GBASE-BER-D ability (1.34.12)

When read as a one, bit 1.34.12 indicates that the PMA/PMD is able to operate as a 25GBASE-BER-D PMA/PMD type. When read as a zero, bit 1.34.12 indicates that the PMA/PMD is not able to operate as a 25GBASE-BER-D PMA/PMD type.

45.2.1.27a.3 25GBASE-BMR-U ability (1.34.11)

When read as a one, bit 1.34.11 indicates that the PMA/PMD is able to operate as a 25GBASE-BMR-U PMA/PMD type. When read as a zero, bit 1.34.11 indicates that the PMA/PMD is not able to operate as a 25GBASE-BMR-U PMA/PMD type.

45.2.1.27a.4 25GBASE-BMR-D ability (1.34.10)

When read as a one, bit 1.34.10 indicates that the PMA/PMD is able to operate as a 25GBASE-BMR-D PMA/PMD type. When read as a zero, bit 1.34.10 indicates that the PMA/PMD is not able to operate as a 25GBASE-BMR-D PMA/PMD type.

45.2.1.27a.5 25GBASE-BLR-U ability (1.34.9)

When read as a one, bit 1.34.9 indicates that the PMA/PMD is able to operate as a 25GBASE-BLR-U PMA/PMD type. When read as a zero, bit 1.34.9 indicates that the PMA/PMD is not able to operate as a 25GBASE-BLR-U PMA/PMD type.

45.2.1.27a.6 25GBASE-BLR-D ability (1.34.8)

When read as a one, bit 1.34.8 indicates that the PMA/PMD is able to operate as a 25GBASE-BLR-D PMA/PMD type. When read as a zero, bit 1.34.8 indicates that the PMA/PMD is not able to operate as a 25GBASE-BLR-D PMA/PMD type.

45.2.1.27a.7 10GBASE-BER-U ability (1.34.5)

When read as a one, bit 1.34.5 indicates that the PMA/PMD is able to operate as a 10GBASE-BER-U PMA/PMD type. When read as a zero, bit 1.34.5 indicates that the PMA/PMD is not able to operate as a 10GBASE-BER-U PMA/PMD type.

45.2.1.27a.8 10GBASE-BER-D ability (1.34.4)

When read as a one, bit 1.34.4 indicates that the PMA/PMD is able to operate as a 10GBASE-BER-D PMA/PMD type. When read as a zero, bit 1.34.4 indicates that the PMA/PMD is not able to operate as a 10GBASE-BER-D PMA/PMD type.

45.2.1.27a.9 10GBASE-BMR-U ability (1.34.3)

When read as a one, bit 1.34.3 indicates that the PMA/PMD is able to operate as a 10GBASE-BMR-U PMA/PMD type. When read as a zero, bit 1.34.3 indicates that the PMA/PMD is not able to operate as a 10GBASE-BMR-U PMA/PMD type.

45.2.1.27a.10 10GBASE-BMR-D ability (1.34.2)

When read as a one, bit 1.34.2 indicates that the PMA/PMD is able to operate as a 10GBASE-BMR-D PMA/PMD type. When read as a zero, bit 1.34.2 indicates that the PMA/PMD is not able to operate as a 10GBASE-BMR-D PMA/PMD type.

45.2.1.27a.11 10GBASE-BLR-U ability (1.34.1)

When read as a one, bit 1.34.1 indicates that the PMA/PMD is able to operate as a 10GBASE-BLR-U PMA/PMD type. When read as a zero, bit 1.34.1 indicates that the PMA/PMD is not able to operate as a 10GBASE-BLR-U PMA/PMD type.

45.2.1.27a.12 10GBASE-BLR-D ability (1.34.0)

When read as a one, bit 1.34.0 indicates that the PMA/PMD is able to operate as a 10GBASE-BLR-D PMA/PMD type. When read as a zero, bit 1.34.0 indicates that the PMA/PMD is not able to operate as a 10GBASE-BLR-D PMA/PMD type.

45.2.1.27b BiDi PMA/PMD extended ability 2 (Register 1.35)

The assignment of bits in the BiDi PMA/PMD extended ability 2 is shown in Table 45–31b.

Table 45–31b—25G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.35.15:6	Reserved	Value always 0	RO
1.35.5	50GBASE-BER-U ability	1 = PMA/PMD is able to perform 50GBASE-BER-U 0 = PMA/PMD is not able to perform 50GBASE-BER-U	RO
1.35.4	50GBASE-BER-D ability	1 = PMA/PMD is able to perform 50GBASE-BER-D 0 = PMA/PMD is not able to perform 50GBASE-BER-D	RO
1.35.3	50GBASE-BMR-U ability	1 = PMA/PMD is able to perform 50GBASE-BMR-U 0 = PMA/PMD is not able to perform 50GBASE-BMR-U	RO
1.35.2	50GBASE-BMR-D ability	1 = PMA/PMD is able to perform 50GBASE-BMR-D 0 = PMA/PMD is not able to perform 50GBASE-BMR-D	RO
1.35.1	50GBASE-BLR-U ability	1 = PMA/PMD is able to perform 50GBASE-BLR-U 0 = PMA/PMD is not able to perform 50GBASE-BLR-U	RO
1.35.0	50GBASE-BLR-D ability	1 = PMA/PMD is able to perform 50GBASE-BLR-D 0 = PMA/PMD is not able to perform 50GBASE-BLR-D	RO

[a]RO = Read only

45.2.1.27b.1 50GBASE-BER-U ability (1.35.5)

When read as a one, bit 1.35.5 indicates that the PMA/PMD is able to operate as a 50GBASE-BER-U PMA/PMD type. When read as a zero, bit 1.35.5 indicates that the PMA/PMD is not able to operate as a 50GBASE-BER-U PMA/PMD type.

45.2.1.27b.2 50GBASE-BER-D ability (1.35.4)

When read as a one, bit 1.35.4 indicates that the PMA/PMD is able to operate as a 50GBASE-BER-D PMA/PMD type. When read as a zero, bit 1.35.4 indicates that the PMA/PMD is not able to operate as a 50GBASE-BER-D PMA/PMD type.

45.2.1.27b.3 50GBASE-BMR-U ability (1.35.3)

When read as a one, bit 1.35.3 indicates that the PMA/PMD is able to operate as a 50GBASE-BMR-U PMA/PMD type. When read as a zero, bit 1.35.3 indicates that the PMA/PMD is not able to operate as a 50GBASE-BMR-U PMA/PMD type.

45.2.1.27b.4 50GBASE-BMR-D ability (1.35.2)

When read as a one, bit 1.35.2 indicates that the PMA/PMD is able to operate as a 50GBASE-BMR-D PMA/PMD type. When read as a zero, bit 1.35.2 indicates that the PMA/PMD is not able to operate as a 50GBASE-BMR-D PMA/PMD type.

45.2.1.27b.5 50GBASE-BLR-U ability (1.35.1)

When read as a one, bit 1.35.1 indicates that the PMA/PMD is able to operate as a 50GBASE-BLR-U PMA/PMD type. When read as a zero, bit 1.35.1 indicates that the PMA/PMD is not able to operate as a 50GBASE-BLR-U PMA/PMD type.

45.2.1.27b.6 50GBASE-BLR-D ability (1.35.0)

When read as a one, bit 1.35.0 indicates that the PMA/PMD is able to operate as a 50GBASE-BLR-D PMA/PMD type. When read as a zero, bit 1.35.0 indicates that the PMA/PMD is not able to operate as a 50GBASE-BLR-D PMA/PMD type.