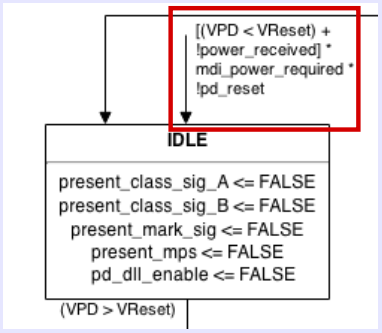
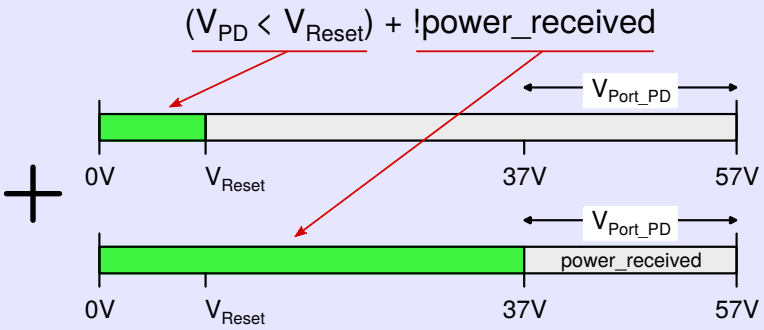
Updated PD state diagram v100

Info (not part of baseline)





33.3.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

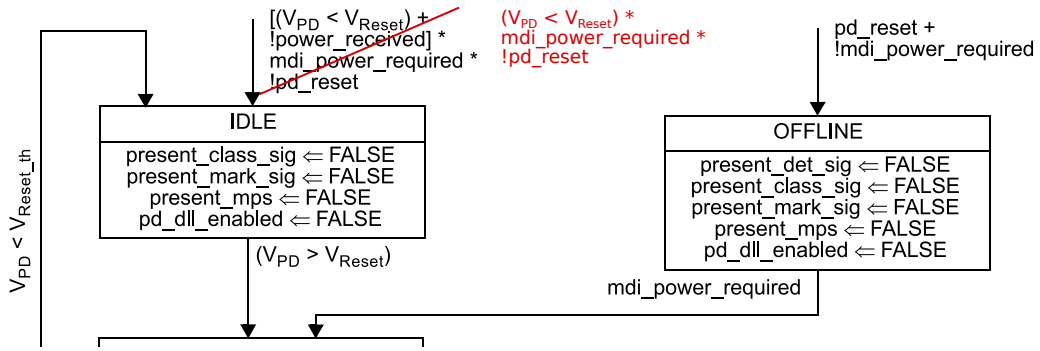
21.5.3 State transitions

Any open arrow (an arrow with no source block) represents a global transition. Global transitions are evaluated continuously whenever any state is evaluating its exit conditions. When a global transition becomes true, it supersedes all other transitions, including UCT, returning control to the block pointed to by the open arrow.

In other words: unless a PD is powered, the SM will continuously flip back to the IDLE state. This entry arrow into IDLE has existed since 802.3at

33.3.3.5 State diagrams

Change Figure 33–16 as follows:



33.3.7.1 Input voltage

Add new paragraph at the end of 33.3.7.1 as follows:

Interoperability between PSE and PD is no longer guaranteed when the PD is in the MDI_POWER1, MDI_POWER_DLY, or MDI_POWER2 state and V_{PD} falls below V_{Off}, until the PD is reset by bringing V_{PD} below V_{Reset}.