

# Error Marking for 100GBASE-ZR

## P802.3ct Task Force

### July 2019

Steve Trowbridge (Nokia)

Pete Anslow (Ciena)

Ilya Lyubomirsky (Inphi)

# May Meeting Contribution showed issue with MTTFPA without error marking in 100GBASE-ZR

- [P802.3ct mean time to false packet acceptance \(MTTFPA\)](#) (Pete Anslow) Slides 3-9
- Objective of the proposal in this presentation: improve the MTTFPA for 100GBASE-ZR without introducing an inconsistency with the ITU-T G.709.2 frame. Ideally this is achieved by adding error marking for known uncorrectable or potentially mis-corrected or not completely corrected Staircase FEC codewords

# Probability of Undetected Uncorrectable Error

- Not tractable using analytical formula, need simulation analysis
- We ran Monte-Carlo simulation on a realistic implementation of Staircase FEC decoder
- Uncorrectable FEC block errors are detected using 512 syndrome calculations on the output 512x512 block
- Results below show all uncorrectable error blocks where detected in simulation

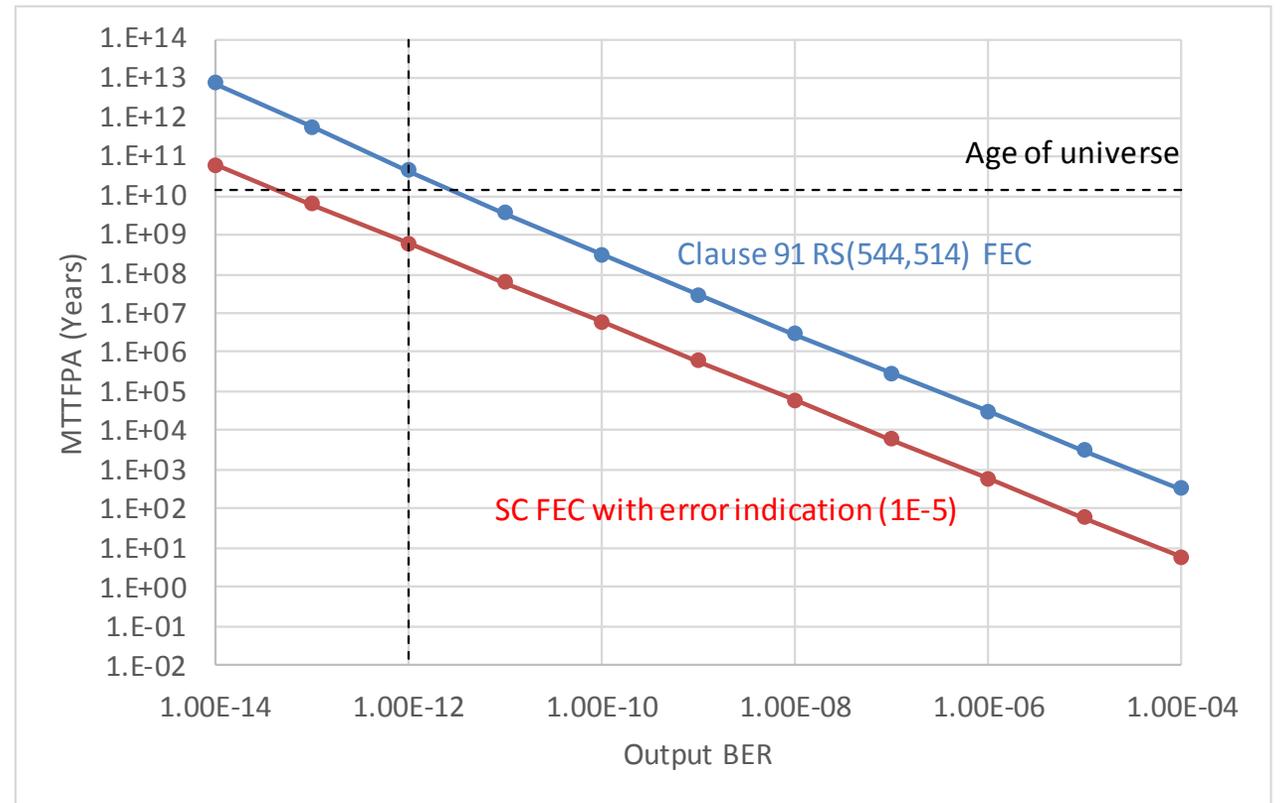
BER_in	Number of Block Errors	BER_out	Undetected Block errors
4.85E-03	2.23E+06	1.92457E-05	0
4.80E-03	2.32E+05	1.86449E-07	0
4.75E-03	3.81E+04	6.99364E-09	0
4.70E-03	5.49E+03	6.17064E-10	0
4.65E-03	8.94E+02	9.14396E-11	0

- **Probability(undetected block error | block error occurred) < 1.e-5**  
(assume  $P=1.e-5 \Rightarrow$  probability all block errors detected in sims  $\sim 1e-11$  is very unlikely)

# Effect of $1E-5$ detection failure probability on MTTFPA

If the probability that an output block containing errors is not detected is  $1E-5$  and blocks known to contain errors are marked as bad, the curve of MTTFPA as a function of output BER is shown by the red curve on the right.

Since the value of  $1E-5$  is a bound derived from simulations that did not have any undetected block errors, it would be helpful if the simulation could be extended to see if a bound of  $1E-6$  could be established, which would move the red curve much closer to the blue one.



# Reed Solomon (528,514) or (544,514) FEC Error Marking – Clause 91.5.3.3

The Reed-Solomon decoder indicates errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors (when the bypass correction feature is enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled), it shall ensure that, for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, `rx_coded_0<1:0>`, is set to 11. In addition, it shall ensure `rx_coded_0<1:0>` corresponding to the 6th 257-bit block and `rx_coded_3<1:0>` corresponding to the last (20th) 257-bit block in the codeword are set to 11. This causes the PCS to discard all frames 64 bytes and larger that are fully or partially within the codeword.

# Features of RS FEC error marking

- Each RS FEC codeword contains twenty 257B blocks or eighty 66B-block equivalent, aligned to the FEC codeword
- If AMs are present in the codeword, they are at the beginning (the first five 257B blocks)
- The first, last, and every 8<sup>th</sup> 66B block is error marked by corrupting the sync header
- The 20<sup>th</sup> 66B block is also error marked, as this would be the first 66B block of packet data in a FEC codeword that contains AMs

# Environment for Staircase FEC error marking

- A Staircase FEC codeword consists of two SC-FEC frames (OTU4 frame equivalent)
- 66B encoded data (serialized and deskewed PCS lanes including AMs) is GMP mapped into the SC-FEC frames
- Each SC-FEC frame carries 188 or 189 GMP words of 80 octets each. There is no assured alignment of 66B blocks to this mapping sequence and no guaranteed position of where the AMs are in this sequence. Two consecutive frames of 188 GMP words may occur, but two consecutive frames of 189 GMP words may not given the clock ratios. So in the Staircase FEC codeword, there are either:
  - 376×80 octets of 66B encoded data, which consists of 3646 full 66B blocks plus 4 extra bits either before, after, or divided before and after the full 66B blocks; or
  - 377×80 octets of 66B encoded data, which consists of 3655 full 66B blocks, plus 50 extra bits either before, after, or divided before and after the full 66B blocks

# Challenges for Error Marking of 66B blocks within uncorrectable Staircase FEC codewords

- Need to error mark a partial 66B block that began in the previous FEC codeword and ends in this one (could be the last 66B block of a packet)
- Need to error mark a partial 66B block that begins in this FEC codeword and ends in the next one (could be the first 66B block of a packet)
- At least one of every eight 66B blocks representing packet data needs to be error marked if sync header corruption is used..
- The alignment of 20-blocks of AM that may appear in the 66B stream is unknown
- You don't want to error mark so many blocks with sync header violations that you trigger the hi\_ber state and bring the link down

# Corrupting every 8<sup>th</sup> 66B block isn't a viable strategy for 100GBASE-ZR and Staircase FEC

- Presence of AMs with unknown alignment can turn 8 block spacing into 12 block spacing, hence not necessarily corrupting a 64-octet frame

66B	AM0	AM1	AM2	AM3	AM4	AM5	AM6	AM7	AM8	AM9	AM10	AM11	AM12	AM13	AM14	AM15	AM16	AM17	AM18	AM19	66B	66B	66B	66B	66B	66B							
X								X								X									X								X

- Corrupting the sync header of every 8<sup>th</sup> block in a Staircase FEC codeword is far more than 97 blocks in a single codeword (<500μs) and will trigger the hi\_ber state

Proposal: Rather than error marking by corrupting sync headers, replace every 66B block that is fully or partially contained in the uncorrectable codeword with an Error Control Block (control block type 0x1E, with 8 /E/ (0x1E) control characters

The Staircase FEC decoder indicates errors to the PCS sublayer by replacing all 66-bit blocks fully or partially contained within an uncorrected codeword (including uncorrectable codewords, or potentially mis-corrected or not fully corrected codewords) with error control blocks. An error control block has control block type 0x1E and carries eight /E/ control characters. The marking includes a 66-bit block that begins in the Staircase FEC codeword preceding the uncorrected Staircase FEC codeword and ending in the uncorrected codeword, and a 66-bit block that begins in the uncorrected codeword and ends in the next codeword.

- Note that had 66B sync headers been corrupted, this would have turned the blocks into error control blocks if an Inverse RS-FEC/RS-FEC encoder/decoder been used across the C2M interface.

THANKS!