Multi-PCS Lane Distribution Delay Compensation

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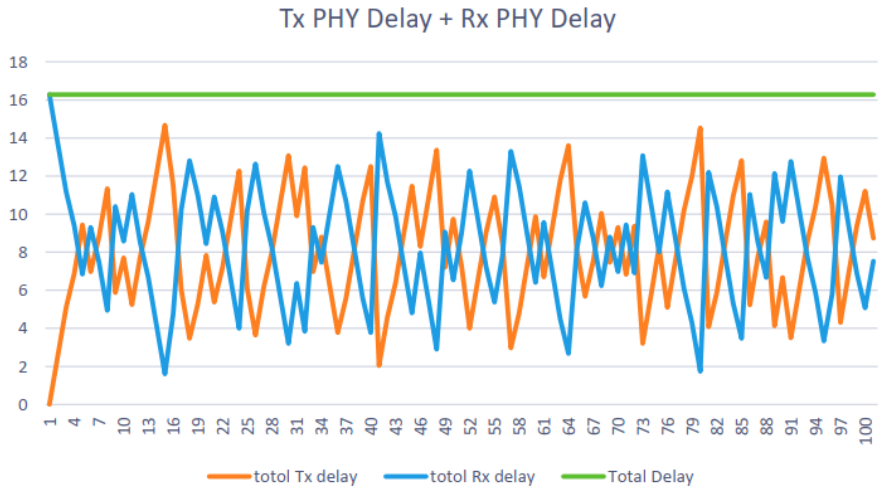
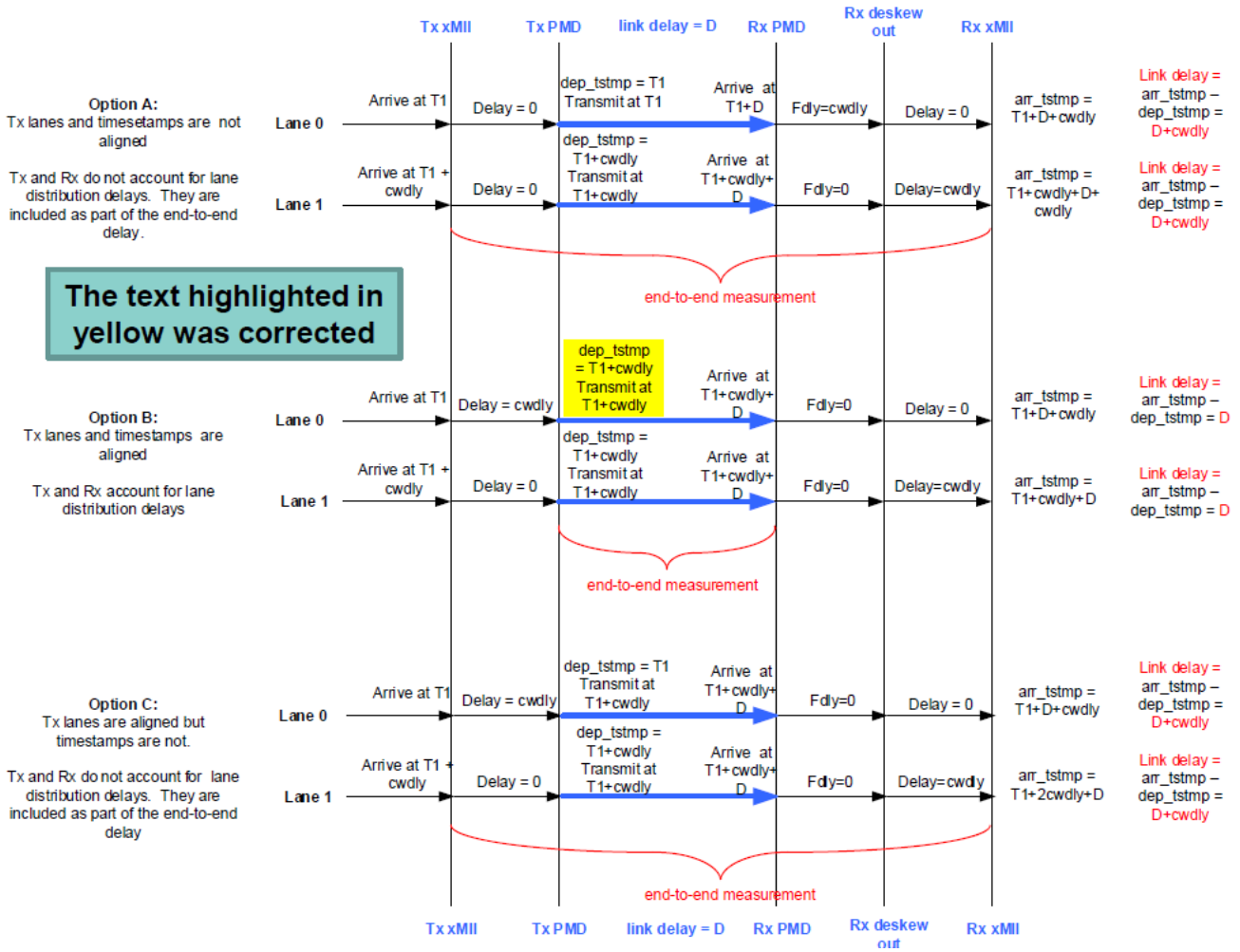
Background

- tse_3cx_02_0520 lists three possible solutions to compensate timestamp error caused by multi-PCS lane distribution.

- tse_3cx_03_0520 proposed to use the sum of Tx and Rx delay to cancel out the intrinsic delay variation caused by PHY sublayers.



tse_3cx_03_0520



tse_3cx_02_0520

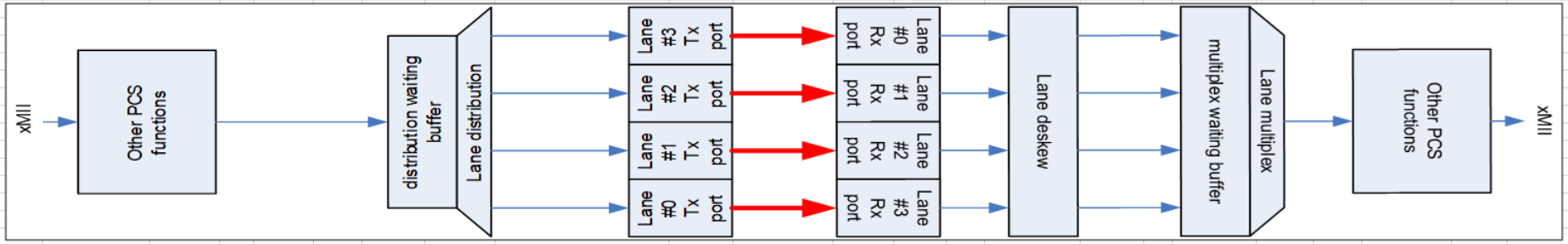
Proposed solutions

- tse_3cx_02_0520 lists three options to generate timestamps at Tx:
  - Option A: 66B blocks and timestamps are not aligned at NxPCS lane transmitter
  - Option B: 66B blocks and timestamps are aligned at NxPCS lane transmitter
  - Option C: 66B blocks are aligned but timestamps are not aligned at NxPCS lane transmitter
- And two methods for compensating multi-PCS lane distribution delay
  - Method 1: Account for the delay between the MII and the lane that carries the message timestamp point of the PTP message
  - Method 2: Use a constant delay regardless of which lane carries the message timestamp point, because the Tx+Rx lane distribution delay is a constant for every lane.
- Two different approaches were proposed in tse_3cx_02_0520 and he_3cx_01_0520.
  - Approach 1: Option C + Method 2, where Tx and Rx compensate a constant delay instead of the accurate delay, because the sum of the end-to-end intrinsic delay is constant.
  - Approach 2: Option B + Method 1, where Tx and Rx accurately compensate TS delay from xMII to MDI.

Multilane PCS distribution delay

- A spreadsheet tse_multilane_TE_analysis gives a good explanation about the PCS multilane distribution delay of 100GE. The TX and RX delay are variable, but the sum of TX and RX is constant.

Block Time	640	ps	time of one block's worth of data (i.e. 64 bits of uncoded data)
Tx Option	C		Blocks on NxPCS lane Tx MDI are aligned, xMII to MDI delay is different for every Tx PCS lane, blocks on Tx PCS lanes have different timestamps because a predetermined constant lane distribution delay is used for all lanes
Rx Option	2		Each Rx lane's MDI to xMII delay is different, but is accounted for as a predetermined constant delay because it can be balanced by a mirror delay on the Tx side
Link delay	0	ps	assumes the same delay for all lanes
Number of lanes	20		number of PCS lanes (max = 20)
Resulting time error	**0**	ps	



Lane	actual arvl time	actual distrib dly	actual dept time	actual arrival time	actual deskew dly	actual merge dly	actual arrival time
0	0	12160	12160	12160	0	0	12160
1	640	11520	12160	12160	0	640	12800
2	1280	10880	12160	12160	0	1280	13440
3	1920	10240	12160	12160	0	1920	14080
4	2560	9600	12160	12160	0	2560	14720
5	3200	8960	12160	12160	0	3200	15360
6	3840	8320	12160	12160	0	3840	16000
7	4480	7680	12160	12160	0	4480	16640
8	5120	7040	12160	12160	0	5120	17280
9	5760	6400	12160	12160	0	5760	17920
10	6400	5760	12160	12160	0	6400	18560
11	7040	5120	12160	12160	0	7040	19200
12	7680	4480	12160	12160	0	7680	19840
13	8320	3840	12160	12160	0	8320	20480
14	8960	3200	12160	12160	0	8960	21120
15	9600	2560	12160	12160	0	9600	21760
16	10240	1920	12160	12160	0	10240	22400
17	10880	1280	12160	12160	0	10880	23040
18	11520	640	12160	12160	0	11520	23680
19	12160	0	12160	12160	0	12160	24320

Multilane TX distribution delay

Multilane RX distribution delay

Time error caused by different compensation methods

- The spreadsheet also shows time error could be as much as ~6ns if Tx and Rx use different options.
  - Data delay measurement as in current standard requires inclusion of all latency caused by the protocol stack between the point timestamp is generated and the reference plane (MDI).
  - All ports in compliance with the current standard will suffer the 6ns time error if the other side chooses to ignore the PCS lane distribution delay and relying on error cancellation.

Block Time	640	ps	Block Time	640	ps
Tx Option	A		Tx Option	A	
Rx Option	1		Rx Option	2	
Link delay	0	ps	Link delay	0	ps
Number of lanes	20		Number of lanes	20	
Resulting time error	**0**	ps	**Resulting time error**	**6080**	ps
Block Time	640	ps	Block Time	640	ps
Tx Option	B		Tx Option	B	
Rx Option	1		Rx Option	2	
Link delay	0	ps	Link delay	0	ps
Number of lanes	20		Number of lanes	20	
Resulting time error	**0**	ps	**Resulting time error**	**6080**	ps
Block Time	640	ps	Block Time	640	ps
Tx Option	C		Tx Option	C	
Rx Option	1		Rx Option	2	
Link delay	0	ps	Link delay	0	ps
Number of lanes	20		Number of lanes	20	
Resulting time error	**6080**	ps	**Resulting time error**	**0**	ps

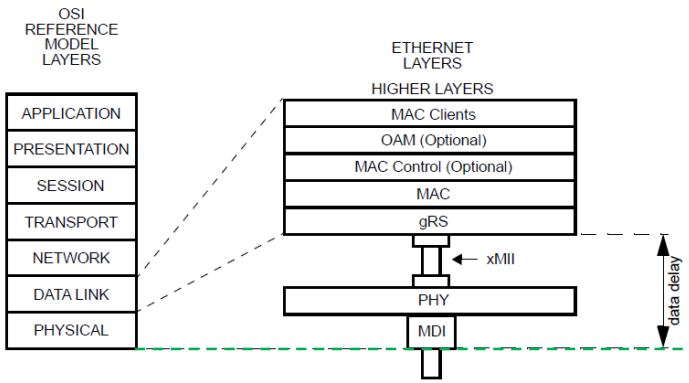


Figure 90–3—Data delay measurement

IEEE Std 1588-2008
IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems

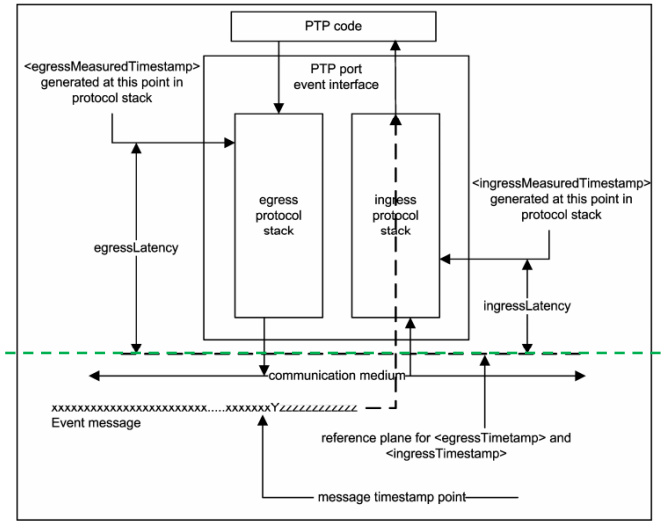


Figure 19—Definition of latency constants

Reference plane defined in IEEE802.3 and IEEE1588

Accurate compensation of multilane distribution delay

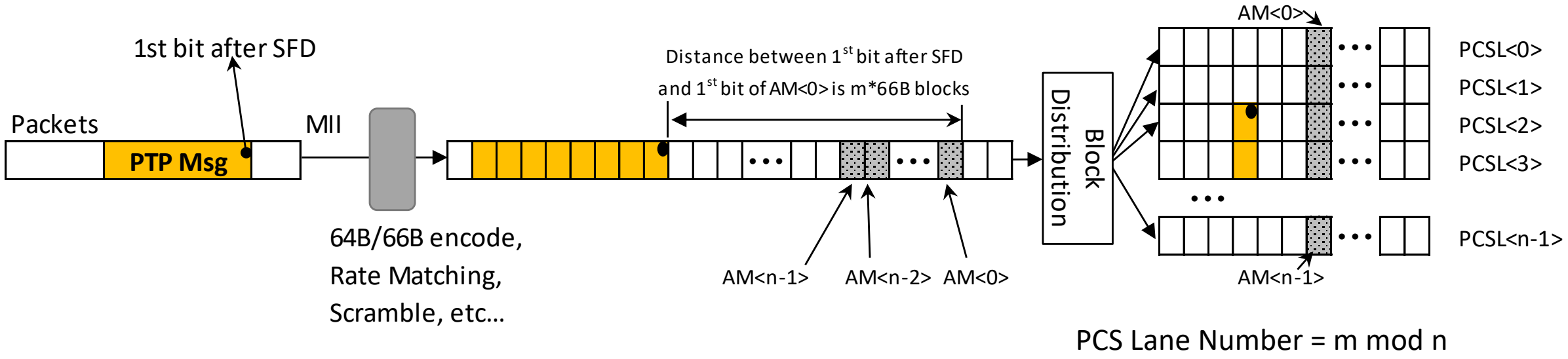
- This slide provides a method how to do the accurate compensation.
  - If the PCS lane number of PTP reference point can be known, the multilane distribution delay can be calculated.
  - For example, if the PTP reference point is carried by lane #3, the multilane Tx distribution delay would be (19 – 3) * 640ps = 10240ps, and the multilane Rx distribution delay would be 3*640 = 1920ps.

Lane	0	actual arvl time	0	actual distrib dly	12160	actual dept time	12160	actual arrival time	12160	actual deskew dly	0	actual merge dly	0	actual arrival time	12160
	1		640		11520		12160		12160		0		640		12800
	2		1280		10880		12160		12160		0		1280		13440
	3		1920		10240		12160		12160		0		1920		14080
	4		2560		9600		12160		12160		0		2560		14720
	5		3200		8960		12160		12160		0		3200		15360
	6		3840		8320		12160		12160		0		3840		16000
	7		4480		7680		12160		12160		0		4480		16640
	8		5120		7040		12160		12160		0		5120		17280
	9		5760		6400		12160		12160		0		5760		17920
	10		6400		5760		12160		12160		0		6400		18560
	11		7040		5120		12160		12160		0		7040		19200
	12		7680		4480		12160		12160		0		7680		19840
	13		8320		3840		12160		12160		0		8320		20480
	14		8960		3200		12160		12160		0		8960		21120
	15		9600		2560		12160		12160		0		9600		21760
	16		10240		1920		12160		12160		0		10240		22400
	17		10880		1280		12160		12160		0		10880		23040
	18		11520		640		12160		12160		0		11520		23680
	19		12160		0		12160		12160		0		12160		24320

  - Then the MAC can compensate the accurate delay into the PTP timestamp generated at xMII.
- Can we predict the lane number where the PTP reference point is?

Lane number prediction based on AM

- AM<0> is ALWAYS on lane 0.
- If the distance between the PTP TS reference point and AM<0> is known, then the PCS lane number where the PTP TS reference point is transmitted on can be accurately predicted.
  - An accurate compensation value thus can be calculated.
  - Similarly, knowing the distance between the PTP reference point and any AM block will also work.



Timestamp reference point tracing over MAC-PHY interconnection

- High speed MAC-PHY connection runs over AUI (e.g. CAUI for 100 GbE), which requires PCS functions in the MAC chip.
  - IEEE 802.3 Figure 83D-1 gives and example of 100 GbE chip-to-chip interface.
- PCS lane distribution is done in 100GBASE-R PCS.
- The number of PCS lane that transmits the PTP TS reference can be either inferred or calculated.
- The PCS lane number is kept unchanged over the whole interface.

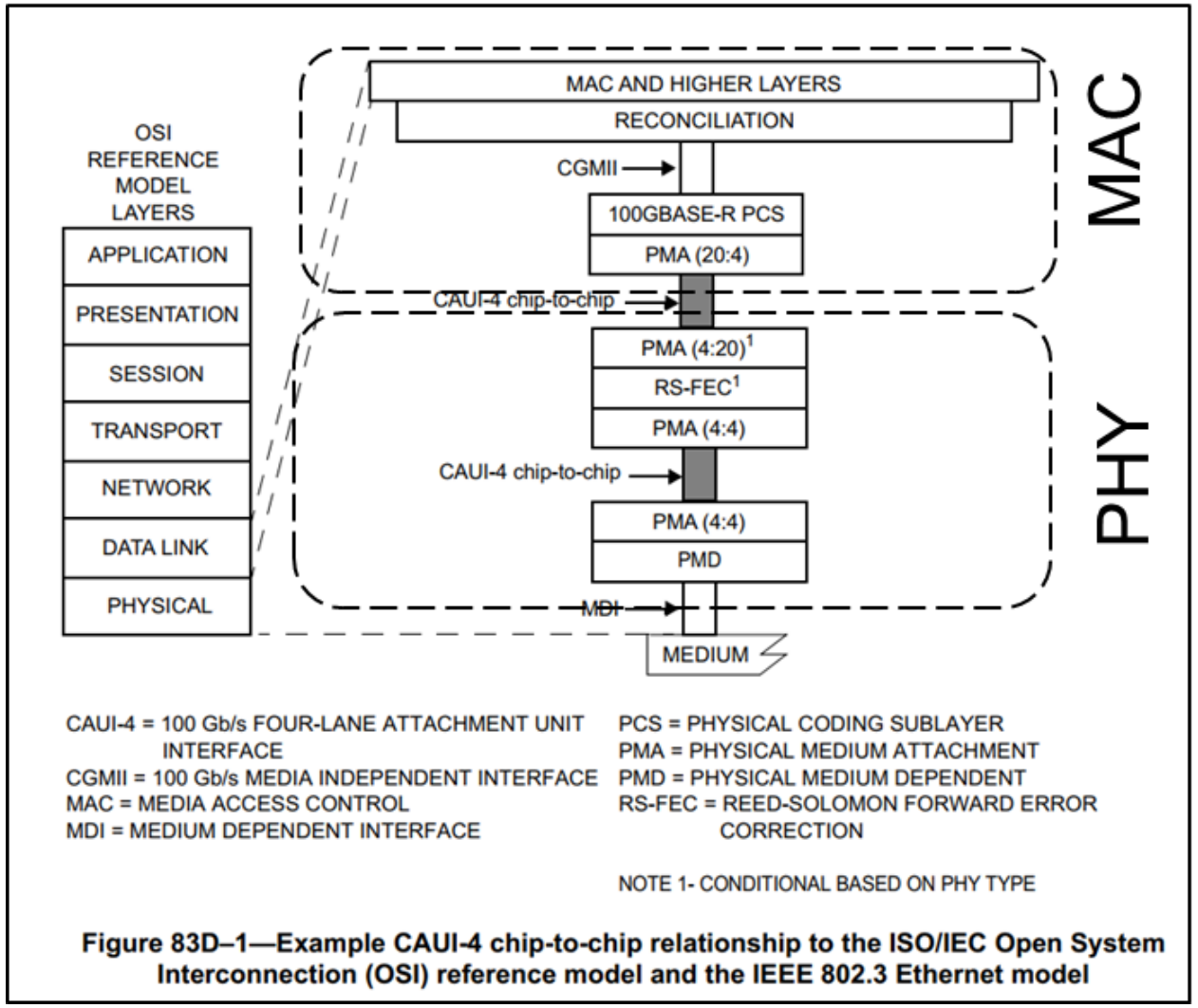


Figure 83D–1—Example CAUI-4 chip-to-chip relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

Summary

- The multilane distribution delay can be accurately calculated and compensated.
  - Location (# of PCSL) of PTP timestamp reference point can be predicted using the distance between PTP timestamp reference point and the AM.
- It is recommended to compensate the multilane distribution delay so that the timestamp is aligned with the MDI reference plane.
  - To avoid the possible ~6ns time error between the old and new standards.

THANK YOU!

Inaccurate compensation of multilane distribution delay

- Option C + method 2 proposed in tse_3cx_02_0520 recommends to use the constant sum of Tx+Rx to cancel out multi-lane distribution delay.
  - tse_3cx_03_0520 extends this method to all other intrinsic delay introduced by the protocol stack.
- The equivalent reference plane is “floating”.
  - Time error is expected when two sides are following different methods.

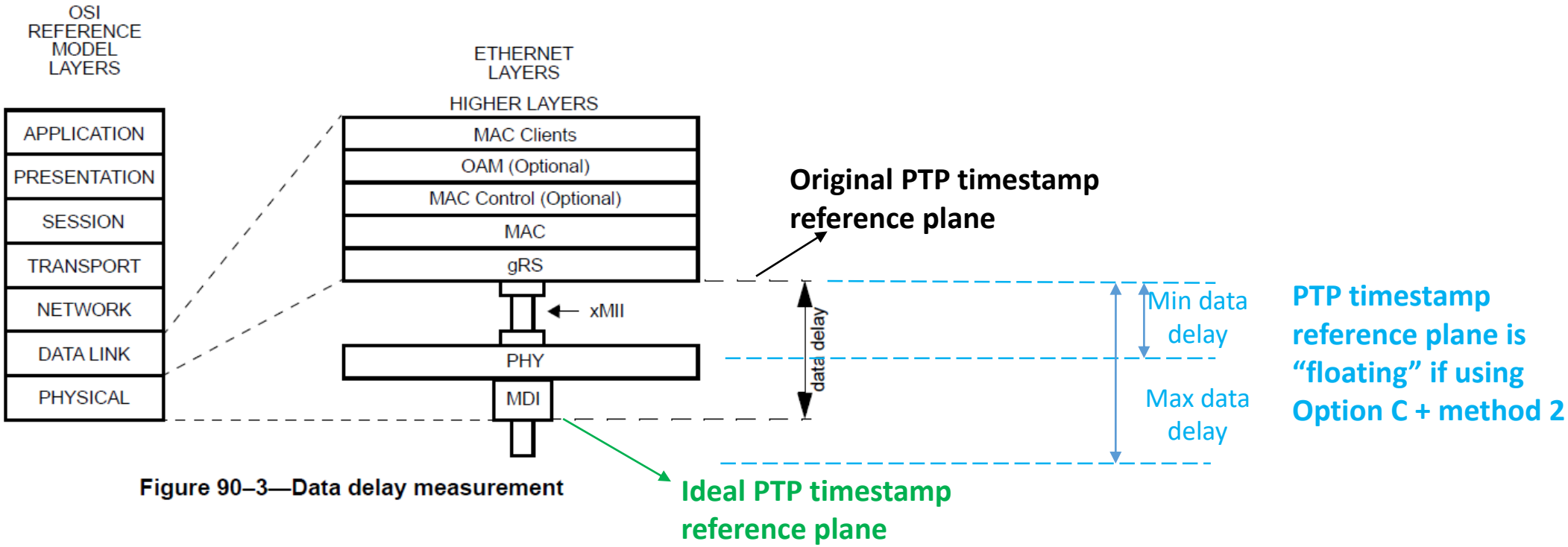


Figure 90–3—Data delay measurement

Accurate compensation of multilane distribution delay

- Option B + Method 1 proposed by [he_3cx_01_0520] requires accurate compensation on both sides.
- Extra work might be needed in the logic layer, and a method was proposed in this contribution.
- After the accurate compensation of multilane distribution delay, the PTP timestamp reference plane aligns with the ideal plane (MDI).

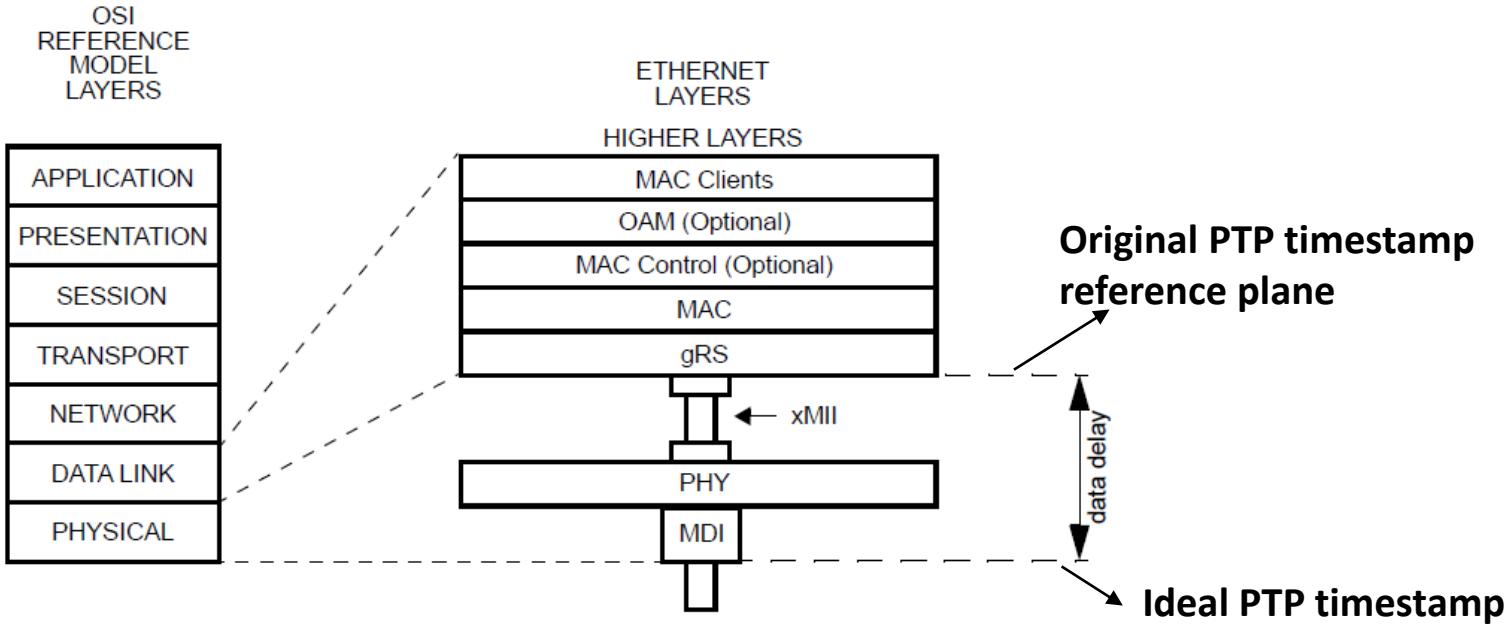


Figure 90–3—Data delay measurement