Cl **00** *SC* **0** *P* *L* # 785

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *EZ*

"groups of 130 65B blocks": elsewhere there are 64B/65B block and 65-bit block

SuggestedRemedy

Change "65B block" to "64B/65B block" or "65-bit block" as appropriate, throughout

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change "65B block" to "64B/65B block" throughout the draft.

Cl **45** *SC* **45.2.1.245.1** *P* **27** *L* **20** # 791

Wienckowski, Natalie General Motors

Comment Type **E** *Comment Status* **D** *EZ*

SuggestedRemedy

Delete red Editorial note.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **105** *SC* **105.1.2** *P* **33** *L* **42** # 792

McClellan, Brett Marvell

Comment Type **E** *Comment Status* **D** *EZ*

typo in editor's instruction

SuggestedRemedy

change 'Insert a new bullet e) in 10.5.2 as shown below.' to 'Insert a new bullet e) in 105.1.2 as shown below.'

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.1.3** *P* **37** *L* **35** # 784

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *EZ*

14 062.5 MBd - as the number is more than 10,000 and the space in a number with a decimal part is hard to parse, ...

SuggestedRemedy

It would be better to put this as 14.0625 GBd throughout. 8 changes.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.1.3** *P* **37** *L* **35** # 793

McClellan, Brett Marvell

Comment Type **E** *Comment Status* **D** *EZ*

D2.0 comment 637 instruction was not followed: delete 'rates'

SuggestedRemedy

implement as instructed

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change "transmitted at a 14 062.5 MBd rate" to "transmitted at 14 062.5 MBd"

Cl **165** *SC* **165.2.2.9.1** *P* **48** *L* **42** # 798

Zimmerman, George CME Consulting/APL Gp, Cisco, CommScope, Marve

Comment Type **E** *Comment Status* **D** *EZ*

the description of FALSE refers to the PCS where it should refer to the PHY (TRUE refers to the PHY)

SuggestedRemedy

Change "FALSE PCS is not in state PCS_Data" to "FALSE PHY is not in state PCS_Data"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.3.5** *P* **64** *L* **21** # 803

Jonsson, Ragnar Marvell

Comment Type **ER** *Comment Status* **D**

Incorrect equation numbering: Equaiton identifier (165-1) was previusly used for equation on page 58, line 36.

SuggestedRemedy

Update equation numbers to have consistent unique numbering thrughout the document.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.3.5** *P* **64** *L* **21** # 802

Jonsson, Ragnar Marvell

Comment Type **TR** *Comment Status* **D**

Incorrect range in the first case in the equation.

SuggestedRemedy

Equation (165-1): change “less than or equal to 17654” to “less than 17646” OR to “less than or equal to 17645”

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

change “less than or equal to 17654” to “less than 17646”

Cl **165** *SC* **165.3.7.3** *P* **68** *L* **16** # 794

McClellan, Brett Marvell

Comment Type **T** *Comment Status* **D**

missing a description of Figure 165–14—EEE transmit state diagram

SuggestedRemedy

insert "The EEE transmit state diagram shown in Figure 165–14 controls transitions between normal operation and low power idle."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.4.2.4.3** *P* **67** *L* **6** # 786

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D**

Partial PHY frame count

SuggestedRemedy

Delete "PHY". There are a few more

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change all instances of "partial PHY frame count" to "partial frame count"

Cl **165** *SC* **165.4.2.4.6** *P* **78** *L* **51** # 790

Wienckowski, Natalie General Motors

Comment Type **T** *Comment Status* **D** *DataSwPFC24*

Change based on D2.0 comments #647 and #471.

SuggestedRemedy

Change: DataSwPFC24 shall be set to an integer multiple of 32. When the value of DataSwPFC24 is a multiple of 16 the switch from PAM2 to PAM4 occurs on a PHY frame boundary.
To: When the value of DataSwPFC24 is a multiple of 32 the switch from PAM2 to PAM4 occurs on a L=8 superframe boundary.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See comment #795

Cl **165** *SC* **165.4.2.4.6** *P* **78** *L* **52** # 795

McClellan, Brett Marvell

Comment Type **E** *Comment Status* **D** *DataSwPFC24*

delete sentence per instruction of D2.0 comment 710 resolution

SuggestedRemedy

When the value of
delete "When the value of DataSwPFC24 is a multiple of 16 the switch from PAM2 to PAM4 occurs on a PHY frame boundary. DataSwPFC24"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.4.2.4.6** *P* **79** *L* **1** # 789

Wienckowski, Natalie General Motors

Comment Type **E** *Comment Status* **D** *EZ*

SuggestedRemedy

Delete red Editorial note.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.4.2.6** *P* **81** *L* **10** # 787

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D**

"signaling rate of the SEND_S signal shall be 703.125 MHz" Is that signaling rate (MBd) or pattern repetition rate?

SuggestedRemedy

Change MHz to MBd?

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The following changes are made:

Delete the text "The nominal signaling rate of the SEND_S signal shall be 703.125 MHz."

Revise the existing statement by adding statement in <<>>:
"An implementation of MASTER and SLAVE PHY SEND_S PN sequence generators by linear-feedback shift registers is shown in Figure 165–20. The bits stored in the shift register delay line at time n are denoted by Sn[7:0]. <<The symbols of the shift register sequence Sn[] shall be generated at a rate of 703.125 MHz.>> At each symbol period, the shift register is advanced by one bit, and one new bit represented by Sn[0] is generated. The PN sequence generator shift registers shall be reset to a value of Sn[7:0] = 0000 0001 upon entering into the TRANSMIT_DISABLE state (see Figure 165–20) or on the transmission of the first symbol of the alert sequence. The receiver may not necessarily receive a continuous PN sequence between separate periods of the SEND_S signal."

Update PICS as needed

Cl **165** *SC* **165.5.2** *P* **93** *L* **25** # 788

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *EZ*

"25GBASE-T1: 1x" looks like a leftover from a diagram that included more lanes

SuggestedRemedy

Delete

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Delete ": 1x"

Cl **165** *SC* **165.5.3** *P* **93** *L* **17** # 781

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D**

For some of the measurements where a high speed signal is to be observed with a scope, there should be a specified scope bandwidth. fb x 3/4 is usual. This standardises the measurement and keeps some irrelevant instrument and DUT noise out of it.

SuggestedRemedy

This would be beneficial for 165.5.3.2 Transmitter linearity (SNDR), 165.5.3.3.1, 2 Transmit MDI jitter in MASTER mode and 165.5.3.5, and harmless for some others such as droop.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

No specific change proposed

Cl **165** *SC* **165.5.3.3** *P* **95** *L* **5** # 782

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D**

Jitter measurement bandwidth "at least 200 MHz" same as it was in 149 for a slower divided clock, and open ended.

SuggestedRemedy

Should it be increased? Give a value or range rather than "at least"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

No specific change proposed.

Cl **165** *SC* **165.5.3.3** *P* **95** *L* **8** # 783

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D**

Measuring jitter on 0.4 ms blocks with no clock recovery unit in the measurement gives an extremely low (~ kHz) implied high-pass jitter measurement corner. 165.5.3.3.2 has fn = 2.5 MHz which is much higher.

SuggestedRemedy

Should there be a "soft" CRU function not just linear regression in the TIE analysis?

Proposed Response *Response Status* **W**

PROPOSED REJECT.

No specific proposed change.

Cl **165** *SC* **165.5.3.4** *P* **96** *L* **1** # 799

Zimmerman, George CME Consulting/APL Gp, Cisco, CommScope, Marve

Comment Type **T** *Comment Status* **D** *LFL*

I realize this is out of scope, and the comment is made to put the issue on the table - for resolution at initial SA ballot. The lower frequency ranges for the PHY, Link Segment specifications, and MDI are all over the place. Starting at 0 Hz is not going to be practical for measurements of a PSD going to up to 13.75 GHz. Likewise, the ANEXT and AFEXT loss are constrained starting at 1 MHz - also too low for practicality. Additionally, the TX PSD lower bound frequency is 5 MHz - below the link segment low frequency limit of the insertion loss. For all of these, going this low won't be necessary for link segments starting at 10 MHz. Suggest they be aligned at 10 MHz.

Unlike my subsequent comments on return loss, I think this comment is likely ready to make the change.

SuggestedRemedy

Change low frequency limit for Upper TX PSD mask (eq 165-6, Pg 96 line 1), Lower TX PSD mask (eq 165-7, Pg 96 line 7), PSANEXT (eq 165-35, Pg 108 line 24), and PSAFEXT (eq 165-36, Pg 109 line 18) to 10 MHz.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.7.1.3.1** *P* **102** *L* **51** # 800

Zimmerman, George CME Consulting/APL Gp, Cisco, CommScope, Marve

Comment Type **T** *Comment Status* **D** *LFL*

(also out of scope)
Link segment return loss specifications start at 30 MHz, whereas the link segment return loss is constrained (at least) by the Insertion loss between 10 MHz and 30 MHz (at least 6.8dB RL at 10 MHz to meet the IL at 10 MHz)

While I've proposed a remedy, I think this needs further thought and I would be OK rejecting this comment and working on it with the TF for initial SA ballot.

SuggestedRemedy

Consider changing the low frequency limit for link segment return loss Eq 165-17 at pg 102 line 51 from 30 MHz to 10 Mhz and adding a frequency range from 10 Mhz to 30 MHz to Equation 165-17 with value of 20 - 6.5 * (30-f)/10 dB 10 <= f < 30 MHz.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.7.1.3.4** *P* **106** *L* **13** # 796

Sedarat, Hossein Ethernovia

Comment Type **T** *Comment Status* **D**

The last sentence was eliminated from step 8 which makes the last step of ETM calcualationn procedure incomplete and ambiguous.

SuggestedRemedy

Change the sentency in step 8 to: "Apply steps 3, 4, and 5 to partial response g_n^m (instead of h_n) to calculate the associated REM. The ETM(m) is this REM calculated for g_n^m and evaluated at Ndiscard_etm."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.7.1.6** *P* **107** *L* **47** # 797

Sedarat, Hossein Ethernovia

Comment Type **T** *Comment Status* **D**

The maximum propagation delay of 69 ns is excessively large and may unnecessarily add complexity to the echo canceller. A value of 55 ns provides roughly 10% margin with respect to available measurements of current (802.3ch-grade) and future (802.3cy-grade) cables. More discussion on the topic can be found on email reflector: https://www.ieee802.org/3/B10GAUTO/email/msg00389.html

SuggestedRemedy

replace 69 ns with 55 ns.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **165** *SC* **165.8.2.1** *P* **110** *L* **21** # 801

Zimmerman, George CME Consulting/APL Gp, Cisco, CommScope, Marve

Comment Type **T** *Comment Status* **D** *LFL*

Why is the link segement return loss only to 30 MHz when the MDI return loss is constrained starting at 5 MHz? These require study and should be considered for changes at initial SA ballot. Whatever considerations are important for one RL are equally applicable to the other. It probably is not relevant to constrain the MDI RL down to 0 dB RL (which is is at 5 MHz). At 10 Mhz, the lower end of the IL spec, the MDI RL is 6 dB as written.

While I've proposed a remedy, I think this needs further thought and I would be OK rejecting this comment and working on it with the TF for initial SA ballot.

SuggestedRemedy

Change MDI return loss lower limit to 10 MHz. (eq 165-37), pg 110, line 21, maintaining the existing equation, except for the frequency limit change.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change MDI return loss lower limit to 10 MHz. (eq 165-37), pg 110, line 21