

P802.3cy Annex 165A Proposal

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Background

- P802.3ch included informative Annex 149C Tx Function to Rx function channel characteristics to provide direction on ECU design to facilitate proper operation of the link
- We are proposing informative Annex 165A Tx Function to Rx function channel characteristics to do the same, with the addition of the test points as defined in [802.3cy Test Fixture Considerations](#)
- This presentation provides a proposal for the informative Annex

Annex 165A

(informative)

Tx function to Rx function channel characteristics

165A.1 Overview

Annex 165A provides information on insertion loss and return loss parameters of the channel defined between Tx function and Rx function illustrated in Figure 165A–1. Table 165-y1 describes the test points illustrated in Figure 165A–1.

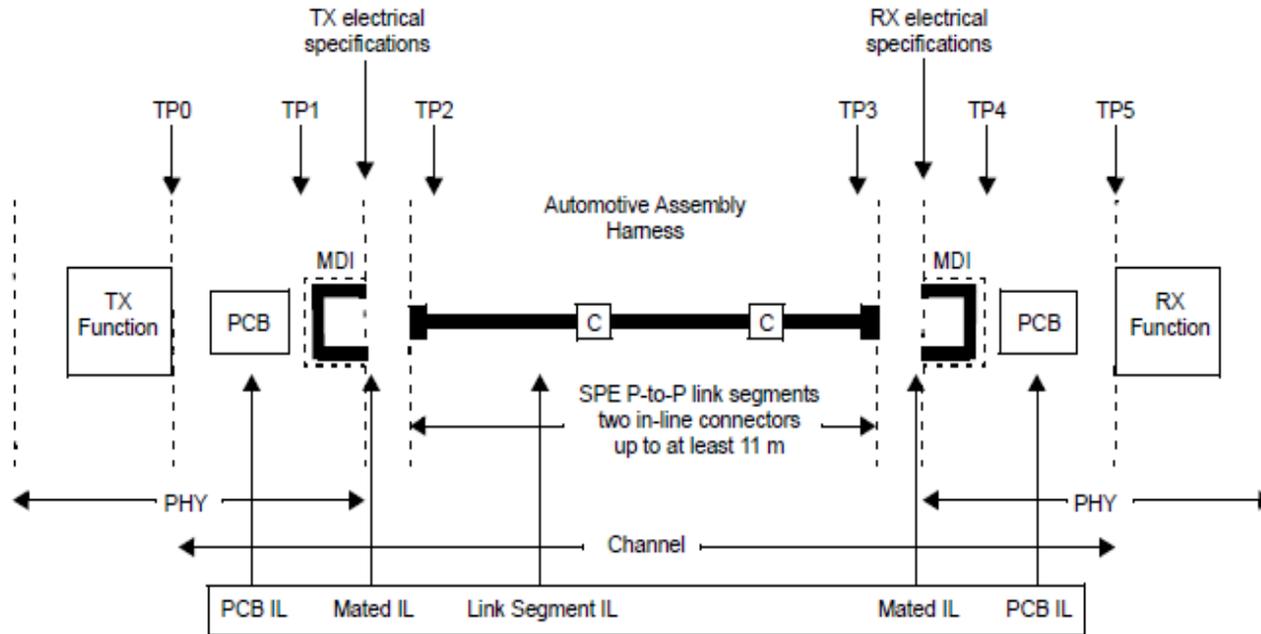


Figure 165A–1—Channel Tx function to Rx function

165A.2 TP2/TP3 to TP0/TP5 reference insertion loss

The recommended maximum insertion loss from TP2/TP3 to TP0/TP5 including the test fixture is shown in Figure 165A-2. Figure 165A-2 includes the host PCB, a mated connector pair, and the HTF reference insertion losses. All losses shown are at 7031.25 MHz.

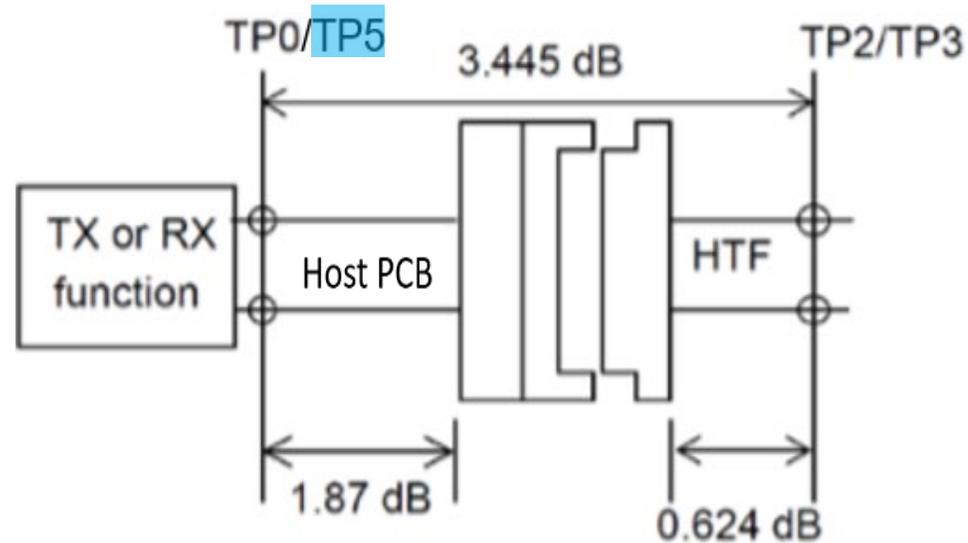


Figure 165A-2—TP2/TP3 to TP0/TP5 reference insertion loss

165A.2.1 Host PCB trace loss

The recommended maximum insertion loss for the Host PCB is determined using Equation (165A–1) and illustrated in Figure 165A–1. The recommended printed circuit board trace insertion loss is based on a 76.2 mm trace length. The recommended maximum insertion loss is 1.871 dB at 7031.25 MHz.

$$IL_{PCB}(f) \leq IL_{PCBmax}(f) = 0.09144 \left(\frac{f_{MHz}}{1000} \right) + 0.51054 \left(\frac{f_{MHz}}{1000} \right)^{0.45} \text{ dB} \quad (165A-1)$$

where

f is the frequency in MHz; $10 \leq f \leq 9000$

The recommended minimum insertion loss for the Host PCB is determined using Equation (165A–2) and illustrated in Figure 165A–1. The recommended printed circuit board trace insertion loss is based on a 25.4 mm trace length. The recommended minimum insertion loss is 0.624 dB at 7031.25 MHz.

$$IL_{PCB}(f) \geq IL_{PCBmin}(f) = 0.03048 \left(\frac{f_{MHz}}{1000} \right) + 0.17018 \left(\frac{f_{MHz}}{1000} \right)^{0.45} \text{ dB} \quad (165A-2)$$

where

f is the frequency in MHz; $10 \leq f \leq 9000$

165A.3 TP0 to TP5 channel insertion loss

The channel insertion loss from TP0 to TP5 is determined using Equation (165A-3), Equation (165A-4), and Equation (165A-5).

$$IL_{Channel} (dB) \leq 2 \cdot IL_{PCBmax}(f) + 2 \cdot IL_{MDI\ connector} + IL_{Linksegment} \quad (165A-3)$$

$$IL_{MDI\ connector} (dB) \leq 0.1 \sqrt{\frac{f_{MHz}}{2500}} \quad (165A-4)$$

$$IL_{LinkSegment} (dB) \leq 0.00135(f_{MHz}) + 0.3564(f_{MHz})^{0.45} + 0.495 \left(\frac{f_{MHz}}{7500} \right)^6 \quad (165A-5)$$

where

f is the frequency in MHz; $10 \leq f \leq 9000$ for Equation (165A-4) and Equation (165A-5).

The 25GBASE-T1 PHY (or one lane of a 50GBASE-T2 or 100GBASE-T4 PHY) utilizes 4-level pulse amplitude modulation (PAM4) transmitted at 14 062.5 MBd. Table 165A–1 shows the recommended maximum insertion losses for the channel and channel components at the Nyquist frequency for this PHY.

Table 165A–1—TP0 to TP5 Channel insertion loss

PHY	Rate MBd	Nyquist Frequency (MHz)	IL_{PCBmax} (dB)	IL_{LinkSegment} (dB)	IL_{MDI connector} (dB)	IL_{channel} (dB)
25GBASE-T1	14 062.5	7031.25	1.871	29.02	0.168	33.098

165A.4 Channel return loss

The channel topology between Tx function and Rx function illustrated in Figure 149C–2 consists of the Tx function to MDI, the link segment, and the MDI to Rx function. The channel return loss can be modeled as a concatenation of the Tx function to MDI return loss, the link segment return loss, and the MDI to Rx function return loss.



Figure 165A-3: Tx/Rx function channel topology

Example implementations for the Tx function and Rx function to MDI topologies are as shown in Figure 149C-3 and Figure 149C-4. For Clause 165 PHYs, the informative values for components are given in Table 165A-2.

Table 165A–2—Analysis parameters and values

Element	Unit	Minimum	Nominal	Maximum
RT	Ω	45	50	55
ZO	Ω	45	50	55
CT	pF	—	TBD	—
LP	μ H	—	TBD	—
CP	pF	—	TBD	—
CESD	pF	—	TBD	—
CAC	nF	—	TBD	—

For additional information on modeling the return loss, See Annex 149C.

165A.5 Coupling between ports on multiport designs

When multiple MultiGBASE-T1 lanes/PHYs are implemented on the same board, care should be taken to avoid coupling between ports. The coupling between adjacent ports on a multiport MDI connector or between adjacent balanced pairs is recommended to be approximately the same level, but no greater, than that specified for **TBD** crosstalk specified in Equation (165–**TBD**).

Questions?

