



Clarify EEE Quiet Signaling

Contribution to IEEE 802.3cy

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Introduction

- Our previous contribution [jonsson_majomard_3cy_01_04_05_22](https://www.ieee802.org/3/cy/public/adhoc/jonsson_majomard_3cy_01_04_05_22) discusses some design considerations for EEE, including
 - the importance of allowing both transmitter and receiver to take full advantage of Low Power Mode
 - to minimize constraints on transmitter and receiver while ensuring interoperability
- This presentation proposes simple changes to the existing EEE text to help with both these issues

Transition to and from EEE Mode

Transition to Data Mode

- Some applications may require specific limits on the latency in transitioning from EEE mode to data mode
- Transition to data mode can not cause link drop if the other transmit direction is already in data mode
- There may be requirements on super-frame alignment when transitioning to data mode

Transition to Low Power Mode

- The transition should be done in such a way that both transmitter and receiver can take full advantage of power savings in low power mode
- While in low power mode the requirements on the transmitter and receiver should be such that both sides can minimize power consumption

The EEE transitions should minimize constraints on transmitter and receiver, while ensuring reliable interaction between the transmitter and receiver

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From:

https://www.ieee802.org/3/cy/public/adhoc/jonsson_majomard_3cy_01_04_05_22.pdf

802.3ch QR State Transition Requirements

- The 802.3ch EEE description implies that the Tx should not transmit any signal during the Quiet Period (this may not be explicitly stated in the standard)
- This implies that the Tx needs to avoid any glitches or transitory signals once it enters Quiet Period
- This restrictions brings no value to the EEE interoperability, but it can make it harder for the Tx to transition to low power mode

149.3.6.2 Quiet period signaling

During the quiet period the PCS transmitter shall pass zeros to the PMA via the PMA_UNITDATA.request primitive.

149.3.6 LPI signaling

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. The transmit function of the PHY initiates a transition to the LPI transmit mode by generating the sleep signal comprised of eight RS-FEC frames composed entirely of LPI control characters, as described in 149.3.2.2.22. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

Within the LPI mode, PHYs use a repeating quiet-refresh cycle (see Figure 149–13 and Figure 149–14). The LPI timing parameters are shown in Table 149–5. The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time. The quiet period is defined in 149.3.6.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time. The refresh period is defined in 149.3.6.3. A cycle composed of one quiet period and one refresh period is known as an LPI cycle and lasts for a time lpi_qr_time.

The parameters lpi_offset, lpi_quiet_time, lpi_refresh_time, and lpi_qr_time are timing parameters that are integer multiples of the RS-FEC frame period. lpi_offset is a fixed value equal to $lpi_qr_time / 2 + 4$ (52 RS-FEC frame periods).

The end of LPI mode occurs at the transmission of the alert signal indicating the end of quiet-refresh cycle.

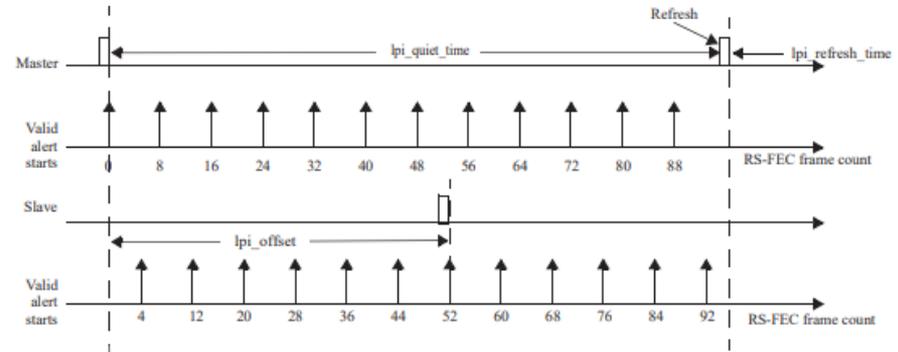


Figure 149–13—Timing periods for LPI signals when Slow Wake not active

Problem Statement and Motivation

The 149.3.6.2 text has two problems:

- It is ambiguous about what shall be transmitted on MDI, because 802.3ch does not define mapping to “zero voltage”, so PCS outputting zeros does not necessarily imply “zero voltage” on the MDI
- It does not state anything about transition period from “normal transmission” to quiet period

Why clarify the text:

- When transitioning to lower internal power state, the transmitter may introduce minor “glitches” on the line
- When transitioning to lower internal power state, the receiver may have some “glitches” in its internal signals
- Allowing for clearly specified transition period can benefit both transmitter and receiver, and help interoperability

Proposed Updates for the 802.3cy EEE Text

In 802.3cy, the text from 149.3.6.2 should be changed to

When entering quiet mode, the receiver shall ignore the first 330 ns (one RS-frame). During this time, the transmitter may output any signal within the bounds of PMA electrical limitations described 165.5.3. After this transition, the PCS transmitter shall pass all zeros to the PMA and the PMA shall transmit silence on the MDI.



149.3.6.2 Quiet period signaling

During the quiet period the PCS transmitter shall pass zeros to the PMA via the PMA_UNITDATA.request primitive.



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