Bit Error Ratio (BER) test mode proposal

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BER test mode: proposal

- BER test mode is for measurement of the bit error ratio (BER) of the link including the PCS, PMA, and PMD sublayers of two nGBASE-AU PHYs and a fiber optic cable connected to them. This mode reuses the normal (non-test) mode with PCS encoder generating Local Fault sequential ordered sets as in training mode.
- Operating in this test mode, the PCS transmitter shall generate LBLOCK_T containing two Local Fault sequential ordered sets regardless the link status and ignore the XGMII, 25GMII or 50GMII input.
- In the absence of errors, LBLOCK_T 65-bit sequences are expected after RS FEC decoder. Any data bit difference with respect LBLOCK_T binary sequence shall be computed as a bit error in the Bit Error Ratio (BER). Any RS code-word containing bit errors shall be counted as a RS code-word error and calculated in the RS-FEC block error ratio.
- The PCS receiver shall encode Local Fault ordered sets in the XGMII, 25GMII or 50GMII output.
- PMA and PMD functions shall operate as in normal mode (non-test) establishing the bidirectional link.
- The PHY shall announce to the link partner the BER test mode using the field PHD.TX.NEXT.MODE. The transmitter operating mode encoded in the field PHD.TX.NEXT.MODE is selected at PMA reset, and it does not change the value unless a PMA reset takes place. The receiver shall reconfigure its circuitry for normal operation or for BER test as function of the received PHD.TX.NEXT.MODE value.

BER test mode: additional explanations

- PCS 64B/65B transmit state diagram will remain in the TX_INIT state assigning tx_block <= LBLOCK_T
- PCS 64B/65B receive state diagram will remain in the RX_INIT state assigning rx_raw <= LBLOCK_R
- Acc. 802.3cz D1.1:
  - tx_block<64:0>: Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure166–12. The leftmost bit in the figure is tx_block<0> and the rightmost bit is tx_block<64>.
  - LBLOCK_T<64:0>: 65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.
  - rx_raw<71:0>: Vector containing two successive XGMII or 25GMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.
  - LBLOCK_R<71:0>: 72-bit vector to be sent to the xMII interface containing two Local Fault ordered sets.

PHD TX mode field

Table 166–2—PHD structure

Field name	Description	Number of bits	Valid values
PHD.TX.NEXT.MODE	Transmission mode of the next Transmit Block, indicated to link partner to align its reception (see TBD)	3	0: normal transmission 1 through 7: reserved

- Edit valid values column as:
  - 0: normal transmission
  - 1: BER test mode transmission
  - 2 through 7: reserved

PHY TX and RX control state diagrams

- PHY TX and RX control state diagrams need to be amended in order for the PCS 64B/65B encoder and decoder to operate according to the configured operation mode (normal transmission or BER test).
- PHD.TX.NEXT.MODE field local and remote values govern the PHY TX and RX control, respectively.

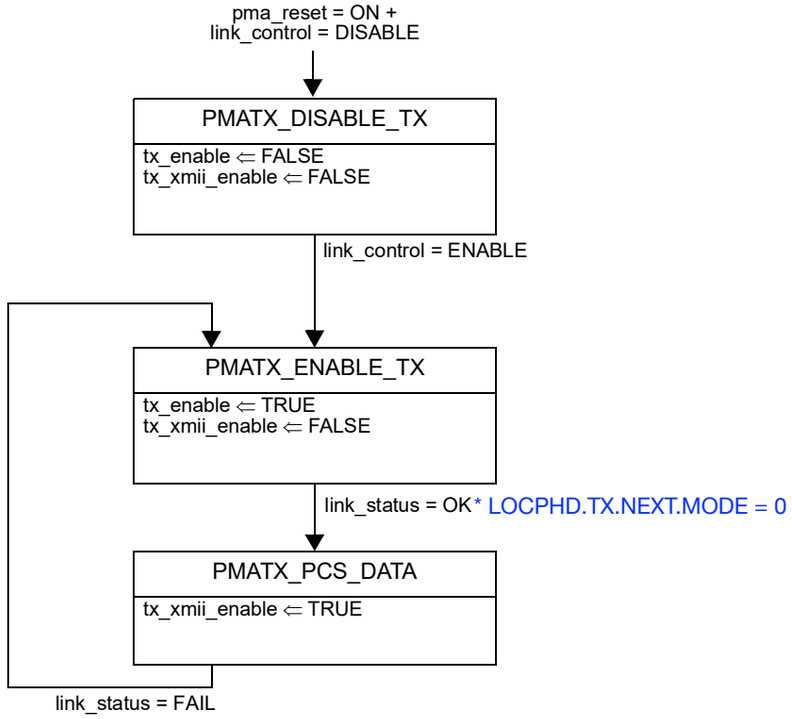

Figure 166–16—PHY TX control state diagram

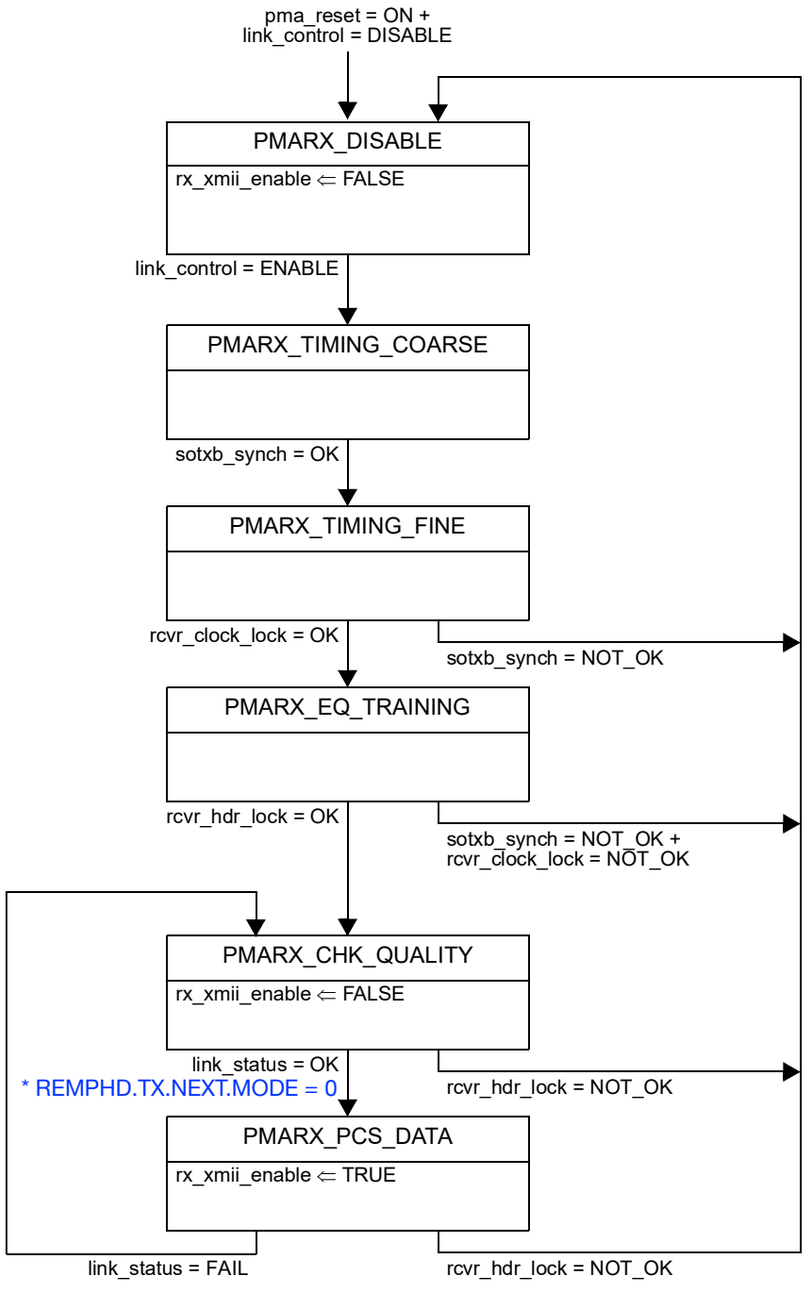

Figure 166–17—PHY RX control state diagram

64B/65B state diagrams: no changes

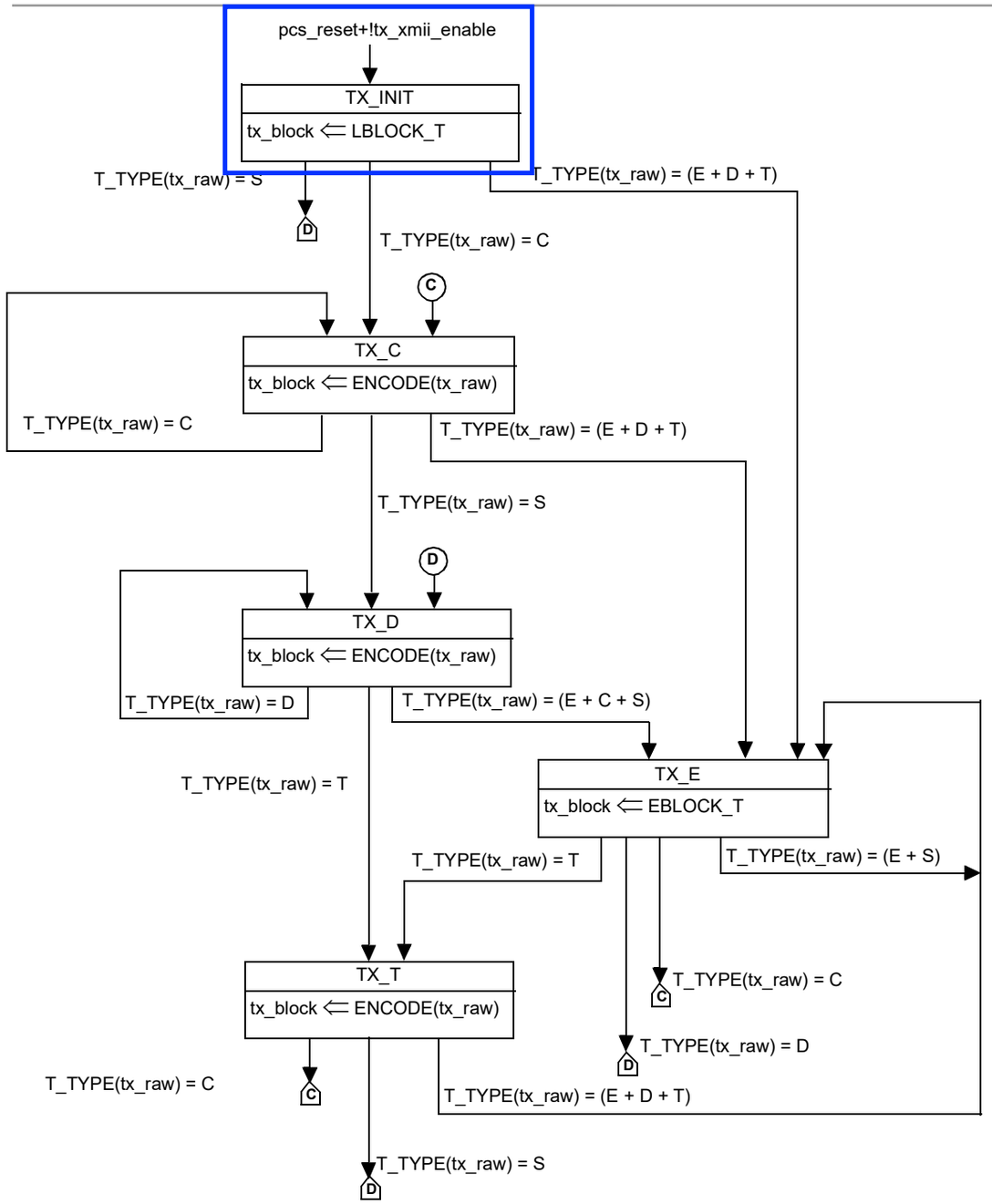

Figure 166–13—PCS 64B/65B transmit state diagram

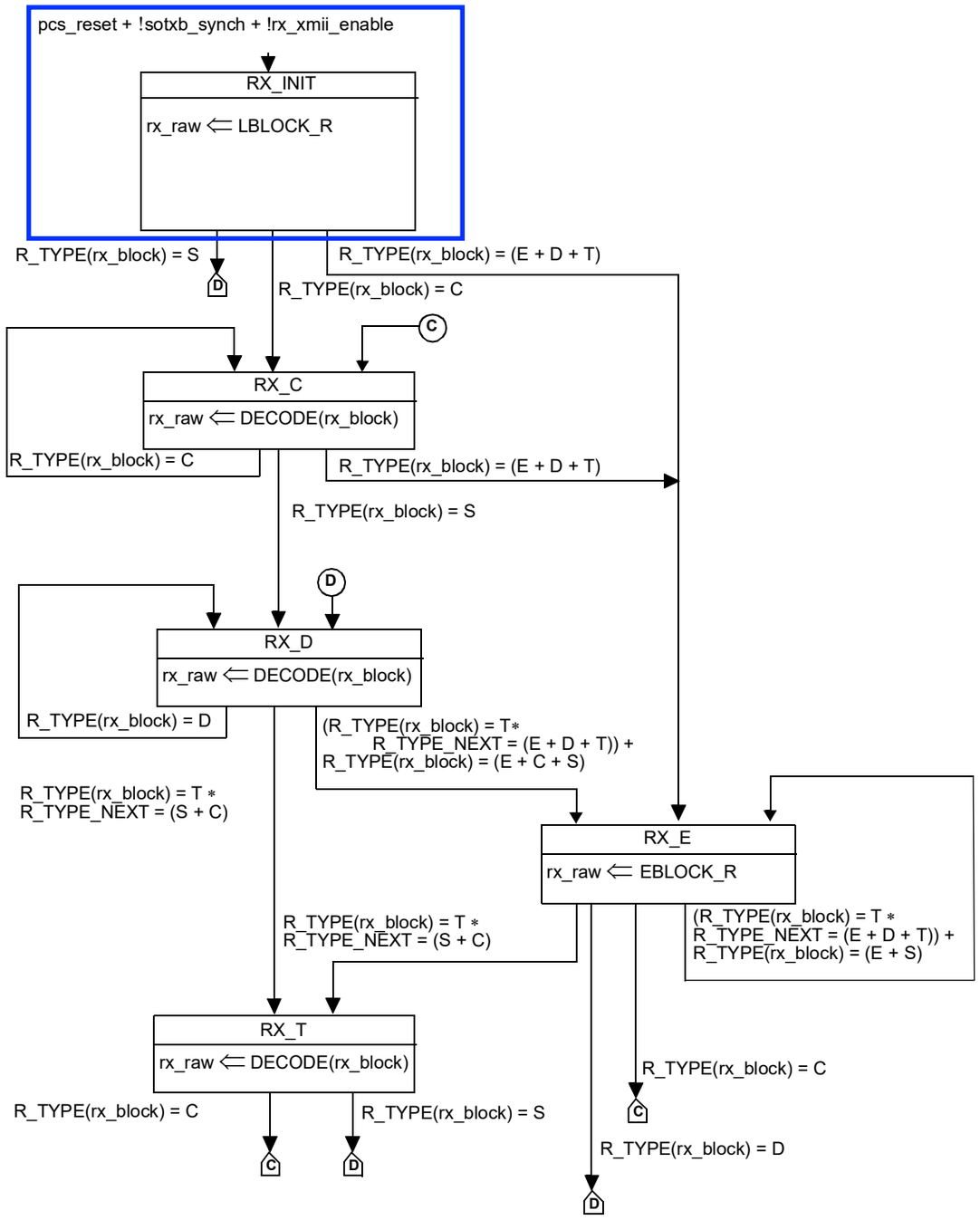

Figure 166–15—PCS 64B/65B receive state diagram

Table 45–244ec—BASE-U PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2348.15:13	Operation mode	15 14 13 0 0 0 = Normal operation 0 0 1 = BER test mode 0 1 x = Reserved 1 x x = Reserved	R/W

Table 45–244eg— BASE-U PCS status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2352.15:0	BER test mode counter	A 16-bit counter used when operating in BER test mode	RO, NR

[a]RO = Read only, NR = Non Roll-over

When the BASE-U based PHY receiver is operating in BER test mode, bits 3.2352.15:0 are a 16-bit counter that counts the number of erroneous bits received at the input of the 64B/65B PCS decoder.

These bits shall be reset to all zeros when the counter is read. The counter shall be held at all ones in the case of overflow.

- Add BASE-U PCS status 5 register similar to BASE-U PCS status 4 register for RS-FEC block error ratio
- Bits name: RS-FEC block error counter
- Description:
  - a 16-bit counter used when operating in BER test mode
  - when the BASE-U based PHY receiver is operating in BER test mode, bits 3.XXXX.15:0 are a 16-bit counter that counts the number of erroneous RS code-words in the input of the 64B/65B PCS decoder
- R/W: RO, NR

Thank you!