Big Picture for VR, and Interoperability

Ramana Murty, Broadcom Inc.

IEEE P802.3db 100 Gb/s, 200 Gb/s, and 400 Gb/s Short Reach Fiber Task Force

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TBDs for VR

There were multiple comments to resolve the TBDs on center wavelength, max TDECQ and length of reference equalizer for the VR link.

Center wavelength	13, 15, 65, 70
Max TDECQ	14, 16, 63, 67
Length of reference equalizer	64, 71

Response to all of the above is

PROPOSED REJECT
This comment must be viewed in the broader context of what features are best to include in the VR link. Isolated changes impact choices for other parameters.
Decision will be based on consensus.

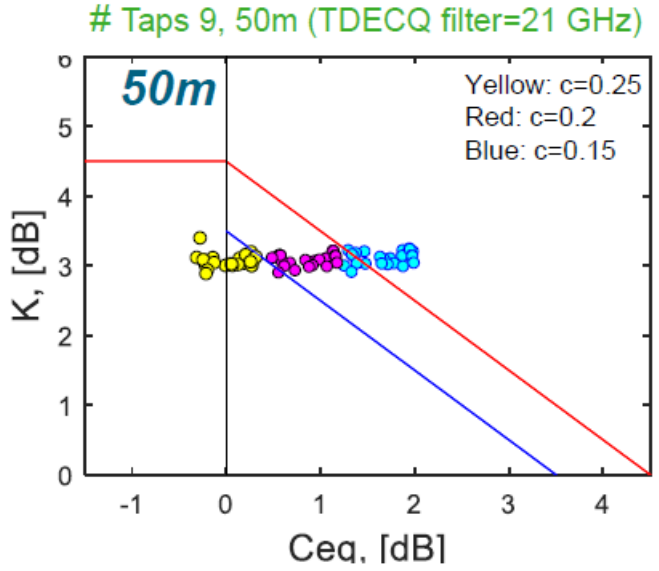
Key Aspects of VR

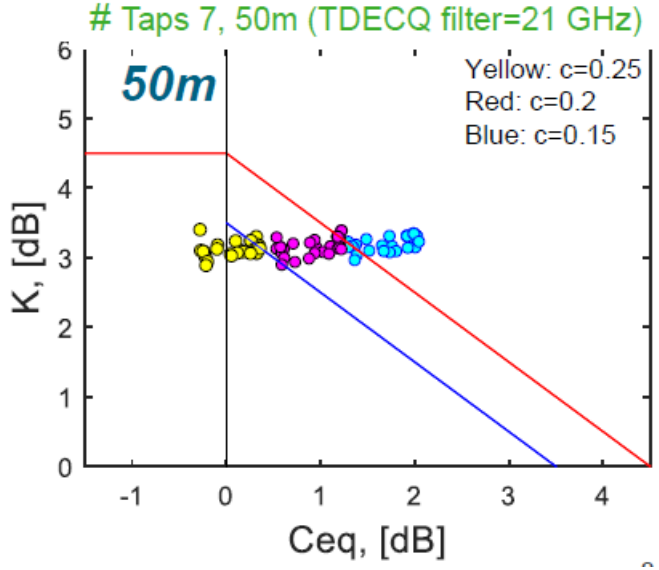
The VR link is expected to have some margin relative to the SR link. This margin is sought by

1. 850 nm VCSEL with lower bandwidth	Low cost
2. 940 nm VCSEL	Enable more VCSEL suppliers Device must be faster to compensate for the lower (0.6X) fiber bandwidth
3. Short reference equalizer	Enable analog solution using fewer (< 7) taps
4. Limit max TDECQ for the link	Reduced SECQ for stressed receiver sensitivity

940 nm	lewis_3db_01_070121.pdf
Reference equalizer	ali
Max TDECQ	latchman_3db_01_031621.pdf, castro_3db_adhoc_01_040121.pdf

850 nm Link – Simulations





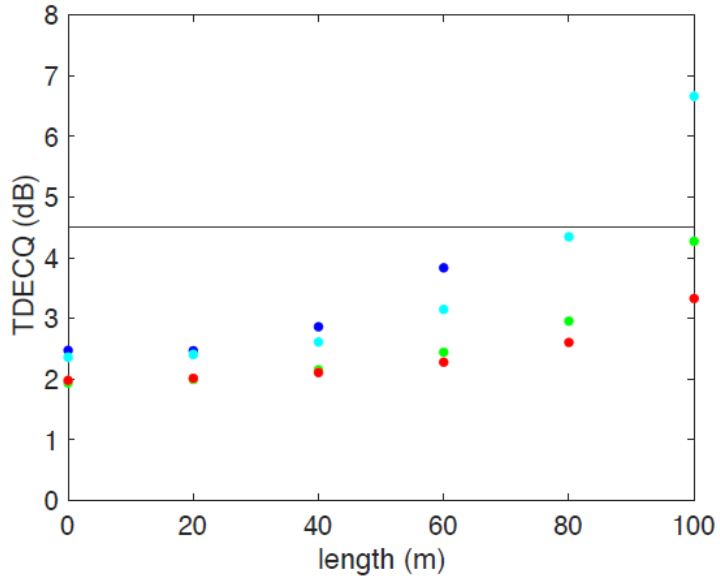
castro_3db_adhoc_01_040121.pdf

No significant difference in TDECQ between 7 and 9 taps for 50m reach.

TDECQ 4.5 dB

TDECQ 3.5 dB

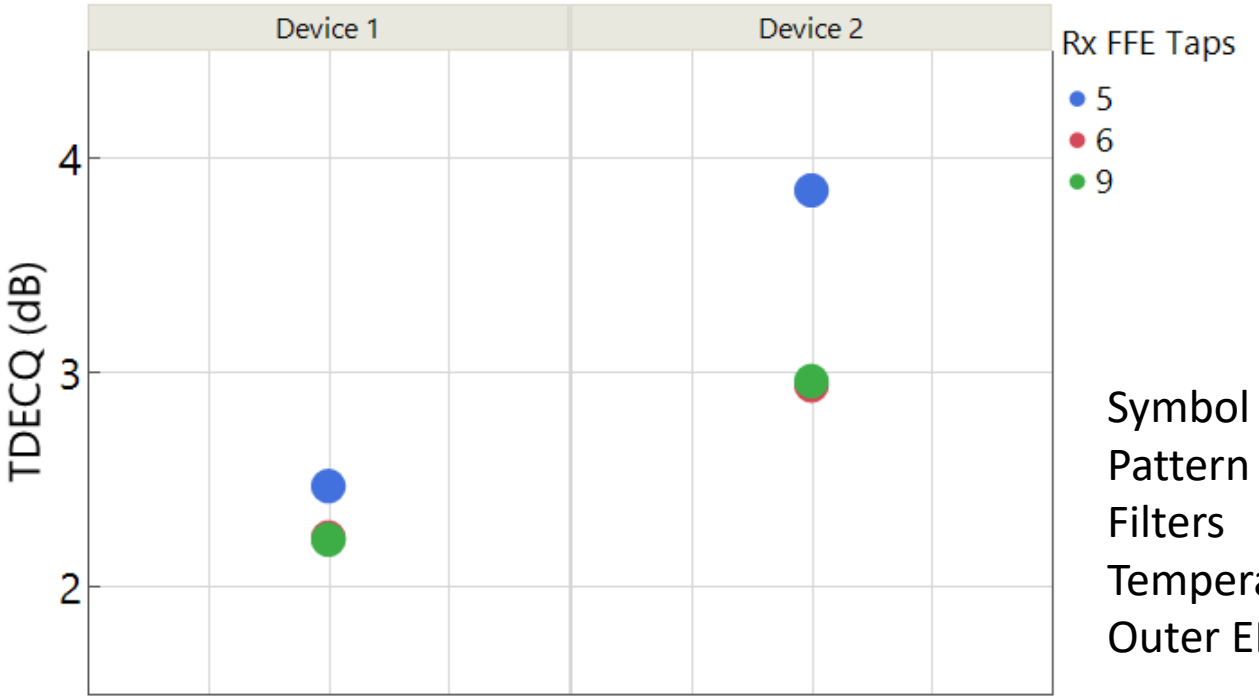
ingham_3db_adhoc_01a_062520.pdf



TDECQ versus OM4 link length for 5-tap Rx FFE (blue), 7-tap Rx FFE (cyan), 9-tap Rx FFE (green) and 23-tap Rx FFE (red)

If TDECQ is not measurable at a particular length, then a data point is not shown

850 nm Link – Measurements



Symbol rate	53.125 GBd
Pattern	SSPRQ
Filters	26.6 GHz (receiver) and 33.6 GHz (50m OM4)
Temperature	75°C
Outer ER	3 dB

- 6 taps on the reference equalizer appear sufficient for the 50m OM4 reach.
- Module manufacturers need margin on the max TDECQ.
  Max TDECQ could be reduced to 4 dB for the 50m reach.

Interoperability between SR and VR

Module interoperability is a challenge under the best of circumstances!

- If max TDECQ or definition of reference equalizer, or both, are different for SR and VR, then

  Interoperability tests for SR:

TECQ	Filter 26.6 GHz	Max TECQ = VR value	Reference equalizer = VR definition
TDECQ	Filter 26.6, 33.6 GHz	Max TDECQ = VR value	Reference equalizer = VR definition

  [assumes reference equalizer length is shorter and/or max TDECQ is smaller for VR compared to SR.]

All measurements can be performed with the capture of one waveform.

Interoperability between 850 and 940 nm Links

1. Photodiode (PD) must have good responsivity across the wavelength range [InGaAs PIN]
2. A wide band AR coating on the PD for not exceeding return loss spec (and maintain good responsivity)
3. Identical length of reference equalizer and max TDECQ

- #1 and #2 will be required for PDs used in both VR and SR links.
- PDs used in previous generation (50G) links were not required to meet #1 and #2.
  Backwards compatibility is not specified in multimode ethernet standards.

Examples of choices for VR

Potential choices for VR:

#	Center Wavelength [VCSEL]	Number of taps on reference equalizer	Max TDECQ (dB)
1	850 nm	9	4.4
2	850 nm	9	4
3	850 nm	6	4
4	850 nm + 940 nm	9	4.4
5	850 nm + 940 nm	9	4
6	850 nm + 940 nm	6	4

P802.3db Objectives

VR Cost and power optimized 100G multimode links [50m OM4]

SR Maximize reach of 100G multimode links [100m OM4]

CSD

P802.3db CSD

Broad Market Potential

A standards project authorized by IEEE 802 LMSC shall have a broad market potential. Specifically, it shall have the potential for:

a) Broad sets of applicability.
b) Multiple vendors and numerous users.

Technical Feasibility

Each proposed IEEE 802 LMSC standard shall provide evidence that a project is technically feasible within the time frame of the project. At a minimum, address the following items to demonstrate technical feasibility:

a) Demonstrated system feasibility.
b) Proven similar technology via testing, modeling, simulation, etc.
c) Confidence in reliability

Economic Feasibility

Each proposed IEEE 802 LMSC standard shall provide evidence of economic feasibility. Demonstrate, as far as can reasonably be estimated, the economic feasibility of the proposed project for its intended applications. Among the areas that may be addressed in the cost for performance analysis are the following:

a) Balanced costs (infrastructure versus attached stations).
b) Known cost factors.
c) Consideration of installation costs.
d) Consideration of operational costs (e.g., energy consumption).
e) Other areas, as appropriate.