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53 Gbaud VCSEL MMF System Measurements on Impact of Rx C2M Channel Loss in a Linear Interface

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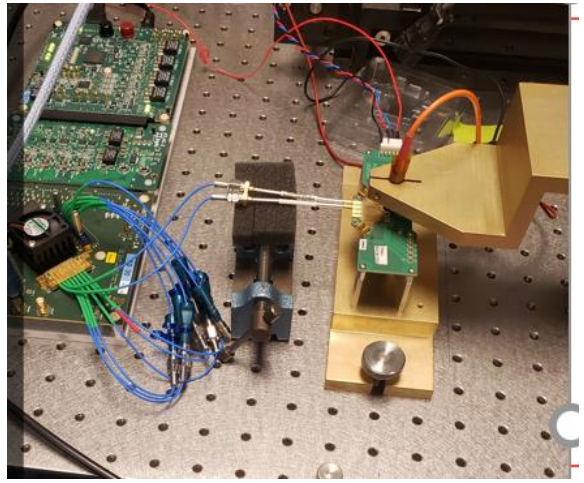
Introduction

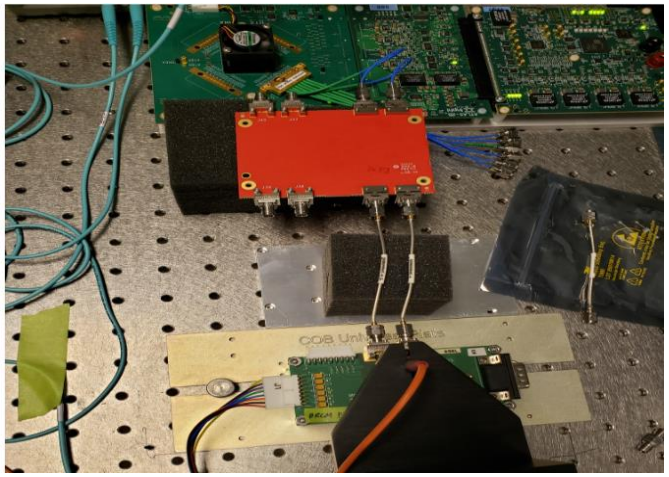
- A linear interface has been proposed in latchman_3db_adhoc_01_100120 and latchman_3db_adhoc_01_101520. However, there is lack of 53 Gbaud PAM4 end-to-end experimental data to demonstrate technical feasibility
- In this work, we present 53 Gbaud PAM4 end-to-end system measurements including both optical VCSEL/MMF channel, as well as electrical ISI channel to emulate the C2M loss at Rx
- Due to lack of availability of QSFP-DD/OSFP mated board, the measured Rx C2M channel is an ideal ISI channel
- The measurement results show even with an ideal Rx C2M channel, the system is not realizable due to severe error floor

53Gbaud VCSEL Experimental Setup

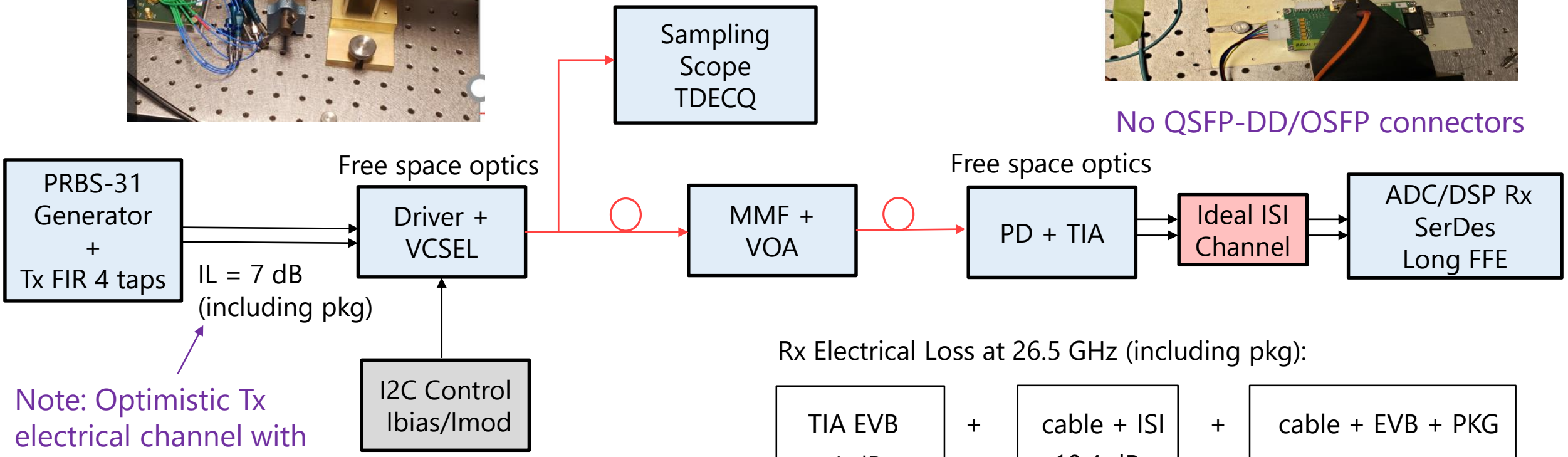
Tx



Rx with ISI Board



No QSFP-DD/OSFP connectors

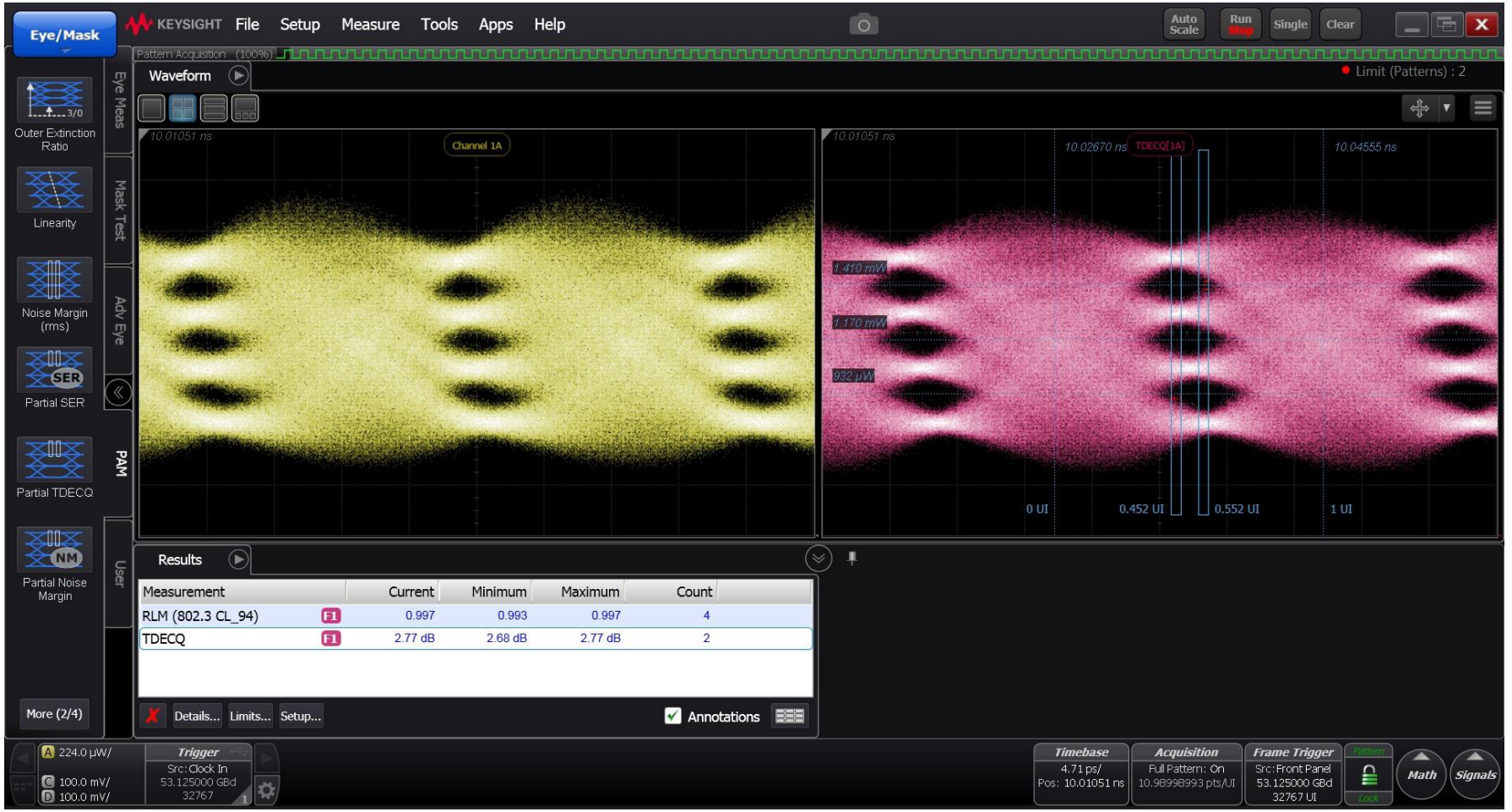


Note: Optimistic Tx electrical channel with low IL, no Xtalk, no large ASIC pkg, no noise penalty from a CTLE

Rx Electrical Loss at 26.5 GHz (including pkg):

TIA EVB	+	cable + ISI	+	cable + EVB + PKG
1 dB		10.4 dB		4.25 dB

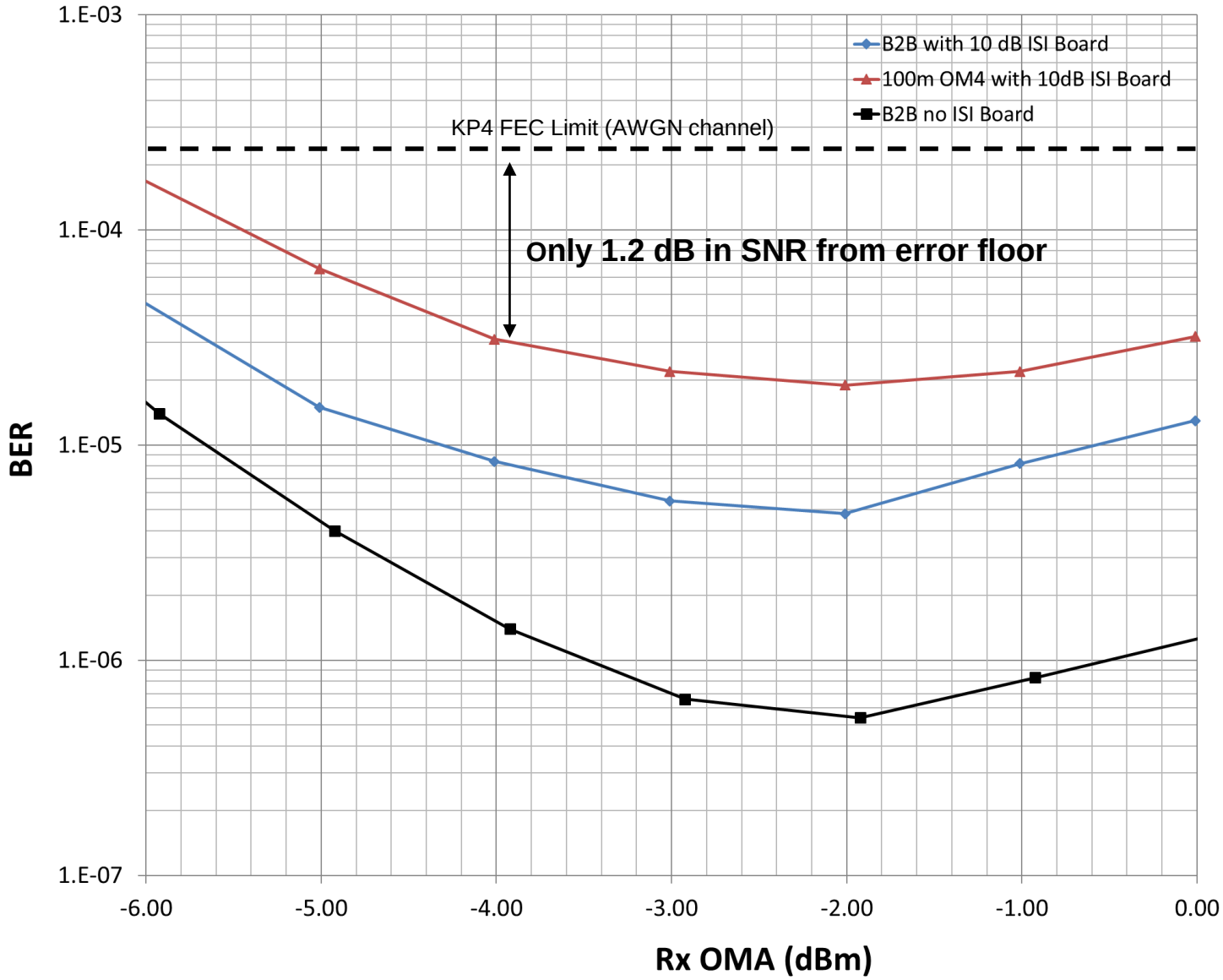
Tx TDECQ Measurement (5-tap FFE)



Measurement Results

Impairments not included in experiment:

- Realistic Tx C2M channel loss
- QSFP-DD/OSFP connector at Tx/Rx
- Electrical Xtalk
- PVT penalties (e.g. VCSEL measured at room temp.)
- Component aging



Conclusions

- 53 Gbaud PAM4 end-to-end system BER measurements show significant penalty for Rx electrical loss in a linear interface
- The data shows an error floor at BER = 3.e-5, with very little margin for expected additional system penalties due to Tx C2M channel, electrical Xtalk, electrical reflections, PVT corners, and device aging
- Future experiments will include a mated QSFP-DD/OSFP test board for more realistic C2M channel at both Tx and Rx