

# **In Support of Linear Interface: Updated Measurements / Simulations**

MACOM

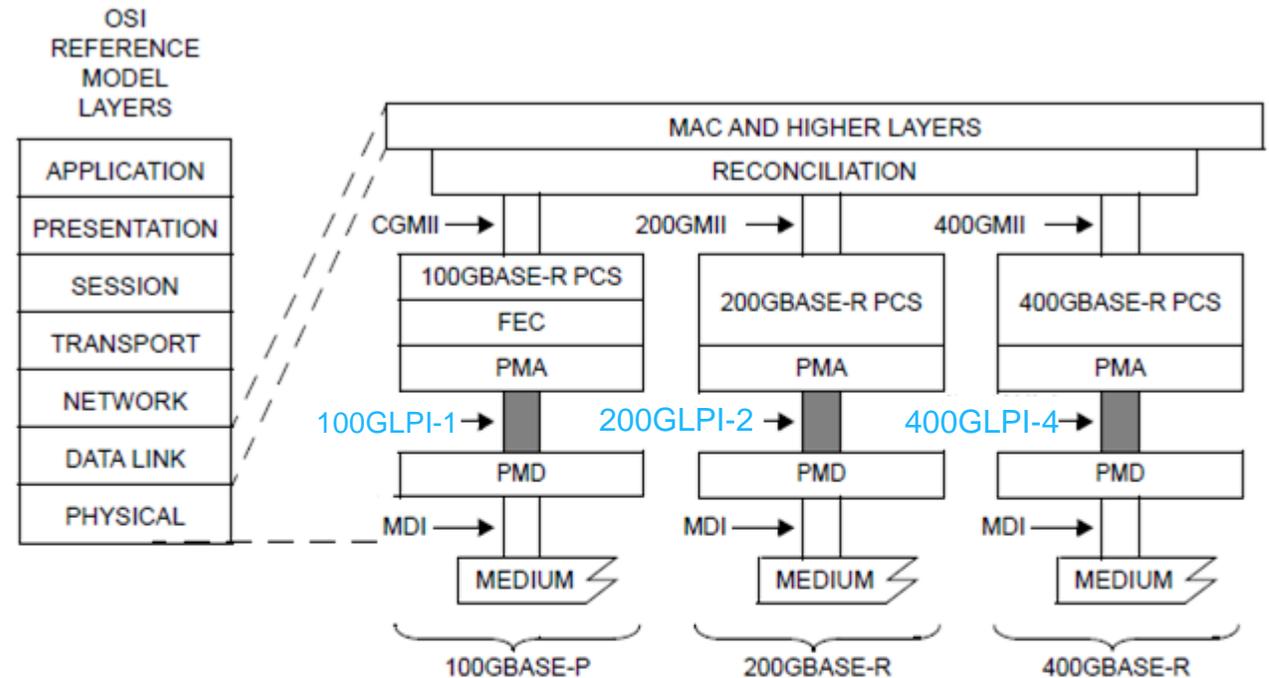
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IEEE P802.3db Ad Hoc Teleconference  
1 Oct 2020

- Introduction
- Rx Path Measured Results
  - Leveraging Electrical TDECQ with Trace Loss
  - Sensitivity results with 10dB Channel
- Tx Path simulations
- Conclusion

# LINEAR PHYSICAL INTERFACE (LPI)

- > LINEAR PHYSICAL INTERFACE (LPI) is an **optional PMD service interface for the PMDs in Clause 140, 151, and TBD**. It allows the construction of compact optical transceiver modules for SMF and MMF applications with no clock and data recovery / DSP circuits inside....
- > Figure TBD shows the relationship of the LPI interface with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model ...

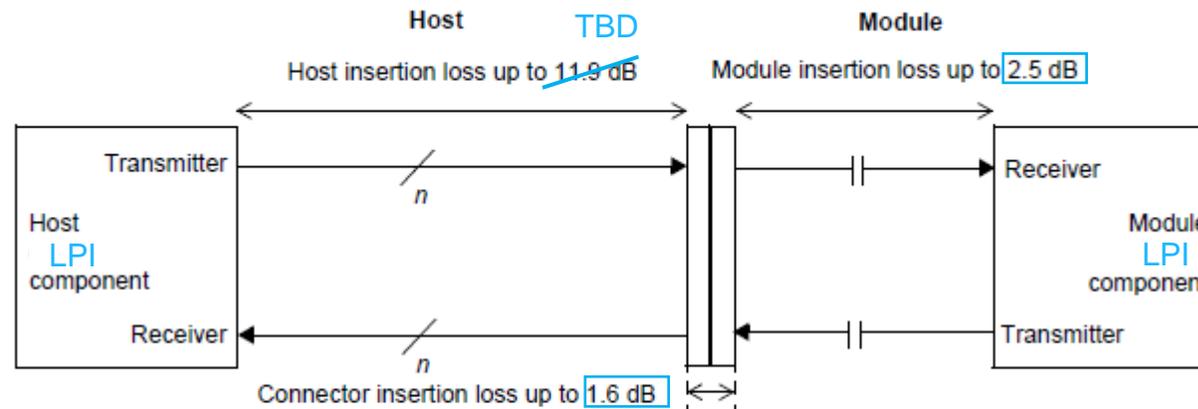


100GAUI-1 = 100 Gb/s ONE-LANE ATTACHMENT UNIT INTERFACE  
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE  
400GAUI-4 = 400 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE  
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE  
MAC = MEDIA ACCESS CONTROL  
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

200GAUI-2 = 200 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE  
FEC = FORWARD ERROR CORRECTION  
MDI = MEDIUM DEPENDENT INTERFACE  
PCS = PHYSICAL CODING SUBLAYER  
PMA = PHYSICAL MEDIUM ATTACHMENT  
PMD = PHYSICAL MEDIUM DEPENDENT

# Channel Insertion Loss Budget & Host LPI

- TBD target= 6.875dB including allowance for BGA and connector footprint vias= 100GBASE-CR
- Host LPI Component much more capable than equalizers used for Optical evaluation



Note—The number of lanes  $n$  is equal to 1 for 100GAUI-1, 2 for 200GAUI-2, and 4 for 400GAUI-4.

Modified

Figure 120G-2—~~100GAUI-1, 200GAUI-2, and 400GAUI-4 C2M~~ insertion loss budget at 26.56 GHz

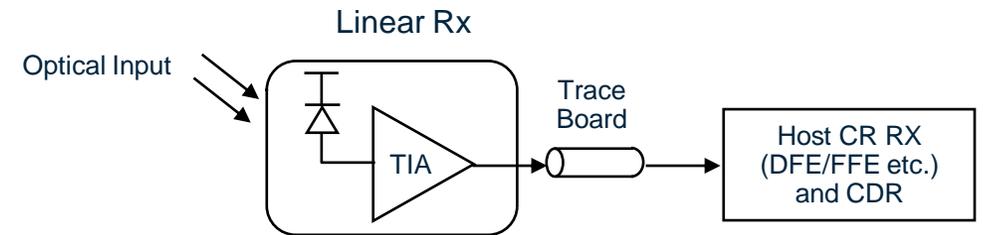
100GLPI-1

200GLPI-2

400GLPI-4

# 100G Linear Interface Rx Demonstration

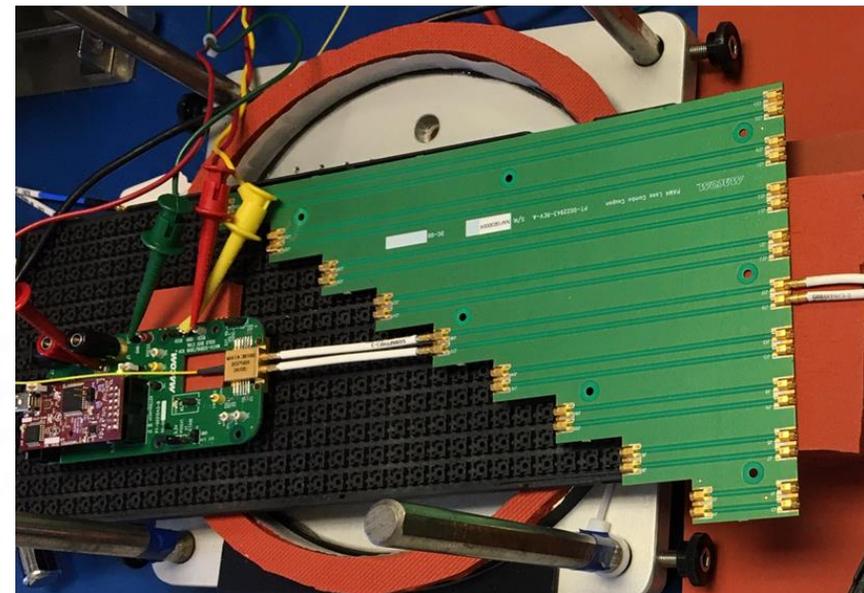
- Optical input: SMF input
- Rx Setup:
  - MACOM PD (BSP56B) and MACOM TIA (MATA-05817B)
  - Trace (emulate host loss)
  - Keysight Scope



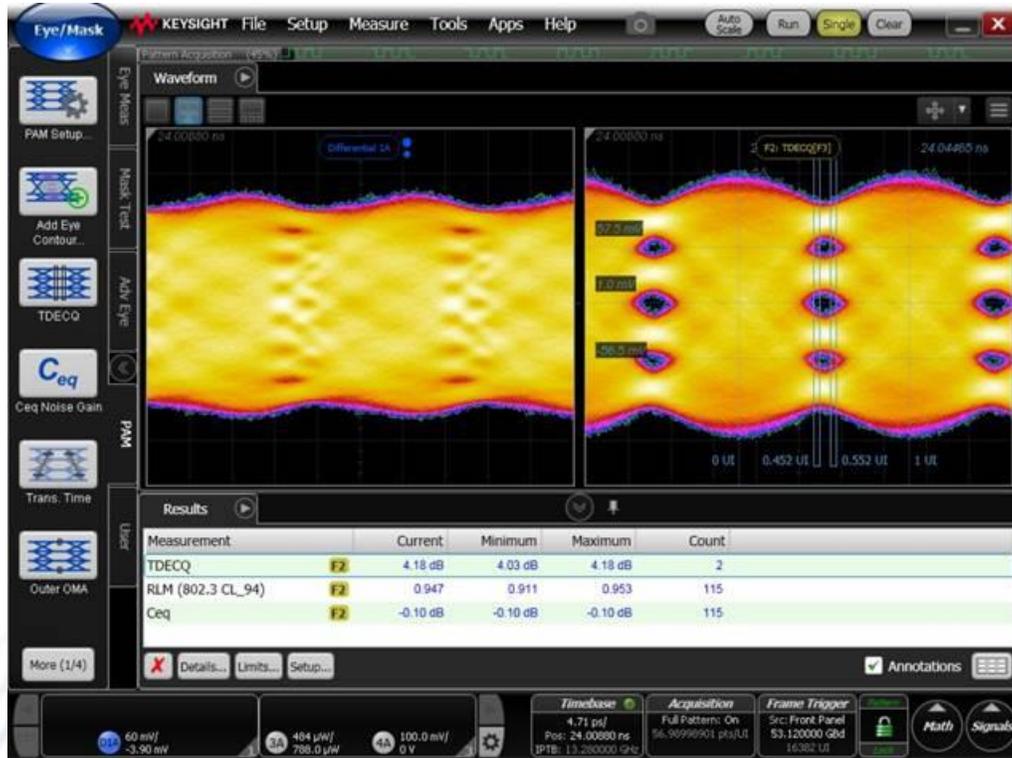
Optical Input



Linear Rx & Trace Board



# Optical Source -->MACOM PD/TIA --> Trace Loss Channel (10dB)--> DCA-X



TDECQ FFE Taps=5  
 Electrical TDECQ after trace = **4.18dB**

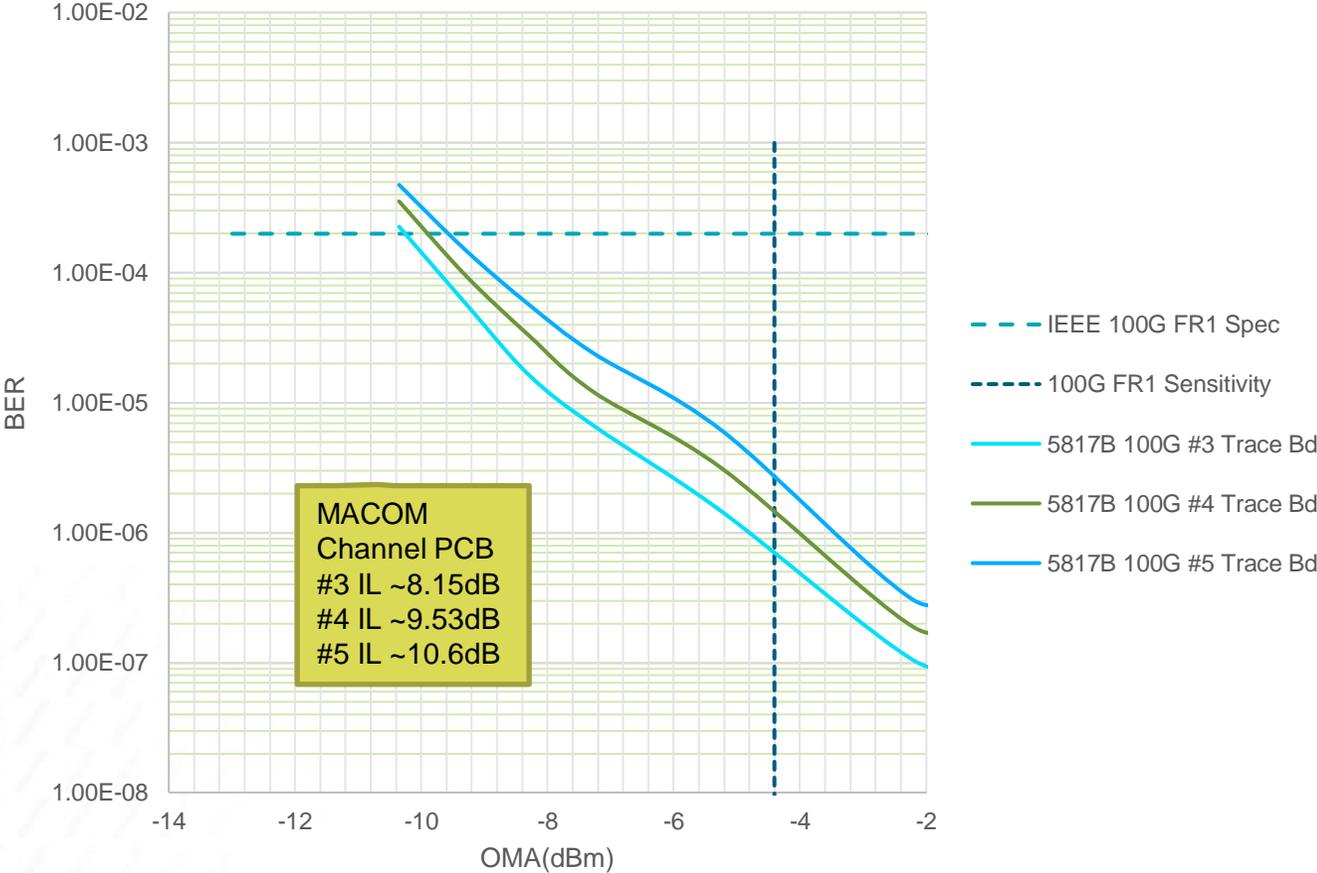
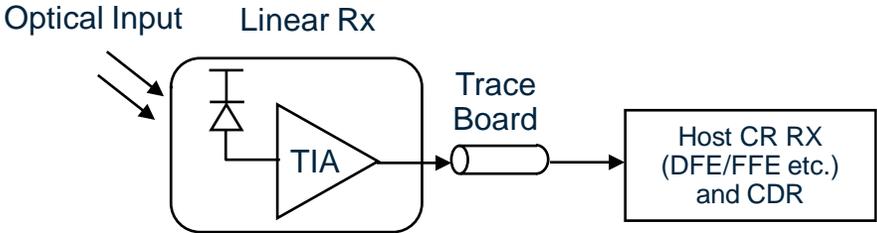


TDECQ FFE Taps=9  
 Electrical TDECQ after trace = **1.86dB**

# 100G Optical Source -->MACOM PD/TIA --> Trace Loss Channel--> BER Curve

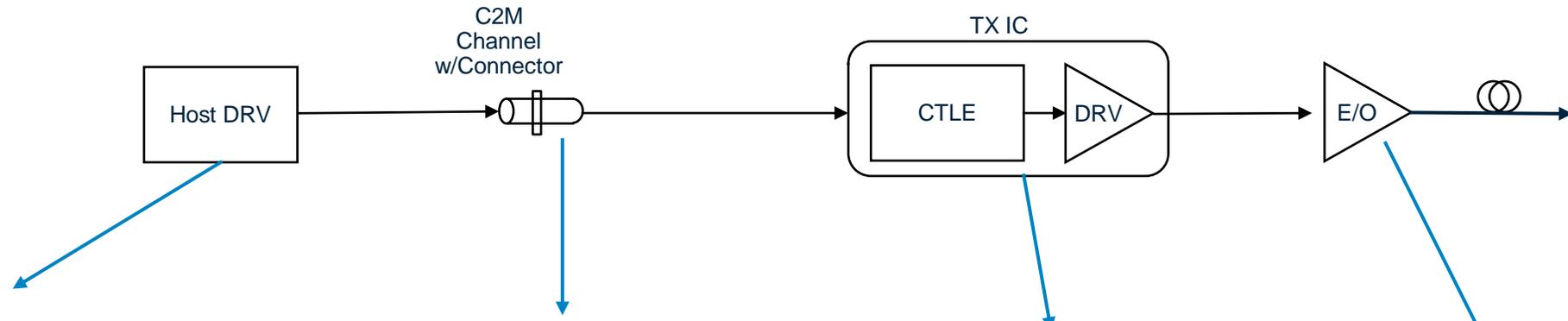


> BER curve measured with 15tap FFE in Rx



# VCSEL Simulations in the Tx

# Tx Path Simulation Model

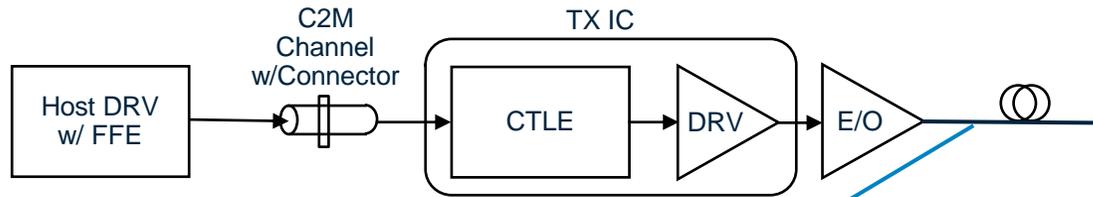


Parameter	Symbol	Value	Units
Device package model			
Single-ended device pad capacitance	$C_d$	$1.2 \times 10^{-4}$	nF
Single-ended device series inductance	$L_s$	0.12	nH
Single-ended device bump capacitance	$C_b$	$3 \times 10^{-5}$	nF
Transmission line length, Test 1	$z_p$	12	mm
Transmission line length, Tx Test 2	$z_p$	31	mm
Transmission line length, Rx Test 2	$z_p$	29	mm
Transmission line parameter, $a_1$	$a_1$	$9.909 \times 10^{-4}$	ns <sup>1/2</sup> /mm
Transmission line parameter, $a_2$	$a_2$	$2.772 \times 10^{-4}$	ns/mm
Single-ended package capacitance at package-to-board interface	$C_p$	$8.7 \times 10^{-5}$	nF
Transmission line characteristic impedance	$Z_c$	87.5	nF
Transmission line 2 length	$z_{p2}$	1.8	mm
Transmission line 2 characteristic impedance	$Z_{c2}$	92.5	$\Omega$

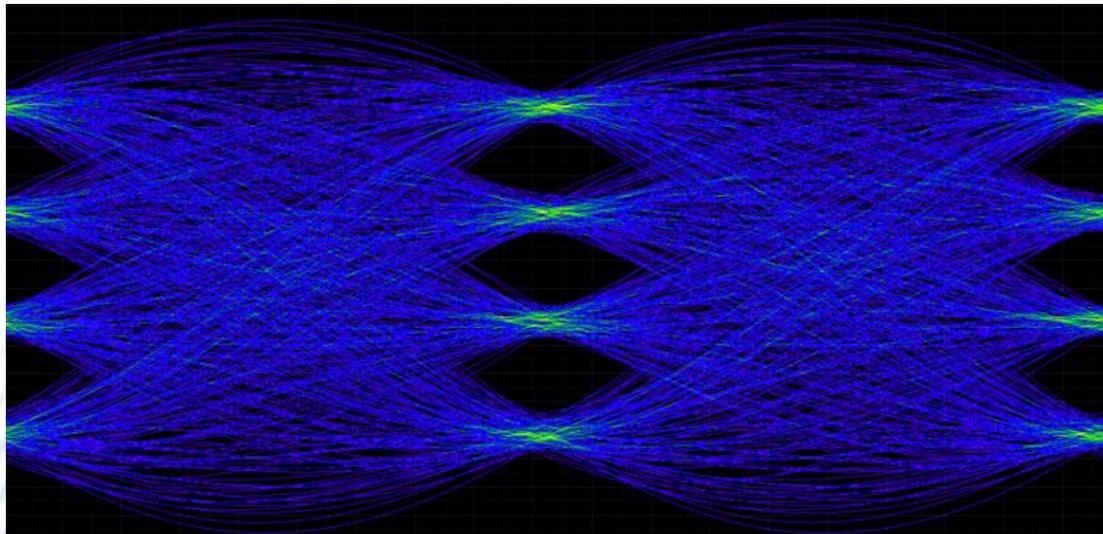
**802.3ck channel**  
 mellitz\_3ck\_01\_0518  
 \_C2M\9dB

**MACOM Tx IC**  
 CTLE + VCSEL  
 Driver

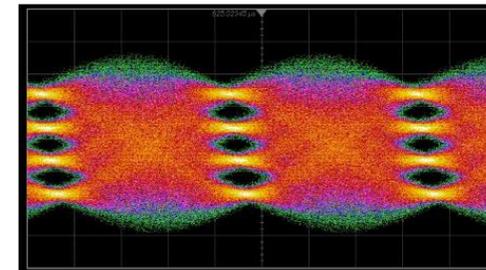
**VCSEL Model**  
 Bandwidth: 26GHz



Eye Diagram Before Fiber  
(with 9 tap FFE)



Eye diagram after 100 m OM4



TDECQ: 3.5 dB

Modulation format	PAM4
Symbol rate	53.125 GBd
Pattern	PRBS15Q
Tx FFE	3-tap T-spaced
SER target for TDECQ	$4.8 \times 10^{-4}$
DCA optical plug-in bandwidth	34 GHz
DCA SIRC bandwidth	38.3 GHz
DCA BT filter bandwidth	26.6 GHz
DCA FFE	9-tap T-spaced
Temperature	75 °C
Center wavelength	863 nm
RMS spectral width	0.42 nm
Outer ER	3 dB

- 100 m OM4 link: TDECQ within 4.5 dB with a 9-tap Rx FFE

Reference: ingham\_3db\_adhoc\_01a\_062520

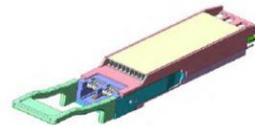
- > Linear interface is demonstrated to be feasible via measurements and simulations
- > Volume adoption at 100G per  $\lambda$  requires improved economics (relative cost and power)
  - Linear architecture as potential to enable volume ramp and save 10s of MILLIONS watts / year

## Quantifying Power Consumption at 100G/lane

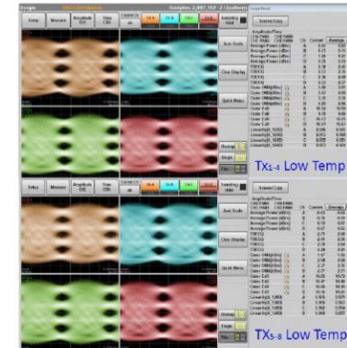


- > 8 x 100G/lane SMF module with DSP inside: **17W-18W**
- > 8 x 25G/lane (e.g. two QSFP28) SMF Module: **7W max**
  - QSFP28: Low power, low cost
  - 40G QSFP (4x10G): similar power consumption to QSFP28

### Example: 800 Gb/s OSFP Capacity Module



- ❖ OSFP Form Factor
- ❖ 8x100G DR8+ 2km with MPO-16 and 2x400G FR4 with CS connector
- ❖ OIF CEI-112G-VSR interface
- ❖ PMD spec follows 400G DR4+ and FR4, interoperable with 400G
- ❖ 0~70degC 18W, 10~60C 17W
- ❖ 7nm DSP inside



Source – Tedros Tsegaye, Innolight