

# 200G PAM4 per Lane C2M Channel Technical Feasibility

Rick Rabinovich  
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# 200G PAM4 C2M Technical Feasibility

## Contributors and Supporters

### Contributors:

- Richard Mellitz (SAMTEC)
- Brandon Gore (SAMTEC)

### Supporters:

- Sam Kocsis (Amphenol)
- Ali Hammoodi (Amphenol)
- Adee Ran (Cisco)
- Ali Ghiasi (Ghiasi-Quantum LLC)
- Howard Heck (Intel)
- Phil Sun (Credo)
- Bill Simms (NVIDIA)
- John Calvin (Keysight Technologies)

# 200G PAM4 C2M Technical Feasibility

## Objectives

- Determine the C2M Channel Technical Feasibility Using COM
- The purpose of this presentation is NOT to offer “the” solution
- The intention is to OPEN the conversation and identify the variables that will need to be adjusted to arrive at a solution
- It will be shown that incremental changes to the .ck project parameters may not be enough and that a more thorough alternative will be necessary.
  - ❖ COMPREHENSIVE rather than INCREMENTAL solution

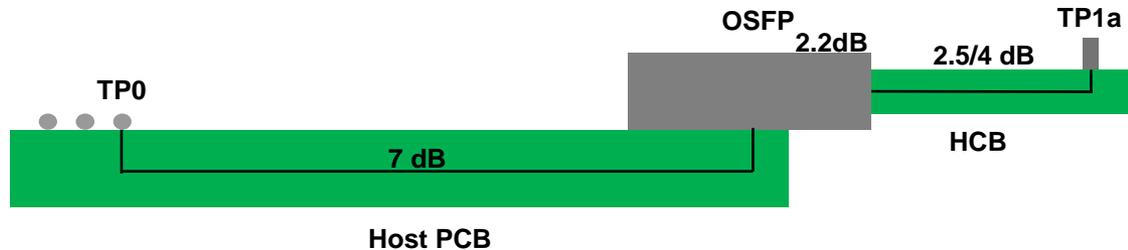
# 200G PAM4 C2M Technical Feasibility

## C2M Channel Highlights

- Traditional Topology, i.e., medium PCB material between ASIC and Connector
  - ❖ Short Channel - Ex. NIC card
- Short Host Channel – IL ~ 7 dB @ Nyquist
- Channel with **IMPAIRMENTS**
  - ❖ ASIC/Connector vias/Insert module finger transition
  - ❖ Layout Turns
  - ❖ Skew Compensation
  - ❖ Full Channel Crosstalk
- MDI is an OSFP Connector
- Assume ASIC Parallel Fan-Out
- Two HCB losses 2.5 dB and 4.0 dB @ Nyquist
- COM rev. 3.4

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## Structure View & Insertion Losses



- Vias = 40 mil long
- Blind Vias
- Frequency Sweep Range = 10 MHz to 120 GHz

IL @ Nyquist (53.125 GHz)

IL<sub>HCB</sub> = 2.5 dB

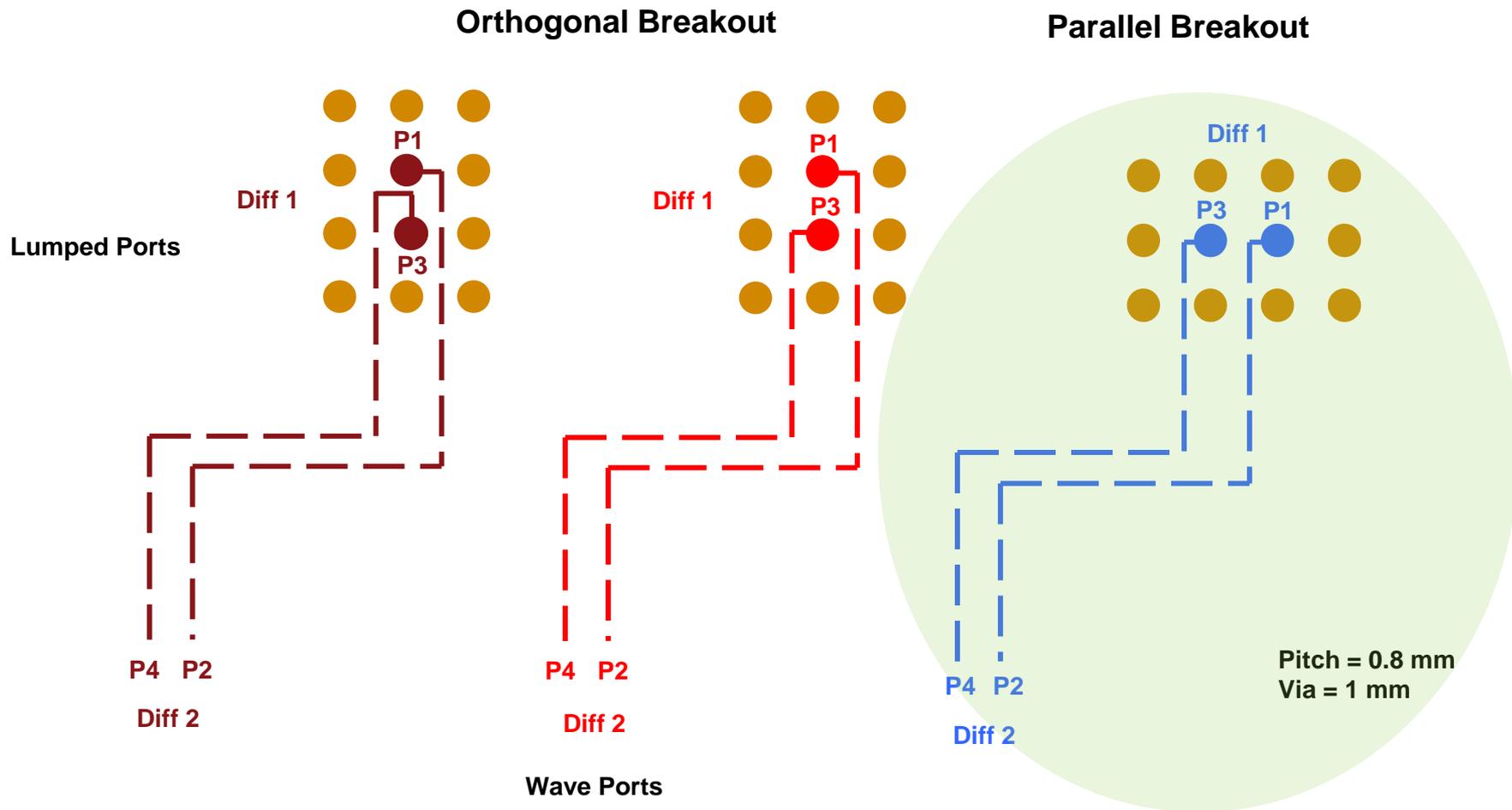
- IL<sub>PCB</sub> = 7 dB
- IL<sub>Conn</sub> = 2.2 dB
- IL<sub>HCB</sub> = 2.5 dB
- IL<sub>C2M</sub> = 11.4 dB

IL<sub>HCB</sub> = 4 dB

- IL<sub>PCB</sub> = 7 dB
- IL<sub>Conn</sub> = 2.2 dB
- IL<sub>HCB</sub> = 4 dB
- IL<sub>C2M</sub> = 12.9 dB

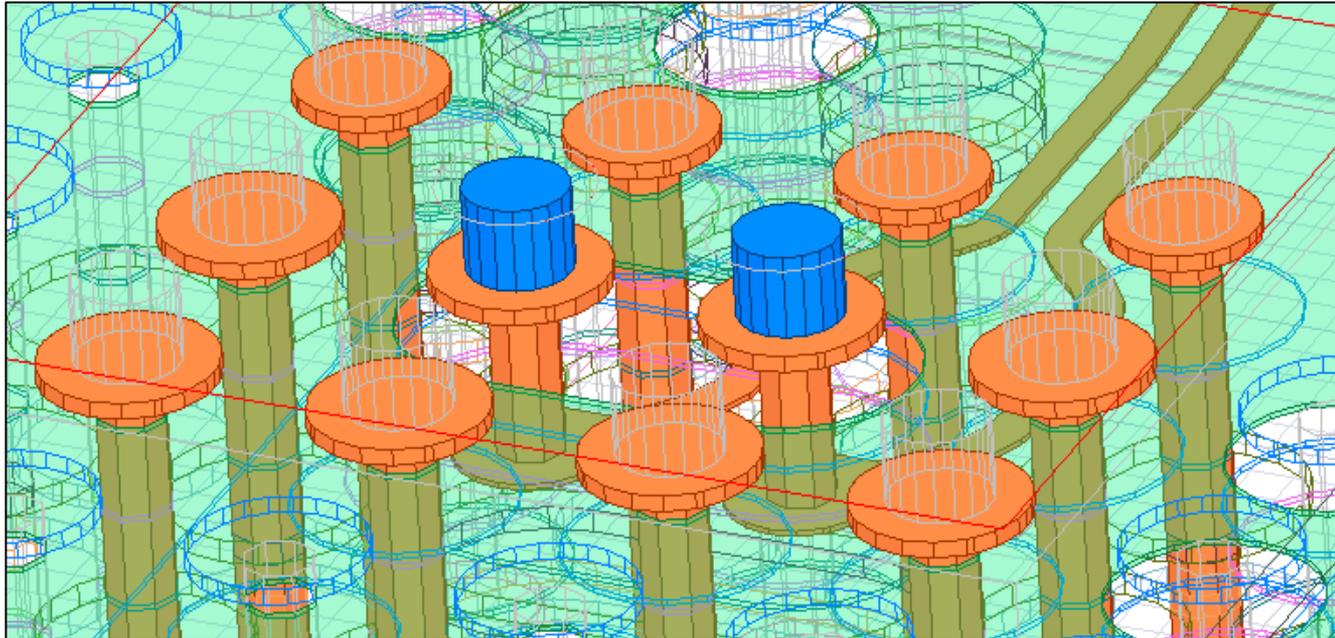
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## Orthogonal vs. Parallel Fanouts



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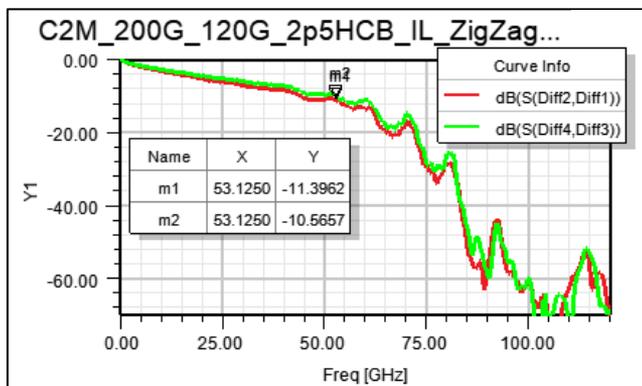
## ASIC Ball Model Example



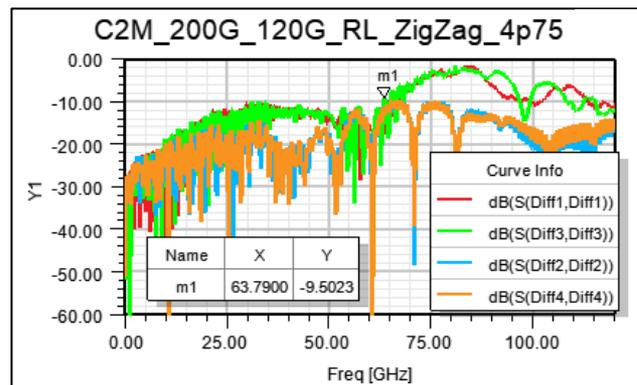
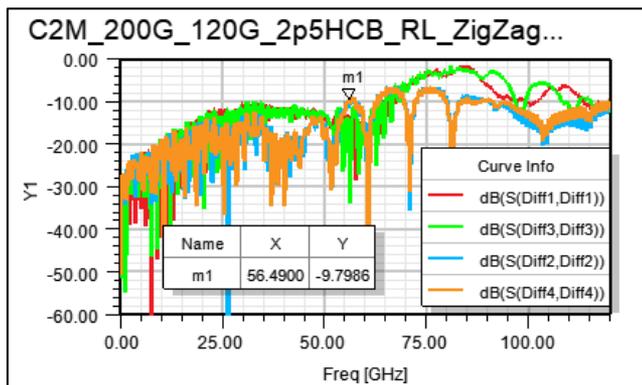
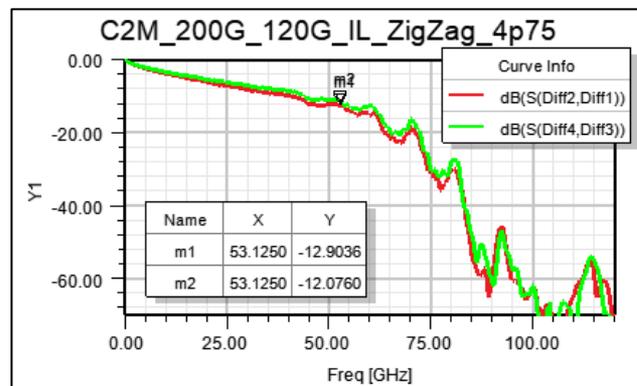
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## IL/RL Performance

$IL_{HCB} = 2.5 \text{ dB}$



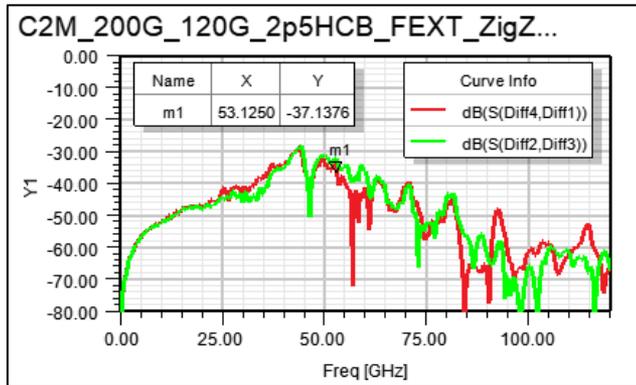
$IL_{HCB} = 4 \text{ dB}$



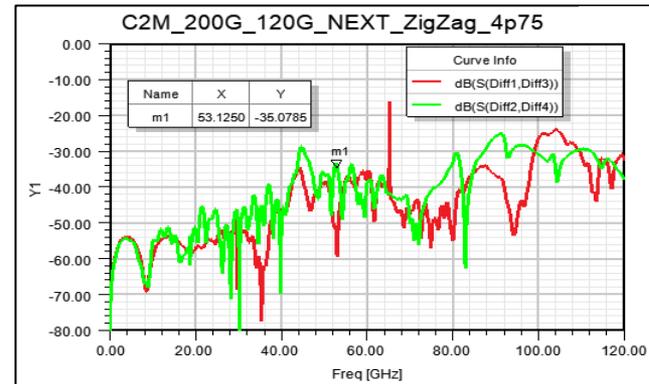
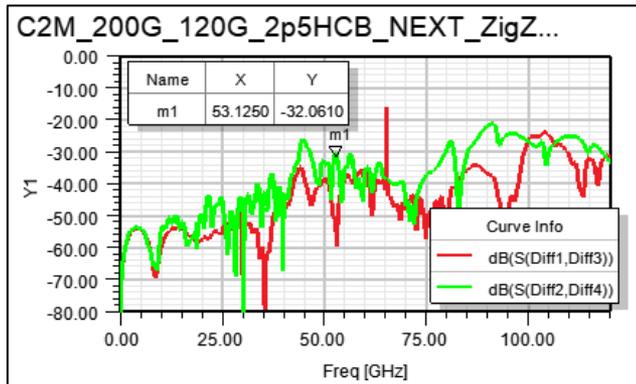
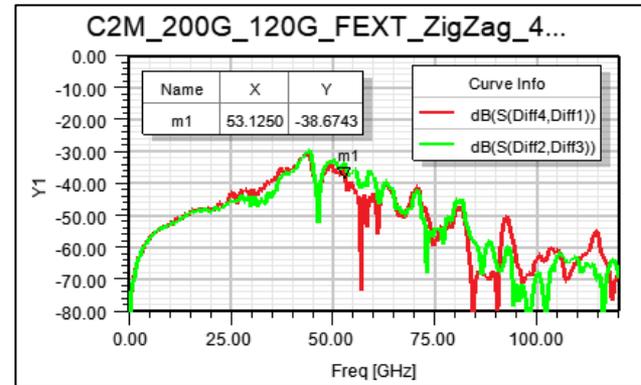
# 200G PAM4 C2M Technical Feasibility

## FEXT/NEXT Performance

$IL_{HCB} = 2.5 \text{ dB}$



$IL_{HCB} = 4 \text{ dB}$



# 200G PAM4 C2M Technical Feasibility

## COM Results – “Incremental” Changes

	P802.3.ck	P802.3df
f_b	53.125	106
C_d	[1.2e-4 0]	[0.7e-4 , 0]
L_s	[0.12 0]	[0.1,0]
C_b	[0.3e-4 0]	[0.23e-4 0]
N_b	4	9
eta_0	4.10E-08	4.10E-09
SNR_TX	32.5	33
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	[0 0.000644085 0.00018018]
package_tl_tau	6.141E-03	0.0057
package_Z_c	[87.5 87.5 ; 92.5 92.5 ]	[87.5 87.5 ; 92.5 92.5 ]

$IL_{HCB} = 2.5 \text{ dB}$

: Case 1: z\_p=(15:1.8, 0:0, 0:0, 15:1.8) (TX, RX, NEXT, FEXT):  
: EH = 6.170 mV (FAIL)  
: VEC = 18.041 dB (FAIL)  
: FAIL ... ERL = 9.712 dB (NaN dB, 9.712 dB)  
: Case 2: z\_p=(31:1.8, 0:0, 0:0, 31:1.8) (TX, RX, NEXT, FEXT):  
: EH = 6.880 mV (FAIL)  
: VEC = 14.833 dB (FAIL)  
: FAIL ... ERL = 9.712 dB (NaN dB, 9.712 dB)

OK

1 FEXT

$IL_{HCB} = 4 \text{ dB}$

: Case 1: z\_p=(15:1.8, 0:0, 0:0, 15:1.8) (TX, RX, NEXT, FEXT):  
: EH = 6.060 mV (FAIL)  
: VEC = 16.963 dB (FAIL)  
: PASS ... ERL = 11.818 dB (NaN dB, 11.818 dB)  
: Case 2: z\_p=(31:1.8, 0:0, 0:0, 31:1.8) (TX, RX, NEXT, FEXT):  
: EH = 5.940 mV (FAIL)  
: VEC = 14.083 dB (FAIL)  
: PASS ... ERL = 11.818 dB (NaN dB, 11.818 dB)

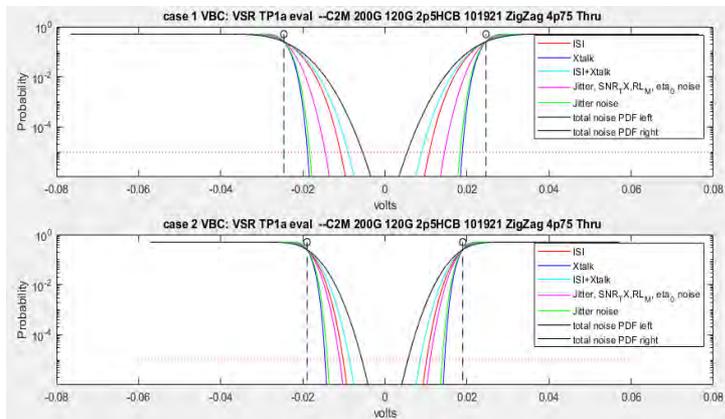
OK

No FEXT

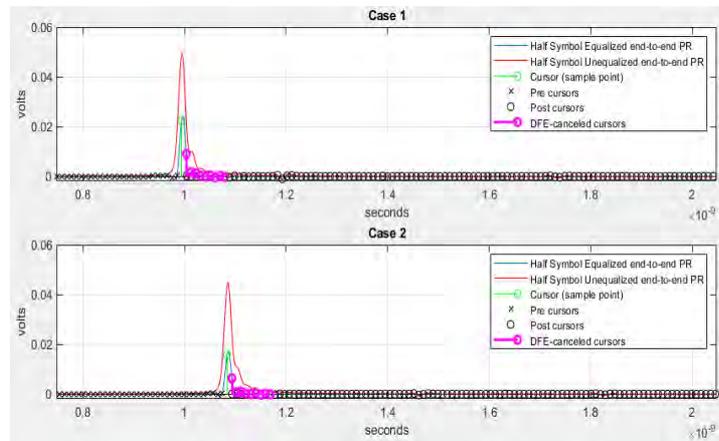
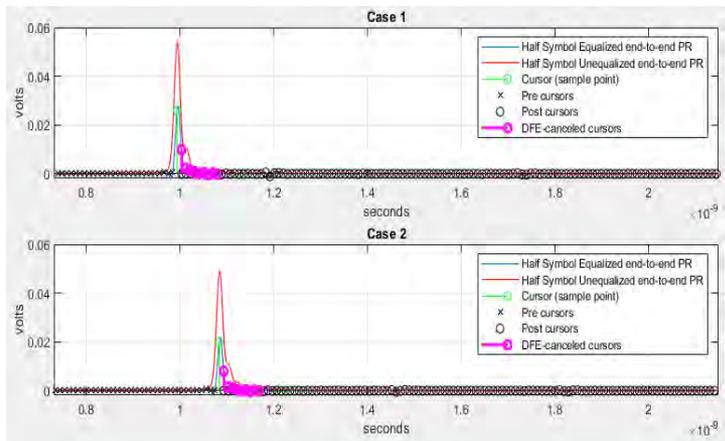
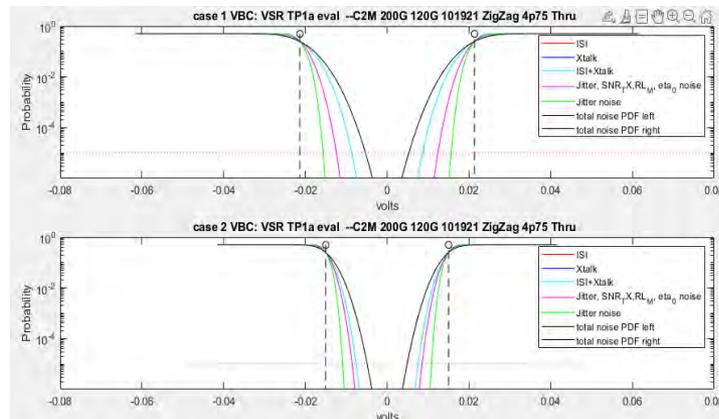
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## Bathtub and Pulse Response – Incremental Changes

$IL_{HCB} = 2.5 \text{ dB}$



$IL_{HCB} = 4 \text{ dB}$



# 200G PAM4 C2M Technical Feasibility

## COM Results – Comprehensive Changes

**IL<sub>HCB</sub> = 2.5 dB**

```
COM r3.40 results
: Case 1: z_p=(15:1.8, 0:0, 0:0, 15:1.8) (TX, RX, NEXT, FEXT):
: EH = 17.710 mV (pass)
: VEC = 10.802 dB (pass)
: PASS ... ERL = 11.993 dB (NaN dB, 11.993 dB)
: Case 2: z_p=(31:1.8, 0:0, 0:0, 31:1.8) (TX, RX, NEXT, FEXT):
: EH = 16.130 mV (pass)
: VEC = 10.734 dB (pass)
: PASS ... ERL = 11.993 dB (NaN dB, 11.993 dB)
```

4 FEXTs

**IL<sub>HCB</sub> = 4 dB**

```
COM r3.40 results
: Case 1: z_p=(15:1.8, 0:0, 0:0, 15:1.8) (TX, RX, NEXT, FEXT):
: EH = 13.760 mV (pass)
: VEC = 11.672 dB (pass)
: PASS ... ERL = 14.213 dB (NaN dB, 14.213 dB)
: Case 2: z_p=(31:1.8, 0:0, 0:0, 31:1.8) (TX, RX, NEXT, FEXT):
: EH = 11.450 mV (pass)
: VEC = 11.765 dB (pass)
: PASS ... ERL = 14.213 dB (NaN dB, 14.213 dB)
```

4 FEXTs

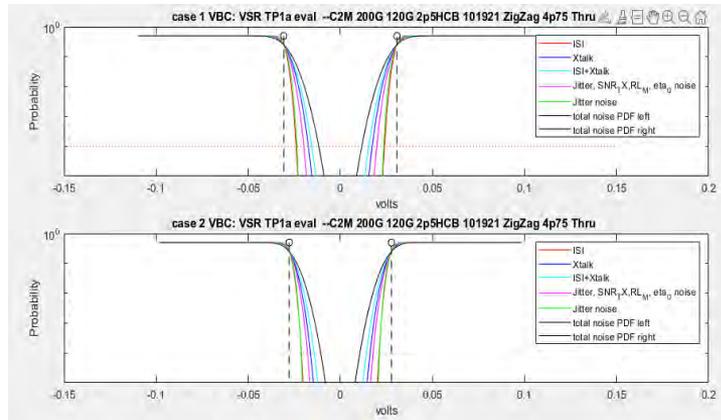
	P802.3.ck	Incremental P802.3df	Comprehensive P802.3df
f_b	53.125	106	106
C_d	[1.2e-4 0]	[0.7e-4, 0]	[0.7e-4, 0]
L_s	[0.12 0]	[0.1, 0]	[0.1, 0]
C_b	[0.3e-4 0]	[0.23e-4 0]	[0.23e-4 0]
N_b	4	9	9
eta_0	4.10E-08	4.10E-09	4.10E-09
SNR_TX	32.5	33	33
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	[0 0.000644085 0.00018018]	[0 0.000644085 0.00018018]
package_tl_tau	6.141E-03	0.0057	0.0057
package_Z_c	[87.5 87.5 ; 92.5 92.5 ]	[87.5 87.5 ; 92.5 92.5 ]	[87.5 87.5 ; 92.5 92.5 ]
b_max(1)	0.4	0.4	0.85
DER_0	1.00E-05	1.00E-05	1.00E-04
N_bg	0	0	3
N_bf	3	3	3
N_f	40	40	40
C_p	[0.87e-4 0]	[0.87e-4 0]	[0 0]*

\* Note: C\_p already included in simulation model

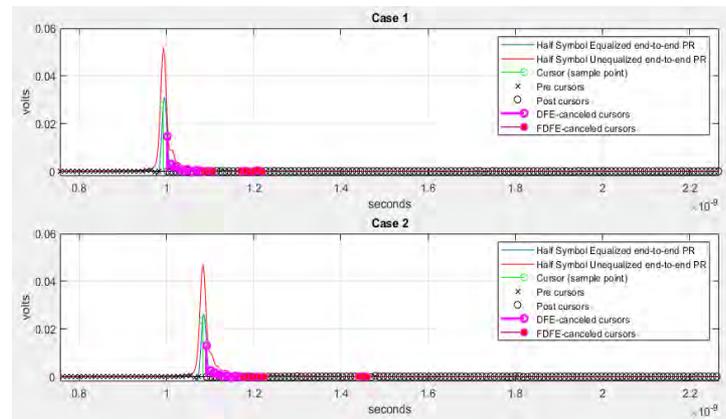
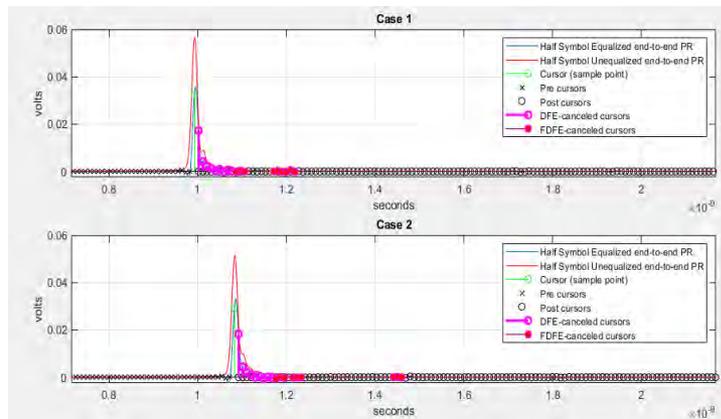
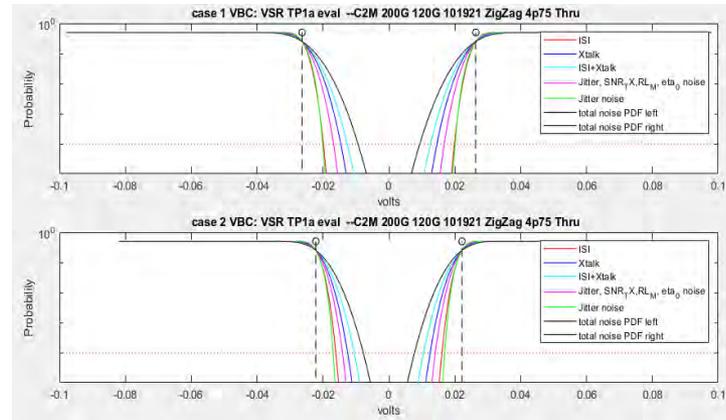
# 200G PAM4 C2M Technical Feasibility

## Bathtub and Pulse Response – Comprehensive Changes

$IL_{HCB} = 2.5 \text{ dB}$



$IL_{HCB} = 4 \text{ dB}$



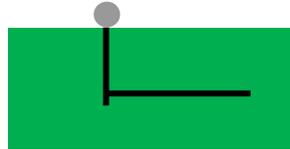
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## Nemesis – Channel Transitions

### Vias and Stubs

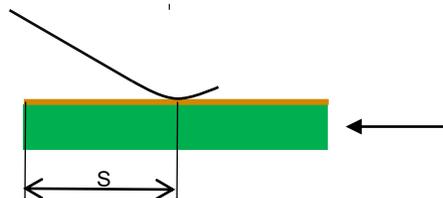
#### 1. ASIC to PCB and PCB to Connector

- Are we reaching the end of life for transition vias?
  - Although blind vias was is used in this study



#### 2. Paddle board finger to connector spring

- Are we reaching the end of life for paddle board finger connectivity?



Comments?

# 200G PAM4 C2M Technical Feasibility

## Summary

**“Equal Distribution of *PAIN*” to make C2M a viable interface:**

- 1. Need to improve transition technology at both ends of connectors and ASIC**
  - Other media rather than PCB, i.e., co-package, pigtail connector, etc.
  - Improve connector performance
- 2. Stronger FEC , i.e.,**
  - DER\_0 to be 1e-4 (one order of magnitude better than it is today)
  - Segmented FEC (?)
- 3. Stronger Equalization at Tx and Rx, i.e.,**
  - Enable three groups of three floating taps (similar to .ck backplane)
  - $b_{\max}(1) = 0.85$  and as an example of strong equalization for this specific channel
- 4. Reduce Intrinsic Chip Noise by one order of magnitude (from 4.10e-08 to 4.10e-09)**
- 5.  $IL_{\text{HCB}}$  range 2.5 dB to 4 dB**
- 6. Improve Interpretation of some COM parameters**
  - $C_p = 0$  to avoid double capacitive counting if model already includes ball elements
    - Ex.: Lumped ports already include the equivalent to solder balls

# Q & A

# Additional Data

# 200G PAM4 C2M Technical Feasibility

## Working Spreadsheet

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
Table 93A-1 parameters						I/O control			Table 93A-3 parameters				Floating Tap Control			
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter (ms)	Setting	Units		N_bg	3	0 1 2 or 3 groups	
f_b	106.00	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	0.000644085 0.00018018			N_bf	3	taps per group	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	0.0057	ns/mm		N_f	40	span for floating taps	
Delta_f	0.01	GHz			RESULT_DIR	\results\200GEL_VSR_host_TP1			package_Z_c	[87.5 87.5 ; 92.5 92.5 ]	Ohm		bmaxg	0.2	E value for floating taps	
C_d	[0.7e-4, 0]	nF	[TX RX]		SAVE_FIGURES	0	logical		ICN & FOM_ILD parameters							
L_s	[0.1, 0]	nH	[TX RX]		Port Order	[ 1 2 3 4 ]			f_v	0.469	*Fb		for TP4-->	[1.2e-4 0]	nF	[TX RX]
C_b	[0.23e-4 0]	nF	[TX RX]		RUNTAG	VSR_TP1a_eval_			f_f	0.469	Hz f_r specified in first column			[0.12 0]	nH	[TX RX]
z_p select	[1 2]		(test cases to run)		COM_CONTRIBUTION	0	logical		f_n	0.469	GHz			[0.3e-4 0]	nF	[TX RX]
z_p (TX)	[15 31; 1.8 1.8]	mm	(test cases)		Local Search	2			f_2	79.5	GHz			[1 2 3]		(test cases to run)
z_p (NEXT)	[0 0; 0 0]	mm	(test cases)		Operational				A_ft	0.450	V			[2 7 8]	mm	(test cases)
z_p (FEXT)	[15 31; 1.8 1.8]	mm	(test cases)		VEC Pass threshold	12	db		A_nt	0.450	V			[0 0 0]	mm	(test cases)
z_p (RX)	[0 0; 0 0]	mm	(test cases)		EH_min	10	mV							[2 7 8]	mm	(test cases)
C_p	[0 0]	nF	[TX RX]		ERL Pass threshold	10	dB							[0 0 0]	mm	(test cases)
R_d	50	Ohm			Min_VEO_Test	8	mV		Histogram_Window_Weight	gaussian	rectangle, gaussian, dual_rayleigh, triangle			[0 0.87e-4]	nF	[TX RX]
R_d	[50, 50]	Ohm	[TX RX]		DER_0	1.00E-04			QL	2.5						
A_v	0.415	V			T_r	3.25E-03	ns									
A_fe	0.415	V			FORCE_TR	1	logical									
A_ne	0.45	V			PMD_type	C2M										
L	4				BREAD_CRUMBS	0	logical									
M	32	Samp/UI			SAVE_CONFIGZMAT	1	logical									
samples_for_C2M	100	Samp/UI			PLOT_CM	0	logical									
T_O	50	mUI			TDR and ERL options											
AC_CM_RMS	0	V	(test cases)	0.0235 0.0256	TDR	1	logical									
filter and Eq					ERL	1	logical									
f_r	0.75	*fb			ERL_ONLY	0	logical		Table 92-12 parameters							
c(0)	0.65		min		TR_TDR	0.005	ns		Parameter	Setting						
c(-1)	[-0.2; 0.02; 0]		(min;step;max)		N	800			board_tl_gamma0_a1_a2	0.000567732 2.90358e-05	1.3 db/in at 56GHz					
c(-2)	[0.02; 0.1]		(min;step;max)		beta_x	0			board_tl_tau	0.0058	ns/mm					
c(-3)	[0]		(min;step;max)		rho_x	0.618			board_Z_c	100	Ohm					
c(1)	[-0.1; 0.02; 0]		(min;step;max)		fixture delay time	[0 0]	port1 port2		z_bp (TX)	130	mm					
N_b	9	UI			TDR_W_TXPKG	1			z_bp (NEXT)	0	mm					
b_max(1)	0.85		As/dffe1		N_bx	0	UI		z_bp (FEXT)	0	mm					
b_max(2..N_b)	0.15 0.15 0.1 0.1 0.1 0.1 0.1		As/dfe2..N_b		Tukey_Window	1			z_bp (RX)	0	mm					
b_min(1)	0		As/dffe1		Receiver testing				C_0	0	nF					
b_min(2..N_b)	0.1 -0.05 -0.05 -0.05 -0.05 -0.05		As/dfe2..N_b		RX_CALIBRATION	0	logical		C_1	0	nF					
g_DC	[-13; -1; 0]	dB	(min;step;max)		Sigma BBN step	5.00E-03	V		include PCB	0	logical					
f_z	42.4	GHz			Noise, jitter											
f_p1	42.4	GHz			sigma_RJ	0.01	UI									
f_p2	106	GHz			A_DD	0.02	UI									
g_DC_HP	[-3.5; 0.5; 0]	dB	(min;step;max)		eta_0	4.10E-09	V^2/GHz									
f_HP_PZ	2.65	GHz			SNR_TX	33	dB									
					R_LM	0.95										
					Impulse response tr	0.0001										

# 200G PAM4 C2M Technical Feasibility

## Channel Contribution

- rabinovich\_3df\_with\_impairments\_01\_022422.zip
  - ❖ KEY\_C2M\_200G\_120G\_2p5HCB\_022422\_FEXT.s4p
  - ❖ KEY\_C2M\_200G\_120G\_2p5HCB\_022422\_NEXT.s4p
  - ❖ KEY\_C2M\_200G\_120G\_2p5HCB\_022422\_Thru.s4p
  - ❖ KEY\_C2M\_200G\_120G\_4p0HCB\_022422\_FEXT.s4p
  - ❖ KEY\_C2M\_200G\_120G\_4p0HCB\_022422\_NEXT.s4p
  - ❖ KEY\_C2M\_200G\_120G\_4p0HCB\_022422\_Thru.s4p
  - ❖ C2M\_212G\_P802p3bj\_PAM4\_022422.xls