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# **802.3df**

## **considerations for insertion loss**

### **specifications:**

#### **MTF, Host, and Cable assembly**

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# Purpose

- Considerations for insertion loss specifications for MTF, Host, and Cable assembly
- Follow-on to MTF insertion loss considerations;  
[https://www.ieee802.org/3/df/public/adhoc/electrical/22\\_0502/diminico\\_3df\\_01\\_220502.pdf](https://www.ieee802.org/3/df/public/adhoc/electrical/22_0502/diminico_3df_01_220502.pdf)

[https://www.ieee802.org/3/df/public/adhoc/electrical/22\\_0418/ran\\_3df\\_elec\\_01a\\_220418.pdf](https://www.ieee802.org/3/df/public/adhoc/electrical/22_0418/ran_3df_elec_01a_220418.pdf)

## Call for action

- We need a clear process of adopting a loss budget
  - Proposals in terms of lengths and IL (assuming PAM4); detailed results with S-parameters would help
  - Explain the targeted application (switch, NIC, other)
- Until we adopt a loss budget we can't make any decisions on device electrical parameters (including reference Tx/Rx) or even modulation
  - Proposals in this area may be premature
- Let's not intermix these steps (e.g. run COM analysis on channels before loss budget is adopted)

# Contributors

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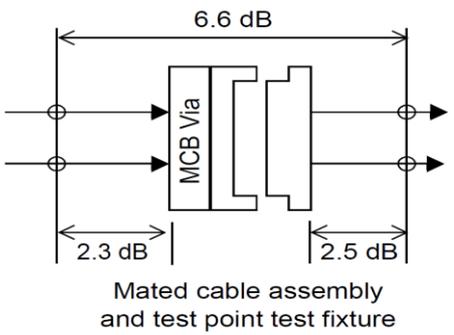
- **Sam Kocsis, Mike Rowland, Amphenol**
- **Nathan Tracy, TE Connectivity**

# 50G/100G CR insertion loss allocation

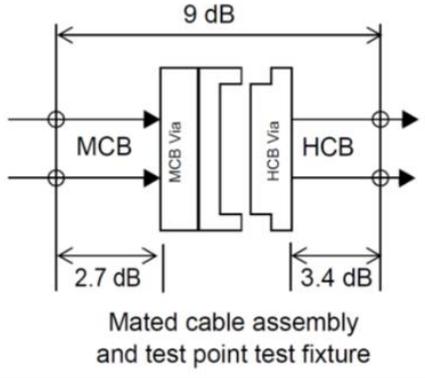
- The channel and test fixture insertion loss allocations are given in Table below for 50GBASE-R PHYs and 100GBASE-R PHYs for comparisons.

Component	50GBASE-CR,100BASE-CR2, 200GBASE-CR4 Insertion Loss dB @ 13.28 GHz	100GBASE-CR1,200GBASE-CR2, 400GBASE-CR4 Insertion Loss dB @ 26.56 GHz
Module Compliance Board (MCB) PCB	1.2	2.3
Host Compliance Board (HCB) PCB	1.38	2.5
Host PCB IL	7	6.875
Host Connector	1.69	1.6
Host	10.07	10.975
Mated Test Fixture (MTF)	3.65	6.6
MTF connector	1.07	1.6
Bulk cable and wire attachment	12.62	11.55
Channel	30	28.5

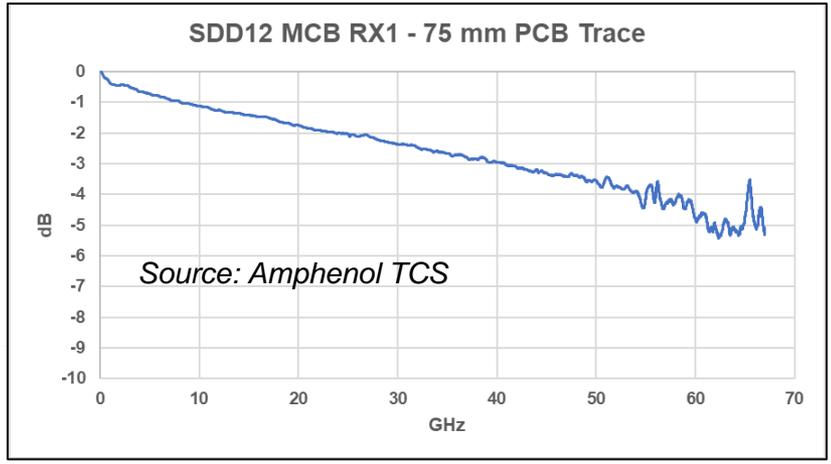
# Mated test fixture insertion loss



insertion loss @ 26.56 GHz  
 Figure source:  
 IEEE Draft P802.3ck/D3.1



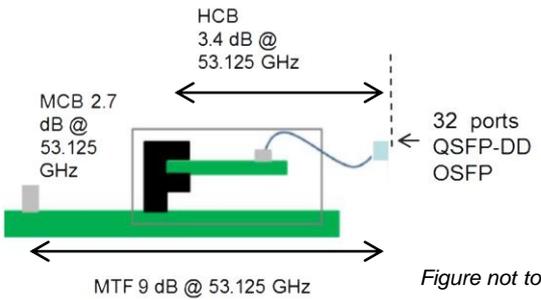
insertion loss @ 53.125 GHz



Board material	Length inches	dB/in 50GHz	dB/in 53GHz
DJN3+	3	1.2	1.3
Simulation	3	1.1	1.2

Component	Insertion Loss (dB)
Module Compliance Board (MCB) PCB - 2" of ~1.35 dB/in	2.7
Host Compliance Board (HCB) - 1inch*1.35dB/in + 6inch coax * .28dB/inch + 0.5dB via and co-ax transitions.	3.4
Mated Test Fixture (MTF)	9
MTF connector + 2 via's	2.9

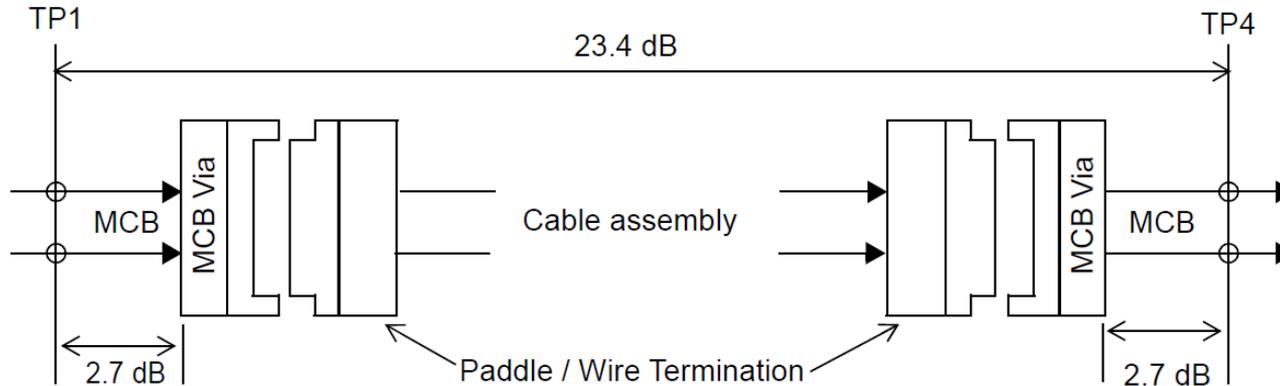
Mated test fixture insertion loss allocations @ 53.125 GHz



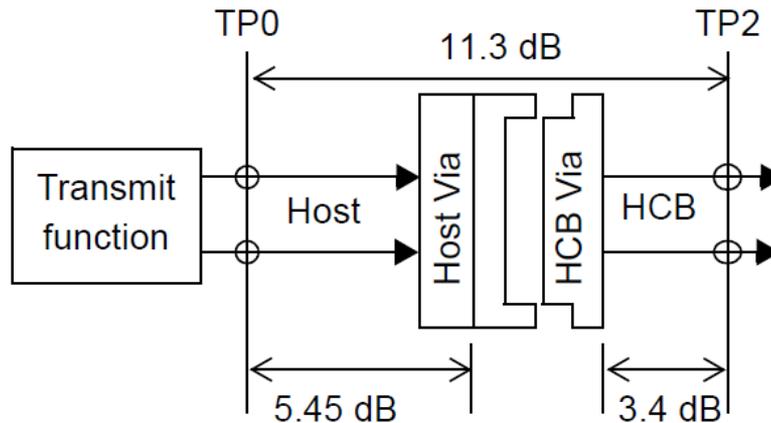
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# Cable assembly insertion loss

- Cable assembly and host insertion loss @ 53.125 GHz for 28 dB Channel



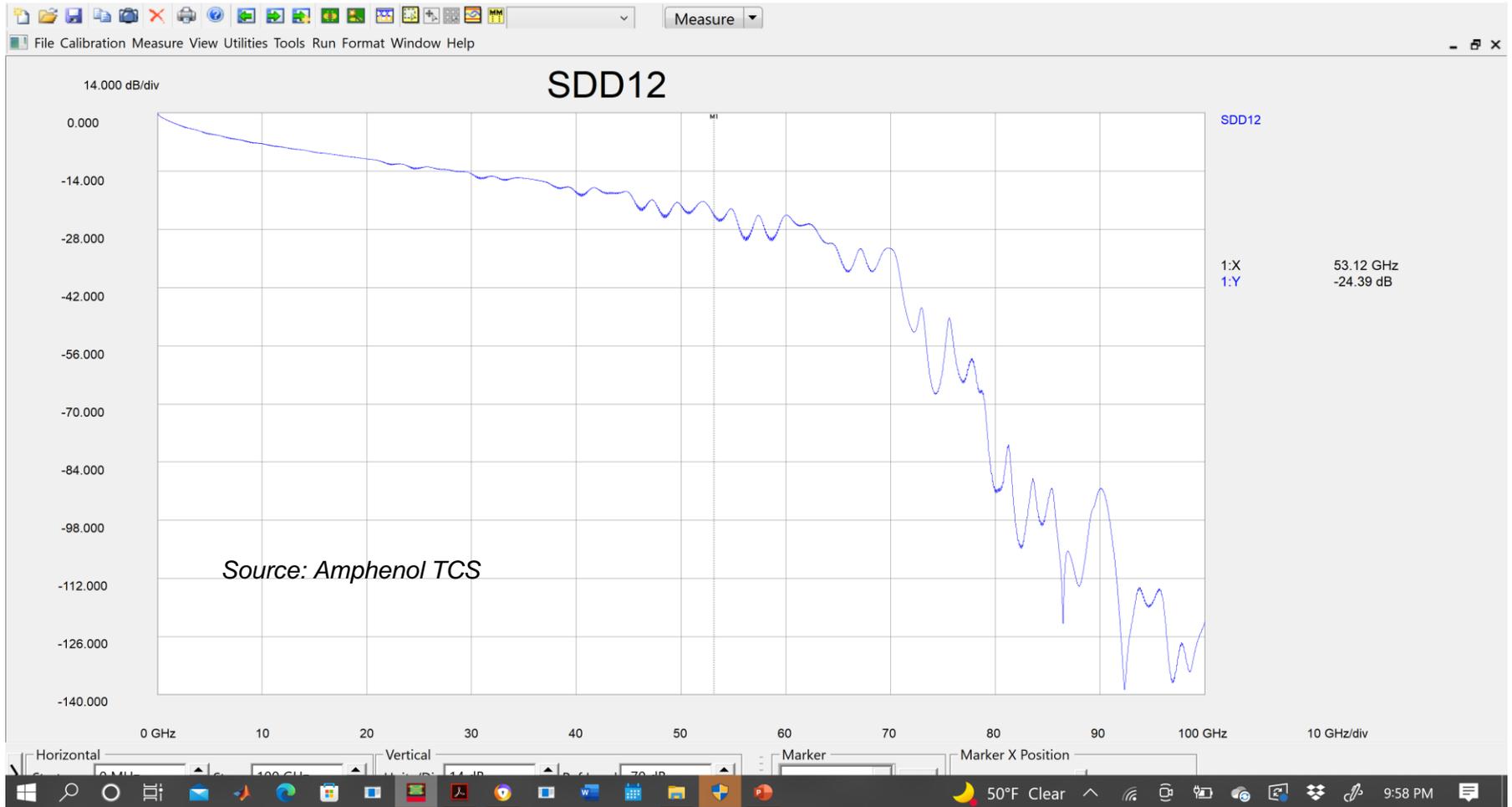
## Cable assembly insertion loss @ 53.125 GHz- 1 m



## Host insertion loss @ 53.125 GHz

# Cable assembly insertion loss - HFFS model

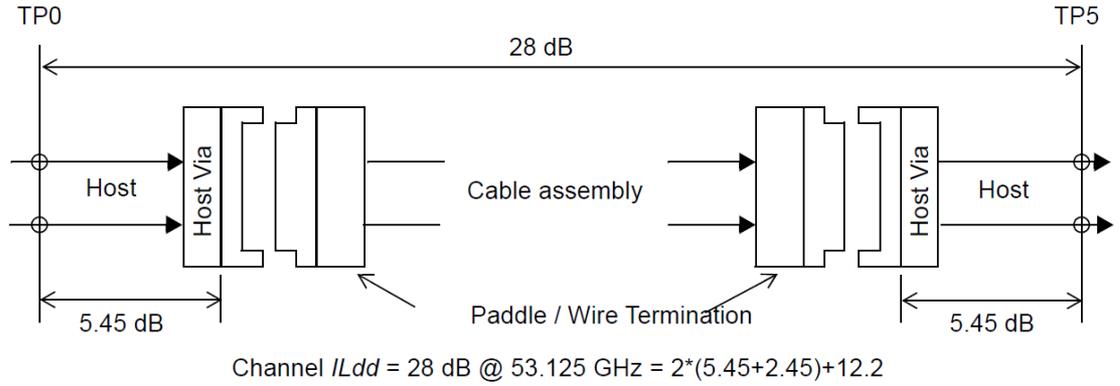
- 1 meter, 27 AWG



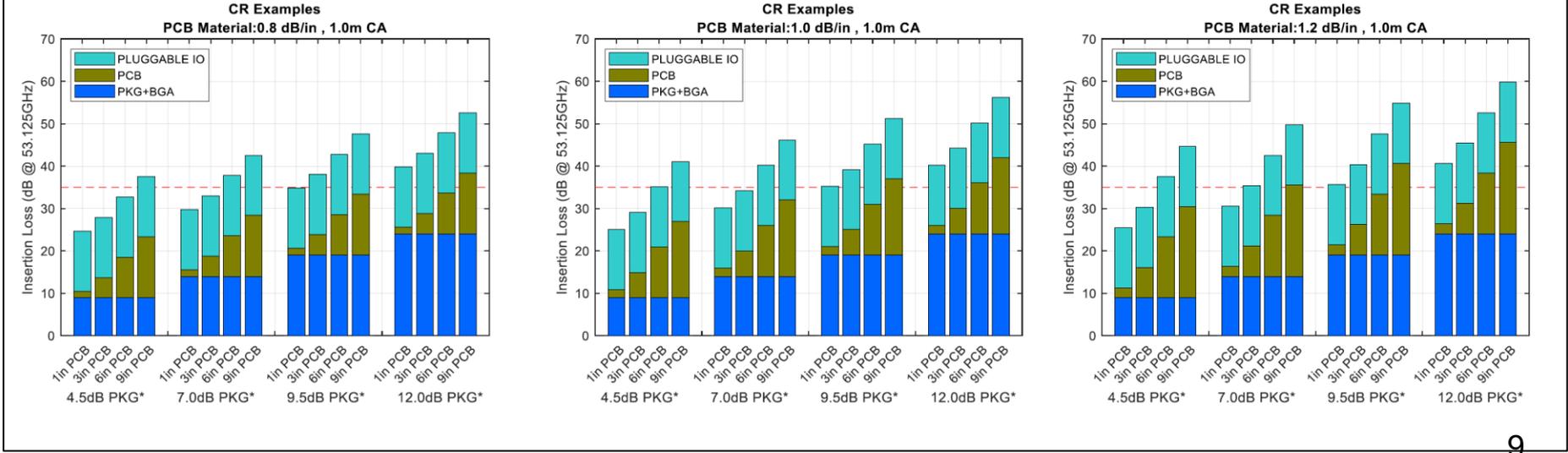


# Channel insertion loss - PCB Host

- TP0-TP5 Channel insertion loss consistent with cable assembly insertion loss.

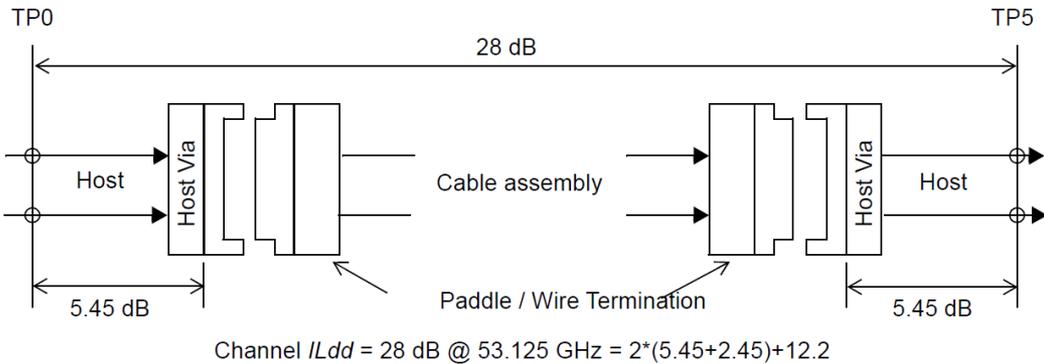


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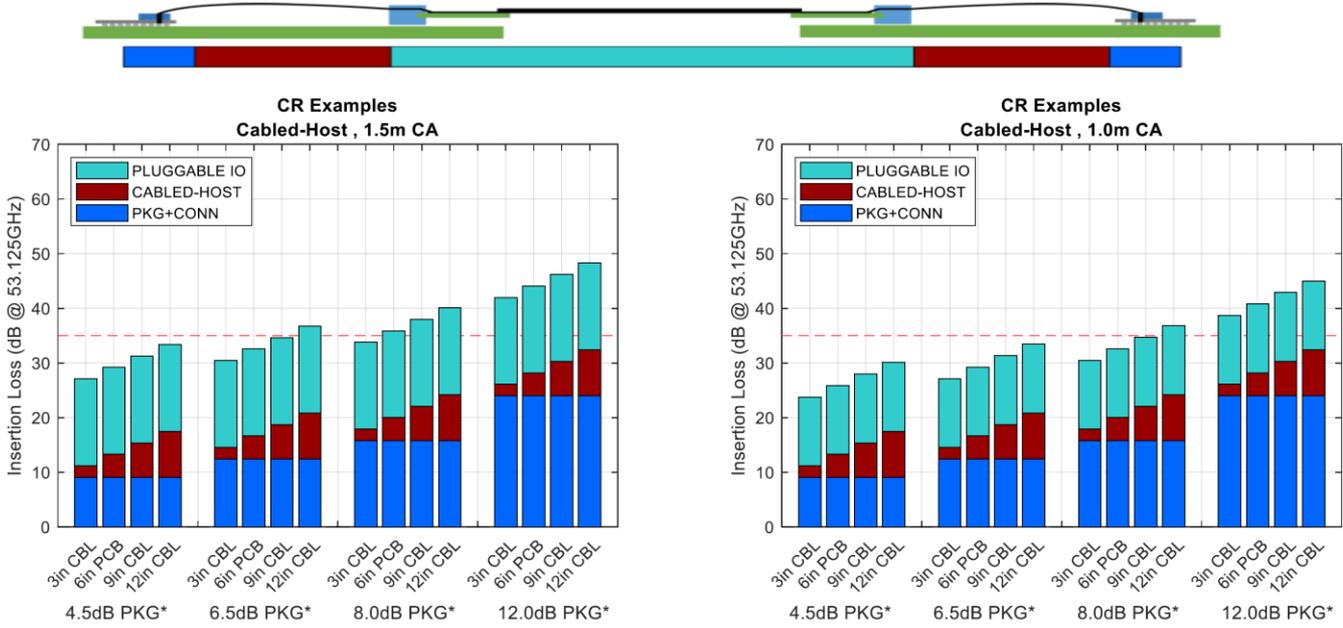


# Channel insertion loss - Cabled Host

- TP0-TP5 Channel insertion loss consistent with cable assembly insertion loss.



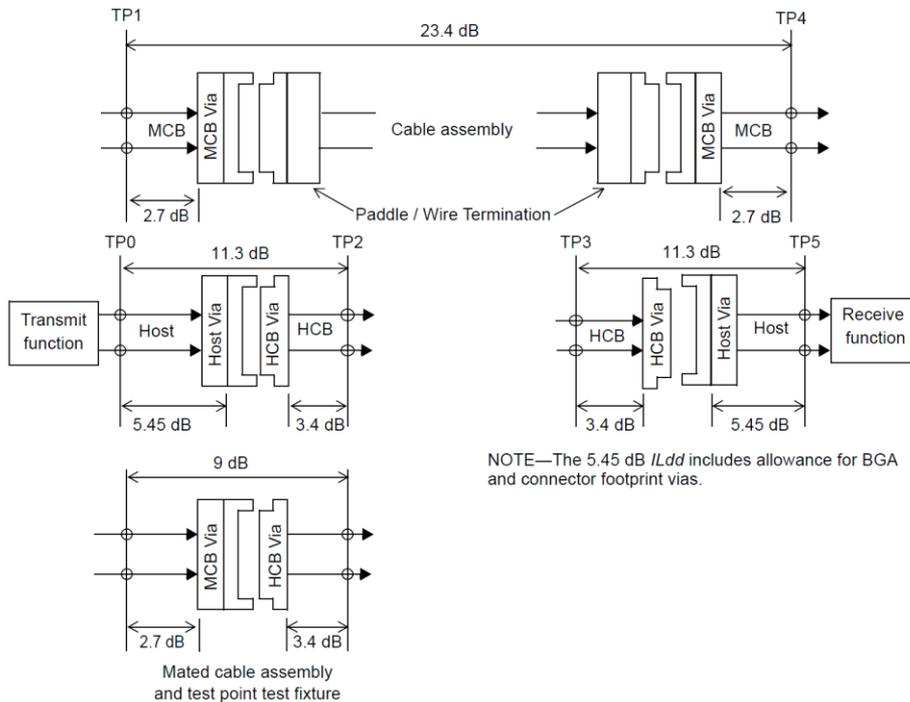
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# 802.3df - Annex XXXA (informative)

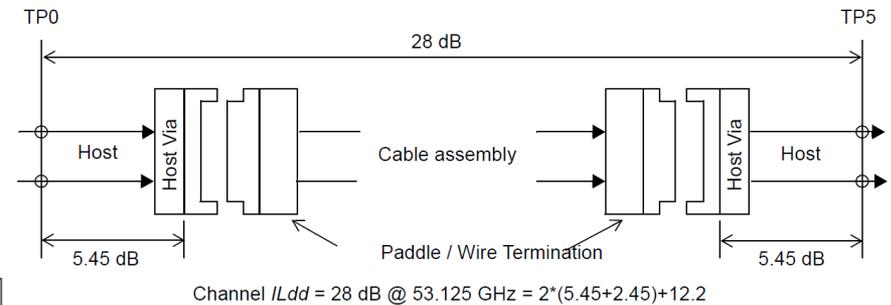
## Annex XXXA (informative)

Transmitter, receiver and channel parameters associated with test points TP0 and TP5 for 200GBASE-CR1, 400GBASE-CR2, 800GBASE-CR4, and 1.6TBASE-CR8.



NOTE—implications of RF connector (TBD)

Figure XXXA-3—Cable assembly, host, and test fixture insertion loss at 53.125 GHz



NOTE—Channel *ILdd* derived from cable assembly host, and mated test fixture

Figure XXXA-4—Channel insertion loss at 53.125 GHz

# Summary

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