

# FEC architecture considerations for 800GbE and 1.6TbE from performance, cost and evolution perspectives

Yuchun LU, Yan ZHUANG, Huawei Technologies

IEEE P802.3df 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force.

Montreal, Quebec, Canada

July 2022

# Background

- FEC architectures for 800GbE & 1.6TbE were discussed in [lu\\_3df\\_01\\_220518](#).
  - End-to-end FEC architecture is optimal for 200G AUIs & 200G PMDs.
  - Segmented FEC architecture is applicable for 100G AUIs & 200G PMDs.
    - Segmented FEC can be supported by Extended Sublayer.
  - Extended Sublayer is essential for 100G/200G AUIs & ZR PMDs.
- A PCS, FEC and PMA baseline is proposed for 800GbE and 1.6TbE using 100G PMD lanes was proposed in [lu\\_3df\\_logic\\_220623](#).
  - Speed up 200GbE & 400GbE clause 119, 2-way interleaved RS(544, 514).
  - 8 FEC lanes for 800GbE and 16 FEC lanes for 1.6TbE
  - 1:1 PMA remove the performance penalty due to the bitmuxing.

# Background (Cont'd)

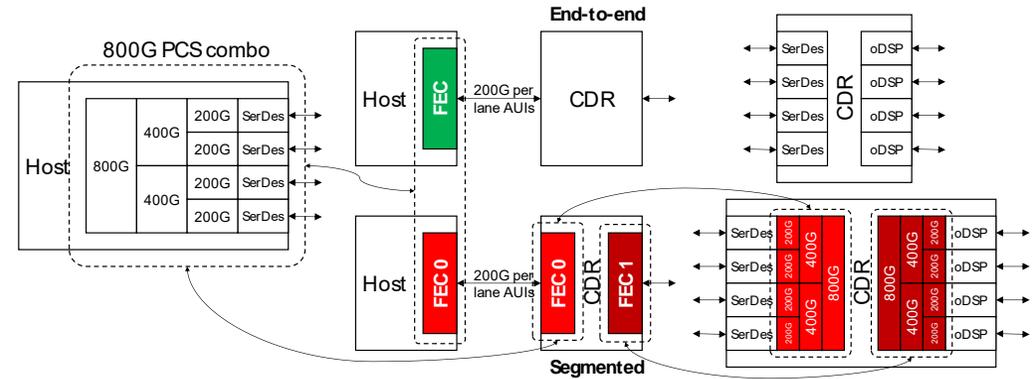
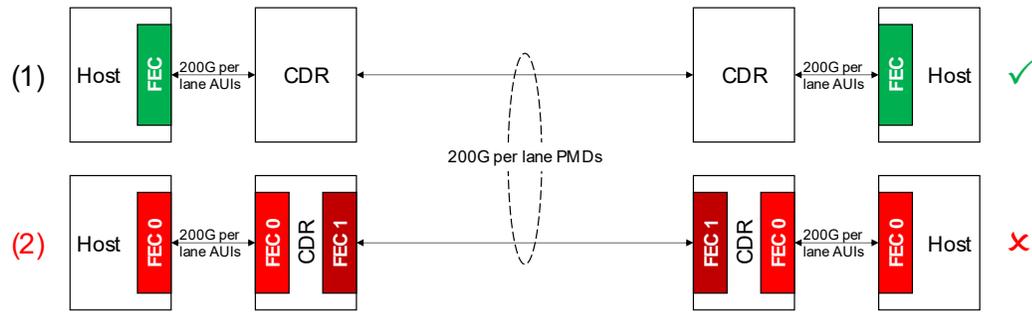
- Major considerations for 800GbE & 1.6TbE FEC architecture design.
  - **Performance**
    - Reasonable net coding gain (NCG), lower latency,
    - Higher reliability (lower FLR, better MTTFPA), ....
  - **Cost**
    - Better power efficiency (lower “pJ/bit”),
    - Smaller area (lower “cost/bit”), ...
  - **Evolution**
    - Backward compatibility (End-to-end FEC, or Segmented FEC),
    - Logic re-use (lower speed interface re-use logic of higher speed interface), ...

# The end-to-end FEC architecture is optimal and historically chosen for all PMDs except ZR PMDs.

Ethernet	Signaling Rate	AUI Interfaces		Task Force	Modulation	Encoding	FEC
100GbE	25.78125Gbps	CAUI-10	10*10.3125Gbps	802.3ba	NRZ	64B66B	No FEC / Firecode
		CAUI-4	4*25.78125Gbps	802.3bm	NRZ	64B66B / 256B257B TC	No FEC / RS(528, 514)
	26.5625Gbps	100GAUI-4	4*26.5625Gbps	802.3cd	NRZ	256B257B TC	RS(544, 514)
	53.125Gbps	100GAUI-2	2*53.125Gbps	802.3cd	PAM4	256B257B TC	RS(544, 514)
	106.25Gbps	100AUI-1	1*106.25Gbps	802.3ck	PAM4	256B257B TC	RS(544, 514)
200GbE	26.5625Gbps	200GAUI-8	8*26.5625Gbps	802.3bs	NRZ	256B257B TC	RS(544, 514)
	26.5625Gbps	200GAUI-4	4*53.125Gbps	802.3bs	PAM4	256B257B TC	RS(544, 514)
	106.25Gbps	200GAUI-2	2*106.25Gbps	802.3ck	PAM4	256B257B TC	RS(544, 514)
	TBD 212.5Gbps / 225Gbps	200GAUI-1	1 * 200G	802.3df	TBD PAM4 / SE-PAM4	256B257B TC	TBD
400GbE	26.5625Gbps	400GAUI-16	16*26.5625Gbps	802.3bs	NRZ	256B257B TC	RS(544, 514)
	53.125Gbps	400GAUI-8	8*53.125Gbps	802.3bs	PAM4	256B257B TC	RS(544, 514)
	106.25Gbps	400GAUI-4	4*106.25Gbps	802.3bs	PAM4	256B257B TC	RS(544, 514)
	TBD 212.5Gbps / 225Gbps	400GAUI-2	2 * 200G	802.3df	TBD PAM4 / SE-PAM4	256B257B TC	TBD
800GbE	106.25Gbps	800GAUI-8	8*106.25Gbps	802.3df	PAM4	256B257B TC	RS(544, 514)
	TBD 212.5Gbps / 225Gbps	800GAUI-4	4 * 200G	802.3df	TBD PAM4 / SE-PAM4	256B257B	TBD
1.6TbE	106.25Gbps	1.6TAUI-16	16*106.25Gbps	802.3df	PAM4	256B257B	RS(544, 514)
	TBD 212.5Gbps / 225Gbps	1.6TAUI-8	8 * 200G	802.3df	TBD PAM4 / SE-PAM4	256B257B	TBD

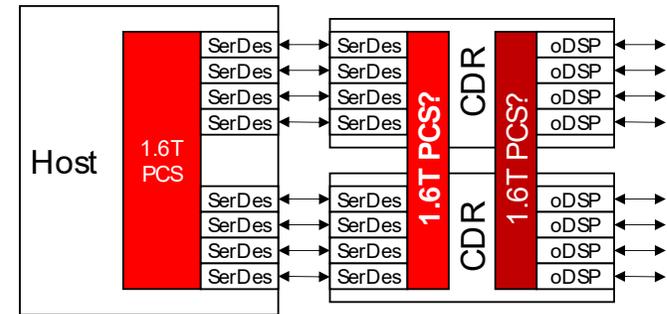
- The end-to-end FEC architecture is optimal and historically chosen for all PMDs except ZR PMDs.
  - 100GAUI-4, 200GAUI-8 and 400GAUI-16 use NRZ modulation, for which RS(544, 514) is far more than enough for performance, however they still carry the RS(544, 514) encoded data stream for PMDs. The RS(544,514) is chosen according to PMDs.
- If the signaling rates of AUIs are different due to the FEC selection, they are actually different AUIs.
  - CAUI-4 and 100GAUI-4 have different signaling rate due to different FEC, thus they are different AUIs with different clauses.

# The end-to-end FEC is optimal. FEC processing in CDR is not cost-effective, should apply only when necessary.



#	AUI BER <sub>0</sub>	PMD BER <sub>1</sub>	AUI BER <sub>2</sub>	E2E BER	ΔSNR
1	1e-5	2.4e-4	1e-5	2.60e-4	0.056dB
2	1e-5	2e-3	1e-5	2.02e-3	0.010dB
3	2e-4	2e-3	2e-4	2.40e-3	0.186dB
4	1e-3	2.4e-4	1e-3	2.24e-3	0.768dB
5	2.4e-4	2.4e-4	2.4e-4	7.20e-4	0.831dB
6	6.7e-4	6.7e-4	6.7e-4	2.01e-3	0.997dB

- ✓ If PMD is dominant, the segmented FEC has less than 0.2dB SNR gain.
- ✓ Case 1 is "100G AUIs & 100G PMDs";
- ✓ Case 2 is potential "100G AUIs & 200G PMDs";
- ✓ Case 2 & 3 are potential "200G AUIs & 200G PMDs".
- ✓ Case 4 ~ 6 are not reasonable, just for reference.

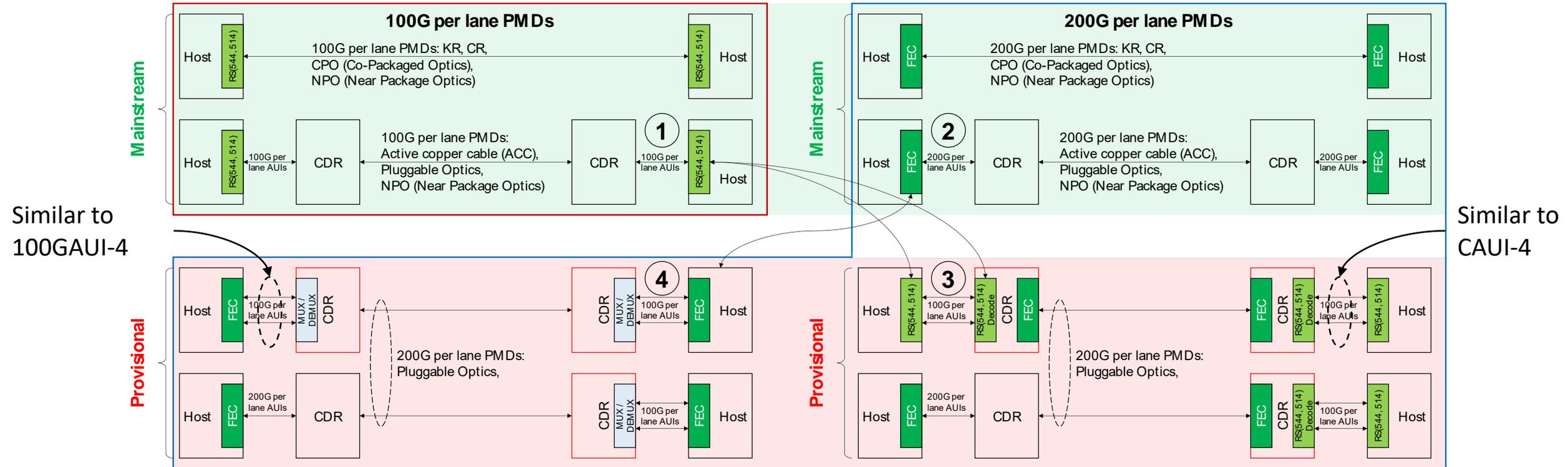


How to achieve 1.6T PCS across two CDR chip?

FEC processing in CDR has small SNR improvement, the gain is negligible if PMD is dominant in the end-to-end performance. [lu\\_3df\\_01\\_220518](#) page 4.

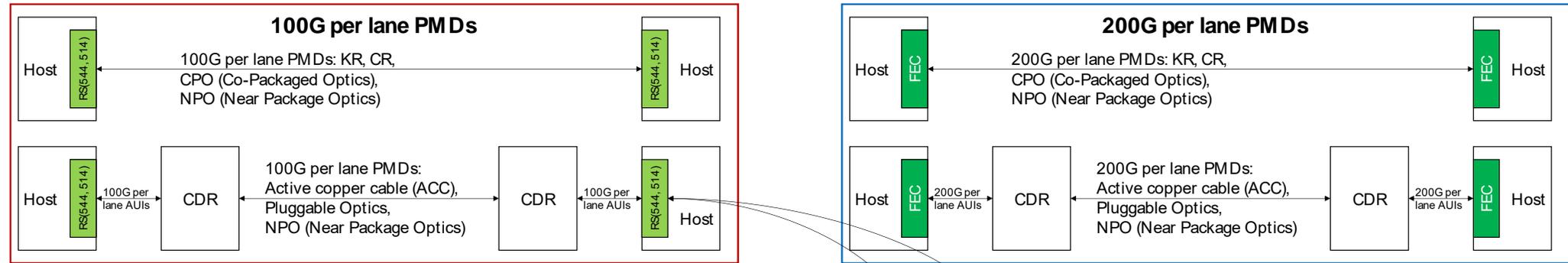
FEC processing in CDR is costly and inflexible, it should be applied only when necessary (e.g. gearbox & new FEC). [lu\\_3df\\_01\\_220518](#) page 5.

# The end-to-end FEC is optimal, new types of AUIs can be defined to support it and guarantee the competitiveness.

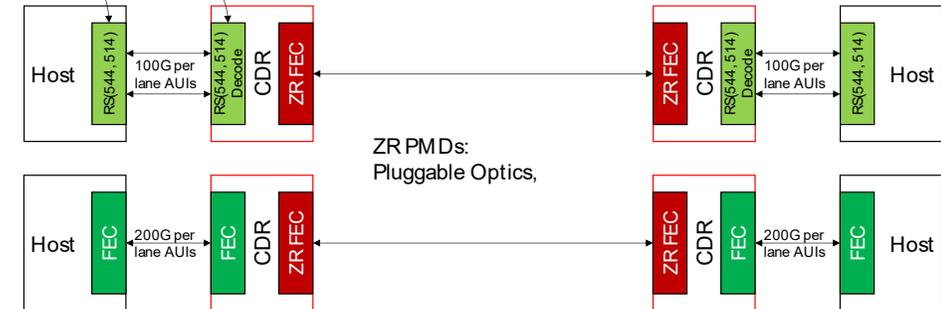


- ① End-to-end FEC is optimal for “100G AUIs and 100G PMDs” solutions.
- ② Choose the end-to-end FEC to optimize the “200G AUIs and 200G PMDs” solutions.
- ③ Use segmented FEC (Inverse FEC / Extender Sublayer) to support the backward compatibility to “legacy” 100G AUIs.
- ④ Define new 100G AUIs to support end-to-end FEC and optimize “100G SerDes and 200G PMD” solutions.

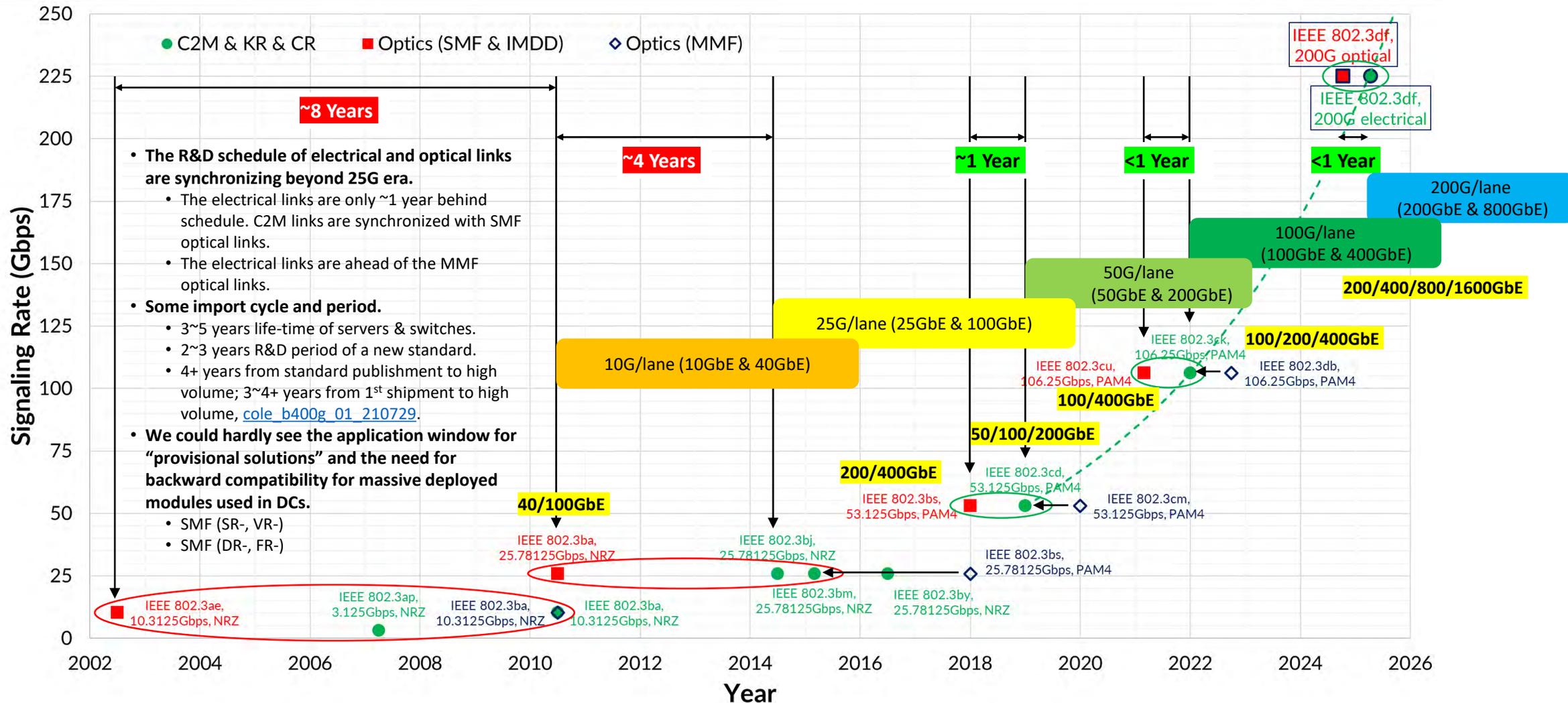
# The end-to-end FEC is optimal, the FEC & PCS should be optimized for segmented FEC for ZR-PMDs.



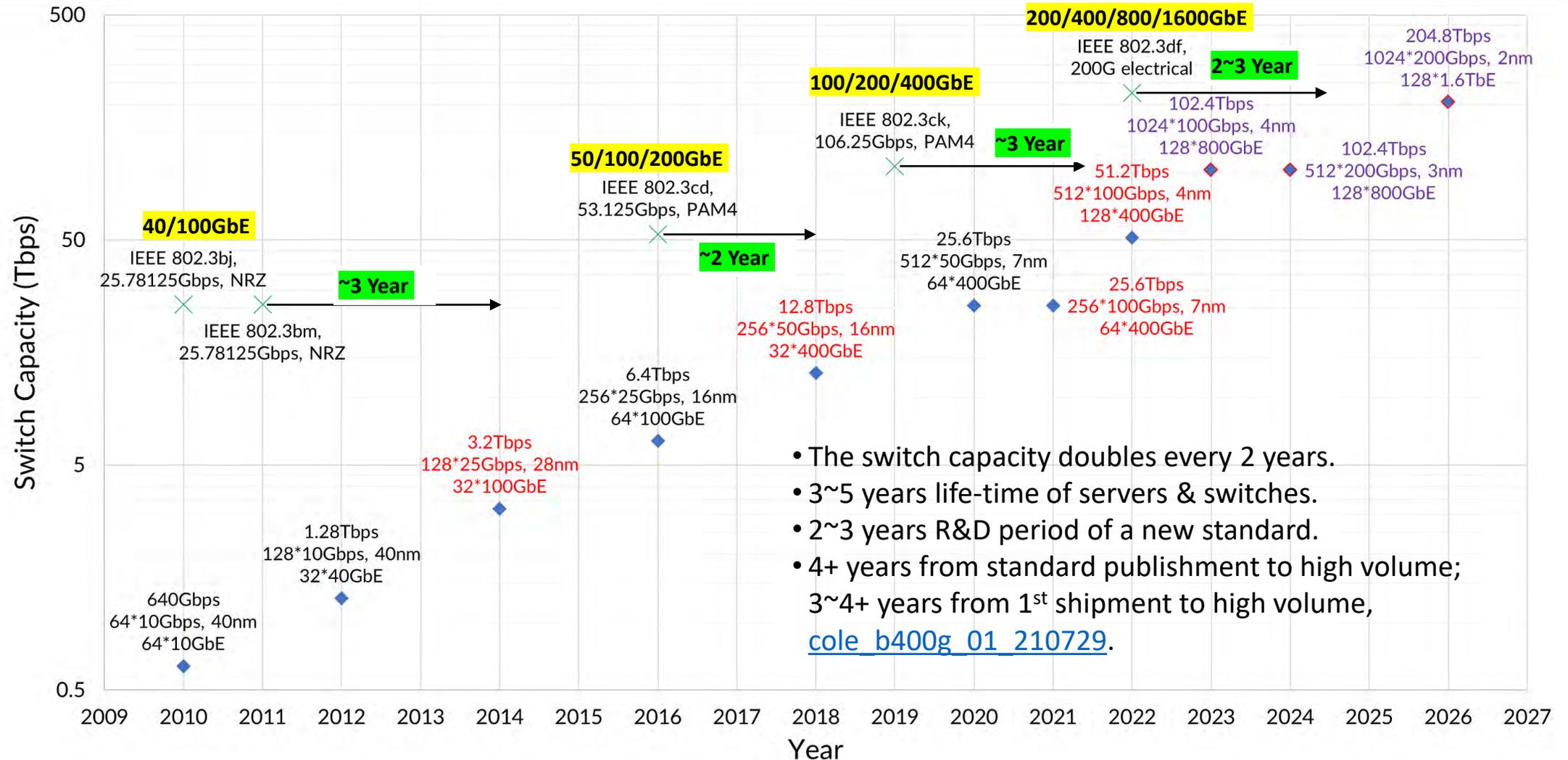
- ① For ZR-PMDs, the FEC & PCS will be implemented in the CDR, which requires the cost as low as possible.
- ② The AUIs for 800GbE and 1.6TbE should be optimized. For 100G/lane AUIs, “good enough” should be the design rule.



# The electrical links are catching up with the SMF optical links and they are ahead of the MMF optical links.

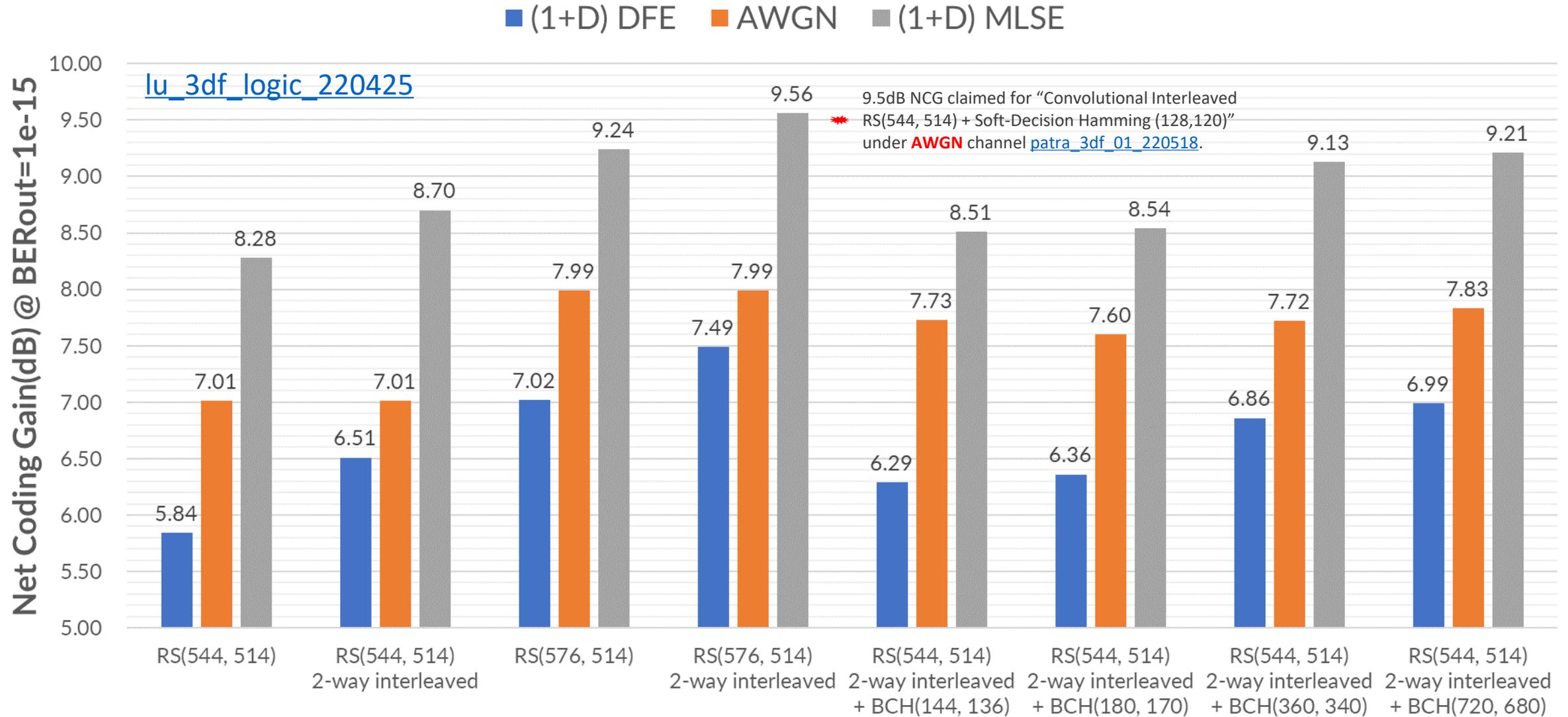


# The R&D of standard and switch chip are synchronized.

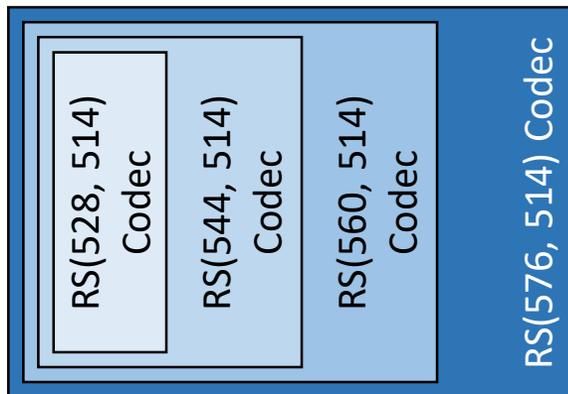
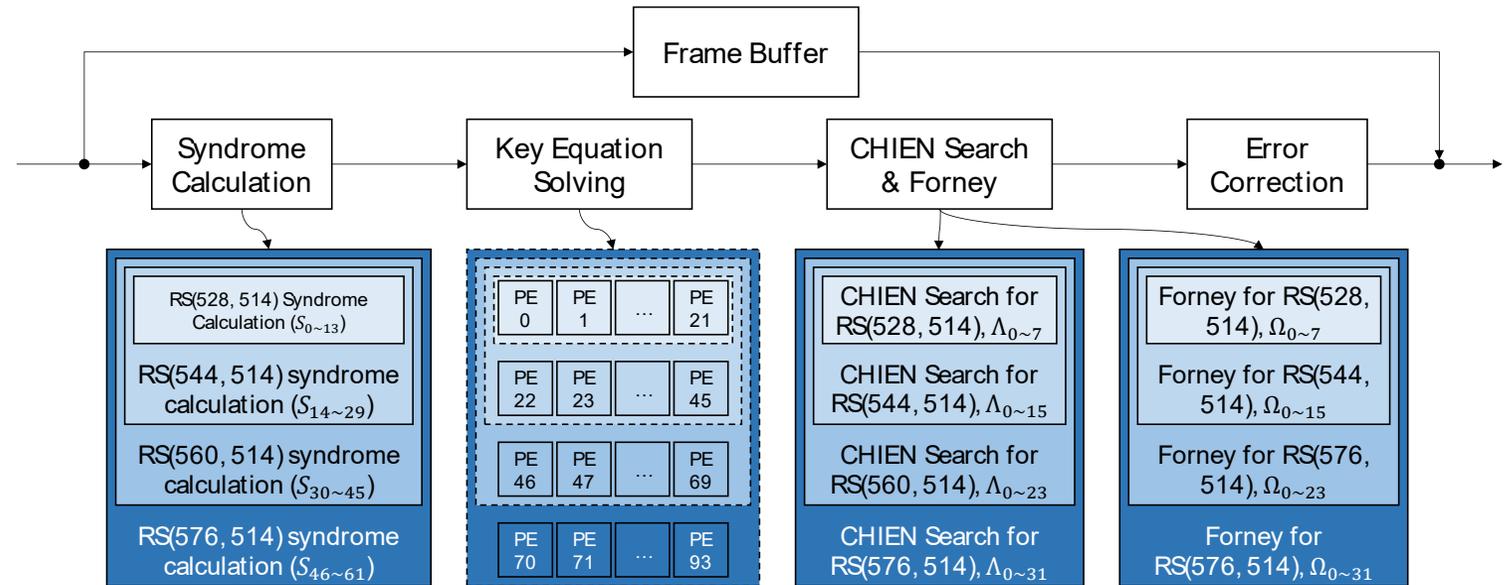
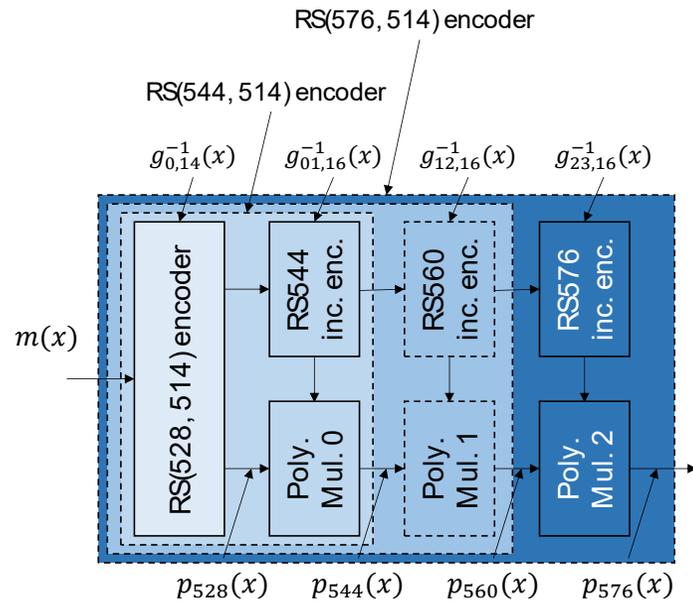


# FEC net coding gain (NCG)

When comparing FEC performance, penalty due to burst error should always be considered [lu\\_3df\\_01b\\_220215](#)! Soft-decision FEC schemes are vulnerable to burst errors.



# RS FEC code family can fully share logics by incremental encoding/decoding from implementation prospective



- RS FEC code can fully share logics by incremental encoding and decoding implementation, it is flexible to support multiple RS codes.
- Reference clock multiplier (RCM) for RS(528, 514), RS(544, 514), RS(560, 514) and RS(576, 514) are 33:32, 34:32, 35:32 and 36:32, respectively. The FEC frame size is increased by  $n \cdot 160$  bits. No additional gearbox is required.

# Summary

- 800GbE & 1.6TbE FEC architecture considerations
  - The end-to-end FEC architecture is optimal and historically chosen for all PMDs except ZR PMDs.
  - Segmented FEC architecture (Inverse FEC / Extender Sublayer) is applicable to support the backward compatibility to “legacy” 100G AUIs.
  - New 100G AUIs can be defined to support end-to-end FEC and optimize “100G SerDes and 200G PMD” solutions.
- 800GbE & 1.6TbE FEC architecture evolution
  - The architecture evolution was resolved by defining new AUIs with lower signaling rate to support end-to-end FEC architecture, which is optimal, e.g. 100GAUI-4, use 4\*26.5625Gbps NRZ with RS(544, 514) FEC.
  - Segmented FEC architecture (Inverse FEC / Extender Sublayer) is also applicable to terminate the “legacy” PCS and add a new PCS, e.g. 100G-ZR & 400G-ZR.
  - We never resolve the architecture evolution issue by breaking down the FEC into two pieces and concatenating. “Concatenated FEC architecture” has nothing to do with “AUI and PMD evolution”, but introduces a lot of known showstopper issues (e.g. [lu\\_3df\\_01\\_220518](#) page 15).

# Recommendation

- Use “End-to-end FEC” architecture (support bit-transparent CDR and flexible CDR breakout) for the mainstream applications, i.e. “100G AUIs & 100G PMDs” and “200G AUIs & 200G PMDs” to achieve low cost, low power consumption, low latency and flexibility (CDR breakout).
- Use “Segmented FEC” (Inverse FEC or Extended Sublayer) architecture for the provisional applications, i.e. “100G AUIs & 200G PMDs” . Use Extended Sublayer for ZR applications to compensate the clock drift difference between AUIs (+/-100ppm) and ZR PMDs (+/- 20ppm).
- RS code family is a good candidate for the optimal end-to-end FEC architecture.
  - Well understood by the industry, numerous industrial practices from 25G up to 100G.
  - It is the best in performance with DSP algorithm and burst errors considered.
  - It can fully share logics by incremental encoding/decoding from implementation prospective.
  - It can provide flexible FEC options regarding the net coding gain, latency and power consumption, etc.

# Q & A