A 212.5 Gbps-PAM4 High-Loss Chip-to-Module Channel and Its Characteristics

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Background and Introduction

• Update to Q3’22 presentation “224 Gbps Chip-to-Module Link Simulation and Analysis Update 2” (oif2022.355.00), with
  – Updated chip-to-module channel which is based on a real/practical high-density/radix switch device and board design

• Progress history
  – Update to Q2’22 presentation “224 Gbps Chip-to-Module Link Simulation and Analysis Update” (oif2022.174.01), with
    • Updated chip-to-model COM configuration and analysis results
    • Time-domain link simulation results
  – Update to Q3’21 presentation “212/224 Gbps Chip-to-Module Link Simulation and Analysis” (oif2021.446.00), with
    • Latest C2M channel model(s)
    • Proposed CEI-224G-LR-PAM4 reference TX (oif2022.067.00)
    • Proposed CEI-224G-LR-PAM4 reference die/package model (oif2022.065.02)
    • TP1a reference scope RX based on the proposed CEI-224G-LR-PAM4 reference RX AFE (oif2022.067.00)
Channel Configuration Summary

- 2 Channels were analyzed
  - CH11: Shown on the left
  - CH12: Same as CH11 with 10-in Host PCB

- Crosstalk
  - 2 FEXT
  - 1 NEXT

Insertion Loss Break Down

<table>
<thead>
<tr>
<th>Component</th>
<th>Insertion Loss (dB) @ 53.125GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CH11 (8-in)</td>
</tr>
<tr>
<td>BGA via</td>
<td>0.95</td>
</tr>
<tr>
<td>PCB</td>
<td>11.2</td>
</tr>
<tr>
<td>Connector via</td>
<td>0.95</td>
</tr>
<tr>
<td>Connector</td>
<td>1.5</td>
</tr>
<tr>
<td>Module card</td>
<td>2.37</td>
</tr>
<tr>
<td>Total</td>
<td>17.14</td>
</tr>
</tbody>
</table>
C2M Channel Characteristics (CH11)

- IL: 17.14dB @ 53.125 GHz
- ILD ~= 1dB
- RL ~= 10dB
- FEXT ~= 46dB NEXT ~= 48dB, ICR ~= 24.36dB
C2M Channel Characteristics (CH12)

- IL: 20.03dB @ 53.125 GHz
- ILD ~1dB
- RL ~10dB
- FEXT ~48dB NEXT ~49dB, ICR ~23.65dB
Summary

• Updated chip-to-module channel based on a high-density/radix switch device and board design with 8-inch and 10-inch PCB lengths

• Key characteristics (at 53.125 GHz)

<table>
<thead>
<tr>
<th>Channel</th>
<th>IL (dB)</th>
<th>ILD (dB)</th>
<th>RL (dB)</th>
<th>ICR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH11 (w/ 8” Host PCB)</td>
<td>17.14</td>
<td>~1</td>
<td>~10</td>
<td>24.36</td>
</tr>
<tr>
<td>CH12 (w/ 10” Host PCB)</td>
<td>20.03</td>
<td>~1</td>
<td>~10</td>
<td>23.65</td>
</tr>
</tbody>
</table>