4				- •				
2012003 6 Move to abook total 3,301,126,310,230,210,126,310 de 3 side 6 sit the baseline for the Latter SCATE, with the noted details (PCS later for small post side of sit the baseline for the Latter SCATE, with the noted details (PCS later for small post side of sit the baseline for the Latter SCATE, with the noted details (PCS later for small post side of sit the same side of si	Session 01-2023	Motion # 4	Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet" previously approved by IEEE P802.3df Task Force noted on Slide #7 of https://www.ieee802.org/3/dj/public/23_01/23_0116/dambrosia_3dj_01a_230116.pdf		Mover Ali Ghiasi	Second Adee Ran		Notes
10-1203 10 More to ode spatial per gardent in the supports 800 80% reports on the supports 800 80% reports 800	01-2023	5	https://www.ieee802.org/3/dj/public/23_01/23_0116/dambrosia_3dj_		Adee Ran	Mike Dudek	•	
1. 16TB COVIET, with the noted details (PCS lane forming and AM construction) 208.065 05.7073 1 Nove to be determined later to be determined by the control of the public later as public late	01-2023	6			Ran	Dudek	· ·	
Replace the following objective. - Doffies a physical jown prescribation that supports 800 Gb/s operation over a single 50f in each direction with lengths up to at least 30 km with the following consistent studyout 80 february 200 februar	01-2023	10	1.6TbE PCS/FEC, with the noted details (PCS lane forming and AM construction)		Gustlin	Brown	•	Replaced by May 2023 Motion #4
- Define a physical layer specification that supports 400 Gb/s operation over 2 pairs of SNP with lengths up to at least 2 km for the physical layer specification that supports 400 Gb/s operation over 2 pairs of SNP with lengths up to at least 2 km for the physical layer specification that supports 400 Gb/s operation over 2 pairs of SNP with lengths up to at least 2 km for the physical layer specification that supports 200 Gb/s Parameter to the previously adopted 1.6Te FCS baseline from gustlin 3dj .01b, 230206.pdf. 4 More to: 4 Adopt ran 3dj .01a, 2303, sildes 6.24 as a baseline for the PMAs with 200 Gbps per lane signaling based per lane signaling and the physical layer specification that supports 2dj .01b, 2303 sildes 6.24 as a baseline for the PMAs with 200 Gbps per lane signaling based provided and the provided provi	03-2023	1	Replace the following objective: • Define a physical layer specification that supports 800 Gb/s operation over a single SMF in each direction with lengths up to at least 10 km with the following two objectives: • Define a physical layer specification that supports 800 Gb/s operation over 1 wavelength over a single SMF in each direction with lengths up to at least 10 km • Define a physical layer specification that supports 800 Gb/s operation over 4		Nowell	Johnson	802.3: 63 / 3 / 12	
1.03-2023 3 Move to Adopt opasanick 3dj (0.12-303, sides 3, 5-9, 12-13, as a supplement to the previously adopted 1.01E-PCS baseline from gustlin, 3dj, 01b_230006.pdf. Move to: Adopt ran, 3dj, 01a_2303, sides 6-24 as a baseline for the PMAs with 200 Gbps per lane signaling Move to: Adopt para, 3dj, 01b_2303 sides 6-108, 13, 14, and 20 to 23 as part of the FEC approach for Adopt para, 3dj, 01b_2303 sides 6-108, 13, 14, and 20 to 23 as part of the FEC approach for Adopt para, 3dj, 01b_2303 sides 6-108, 270 FEA, and PMY XS noted on slide #4 of dambrosia, 3dj, 01a_2305 for all 200 Gby, per lane signaling based PMYs for 200 Gbe, 400 Gbb, and 300 Gbb Move to: adopt the PKS, DFX S, and PMY XS noted on slide #4 of dambrosia, 3dj, 01a_2305 for all 200 Gby, per lane signaling based PMYs for 200 Gbe, 400 Gbb, and 300 Gbb Move to: adopt the PKS, DFX S, and PMY XS noted on slide #4 of dambrosia, 3dj, 01a_2305 for all 200 Gby, per lane signaling based PMYs for 200 Gbe, 400 Gbb, and 300 Gbb Move to adopt putslin, 3dj, 01b_230206, slides 6-12, as the baseline for the 1.6TB PCF/FEC Move to: a dopt the PKS, DFX S, and PMY XS noted on slide #4 of dambrosia, 3dj, 01a_2305 for all 200 Gby, per lane signaling based PMYs for 200 Gbe, 400 Gbb, and 300 Gbb Move to: adopt the PKS, DFX S, and PMY XS noted on slide #4 of dambrosia, 3dj, 01a_2305 for all 200 Gby, per lane signaling based PMYs for 200 Gbb, 400 Gbb, and 300 Gbb Move to: adopt the PKS, DFX S, and PMY XS noted on slide #4 of dambrosia, 3dj, 01a_2305 for all 200 Gby, per lane with the per lane signaling based PMYs for 200 Gbb, 400 Gbb, and 300 Gbb Move to: adopt the PKS, DFX S, and PMY XS noted on slide #4 of dambrosia and the per lane signaling based PMYs for 200 Gbb, 400 Gbb, and 300 Gbb Move to: adopt the PKS, DFX S, and PMY XS noted on slide #4 of dambrosia and the per lane signaling based PMYs for 200 Gbb, 400 Gbb, and 300 Gbb Move to: adopt the PKS, DFX S, And PMY XS noted on slide #4 of dambrosia and the per lane signaling based PMYs	03-2023	2	• Define a physical layer specification that supports 400 Gb/s operation over 2		Welch	Johnson	•	
### Adopt ran, 3dj_01a_2303, sildes 6-24 as a baseline for the PMAs with 200 Gbps per lane signaling ### Owner to: ### Adopt parra, 3dj_01a_2303, sildes 6-to 8, 13, 14, and 20 to 23 as part of the FEC approach for ### Adopt parra, 3dj_01b_2303 sildes 6 to 8, 13, 14, and 20 to 23 as part of the FEC approach for ### A00GBASE-DR4, 300GBASE-DR4.2, 800GBASE-PR4 ### A00GBASE-DR4, 200GBASE-PR4 ### A00GBASE-DR4, 200GBASE-PR4 ### OWNERS-DR4, 200GBASE-PR4	03-2023	3	Move to: • adopt opsasnick_3dj_01a_2303, slides 3, 5-9, 12-13, as a supplement to the	https://www.ieee802.org/3/dj/public/23_03/opsasnick_3dj_01a_2303.pdf	Opsasnick	He	•	
Adopt parts_3dj_01b_2303 slides 6 to 8, 13, 14, and 20 to 23 as part of the FEC approach for 800GBASE-DR4, 800GBASE-DR4-2, 800GBASE-DR2-2 pending WG objective approval) • 200GBASE-DR1, 200GBASE-BR1 with FEC lane rate, convolutional interleaver details, and 1.6T support to be determined later 05-2023 3 Move to adopt the PCS, DTE XS, and PHY XS noted on slide #4 of dambrosia_3dj_01a_2305 for all 200 Gb/s per lane signaling based PHYs for 200 GbC, 400 GbC, and 800 GbE 05-2023 4 Move to adopt the PCS, DTE XS, and PHY XS noted on slide #4 of dambrosia_3dj_01a_2305 for all 200 Gb/s per lane signaling based PHYs for 200 GbC, 400 GbC, and 800 GbE 05-2023 5 Move to adopt twillin_3dj_01b_230206, sildes 6-12, as the baseline for the 1.6TbE PCS/FEC 05-2023 5 Move to: • Adopt the following backplane objectives for 200GBASE-KR1, 400BASE-KR2, 800GBASE-KR3, and 1.6TBASE-KR8: • O Define a physical layer specification that supports 200 Gb/s operation over 1 lane over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz • O Define a physical layer specification that supports 800 Gb/s operation over 2 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz • Define a physical layer specification that supports 800 Gb/s operation over 8 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz • Define a physical layer specification that supports 800 Gb/s operation over 8 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz • Define a physical layer specification that supports 800 Gb/s operation over 8 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz • Define a physical layer specification that supports 800 Gb/s operation over 8 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz • Define a physical layer specification that supports 800 Gb/s operation over 8 lanes over electrical b	03-2023	4	• Adopt ran_3dj_01a_2303, slides 6-24 as a baseline for the PMAs with 200 Gbps	https://www.ieee802.org/3/dj/public/23 03/ran 3dj 01a 2303.pdf	Ran	Nicholl	802.3: 69 / 1 / 13	
dambrosia_3dj_01a_2305 for all 200 Gb/s per lane signaling based PHYs for 200 GbE, 400 GbE, and 800 GbE 05-2023 4 Move to adopt gustlin_3dj_01b_230206, slides 6-12, as the baseline for the 1.6TbE PCS/FEC 206.pdf Move to: Adopt the following backplane objectives for 200GBASE-KR1, 400BASE-KR2, 800GBASE-KR4, and 1.6TBASE-KR8: O Define a physical layer specification that supports 200 Gb/s operation over 1 lane over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz O Define a physical layer specification that supports 800 Gb/s operation over 2 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz O Define a physical layer specification that supports 800 Gb/s operation over 4 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz O Define a physical layer specification that supports 800 Gb/s operation over 4 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz O Define a physical layer specification that supports 800 Gb/s operation over 4 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz O Define a physical layer specification that supports 1.6 Tb/s operation over 8 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at	03-2023	5	Adopt patra_3dj_01b_2303 slides 6 to 8, 13, 14, and 20 to 23 as part of the FEC approach for • 800GBASE-DR4, 800GBASE-DR4-2, 800GBASE-FR4 • 400GBASE-DR2, 400GBASE-DR2-2* (Note: 400GBASE-DR2-2 pending WG objective approval) • 200GBASE-DR1, 200GBASE-FR1 with FEC lane rate, convolutional interleaver details, and 1.6T support to be	https://www.ieee802.org/3/dj/public/23 03/patra 3dj 01b 2303.pdf	Healey	Dudek	802.3: 70 / 5 / 15	
1.6TbE PCS/FEC Discrete PCS/	05-2023	3	dambrosia_3dj_01a_2305 for all 200 Gb/s per lane signaling based	https://www.ieee802.org/3/dj/public/23 05/dambrosia 3dj 01a 2305.pdf	Dudek	Nicholl	•	
● Adopt the following backplane objectives for 200GBASE-KR1, 400BASE-KR2, 800GBASE-KR4, and 1.6TBASE-KR8: ○ Define a physical layer specification that supports 200 Gb/s operation over 1 lane over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz ○ Define a physical layer specification that supports 400 Gb/s operation over 2 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz ○ Define a physical layer specification that supports 800 Gb/s operation over 4 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz ○ Define a physical layer specification that supports 1.6 Tb/s operation over 8 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at	05-2023	4			Gustlin	Ran	•	Replaces Jan 2023 Motion #4
	05-2023	5	• Adopt the following backplane objectives for 200GBASE-KR1, 400BASE-KR2, 800GBASE-KR4, and 1.6TBASE-KR8: o Define a physical layer specification that supports 200 Gb/s operation over 1 lane over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz o Define a physical layer specification that supports 400 Gb/s operation over 2 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz o Define a physical layer specification that supports 800 Gb/s operation over 4 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz o Define a physical layer specification that supports 1.6 Tb/s operation over 8 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at	Key Motions	Mellitz	Weaver	•	

05-2023	6	Move to: • Adopt differential PAM4 signaling as the basis for all of the 200 Gbps/lane passive copper cable and backplane PMDs and adopt RS(544,514,10) as the only FEC encoding for all of the 200 Gbps/lane passive copper cable and backplane PMDs		Li, Mike	Ghiasi	802.3: Passed by Unanimous Consent
05-2023	7	Move to adopt a CRU bandwidth and jitter tolerance corner frequency of 4 MHz for all 802.3dj PMD/AUIs operating at RS544 FEC (The calculation for CRU BW is based on the following fBaud/26562.5)		Ghiasi	Li, Mike	802.3: Passed by Unanimous Consent
05-2023	8	Move to: • adopt a DERO value of 2.67e-5 (equivalent to measured BER of 4e-5 with precoding ON) as the total allocation for higher-loss AUIs within a PHY (BER division between C2C and C2M as well as the measurement method to be determined later)		Ran	Kota	802.3: 75 /3 /20
05-2023	9	Move to: • Adopt patra_3dj_01b_2303 slides 6 to 8, 13, 14, and 20 to 23 as part of the FEC approach for 800GBASE-LR4 with FEC lane rate and convolutional interleaver details to be determined later	https://www.ieee802.org/3/dj/public/23 03/patra 3dj 01b 2303.pdf	Rodes	Ghiasi	802.3: Passed by Unanimous Consent
05-2023	10	Move to: ■ adopt DP-16QAM modulation on a single wavelength as the basis for the following objectives: O Define a physical layer specification that supports 800 Gb/s operation: ■ over 1 wavelength over a single SMF in each direction with lengths up to at least 10 km ■ over a single SMF in each direction with lengths up to at least 40 km		Nowell	Brown	802.3: Passed by Unanimous Consent
07-2023	4	Move to adopt the direction of adding an option to support only RS544 FEC (aka Bypass Inner FEC) for the single wavelength 500m and 2km optical PMDs with the mechanism to enable it remaining TBD		Welch	Rechtman	802.3: Passed by Unanimous Consent
07-2023	5	Move to adopt BCH FEC as defined in kota_3dj_01a_307.pdf slides 6-18 as the baseline FEC specification for the single wavelength 10 km 800Gb/s optical PMD.	https://www.ieee802.org/3/dj/public/23 07/kota 3dj 01a 2307.pdf	Maniloff	Stassar	802.3: 60 / 14 / 20
07-2023	6	Move to adopt one DERO value of 2.67e-5 (equivalent to measured BER of 4e-5 with precoding ON) as the total allocation for 200Gbps/lane AUIs within a PHY (BER division between C2C and C2M as well as the measurement method to be determined later)		Ran	Tobey PR. Li	802.3: Passed by Unanimous Consent
07-2023	7	Move to adopt a die-to-die insertion loss <= 40 dB at 53.125 GHz for 200GBASE-CR1, 400GBASE-CR2, 800GBASE-CR4 and 1.6TBASE-CR8 PHYs		Mike Li	Tracy	802.3: Passed by Unanimous Consent
07-2023	8	Move to adopt stateless 64b/66b encode and decode, as defined in opsasnick_3dj_01a_2307.pdf slides 7 and 8, as an option for 200GbE and 400GbE for all 200G/lane PHY/PMDs	https://www.ieee802.org/3/dj/public/23 07/opsasnick 3dj 01a 2307.pdf	Opsasnick	Gustlin	802.3: Passed by Unanimous Consent
07-2023	9	Move to adopt the same inner FEC architecture used for 200GbE/400GbE/800GbE for 1.6TbE SMF optical PMDs (500m/2km)		Ghiasi	Kota	802.3: Passed by Unanimous Consent
07-2023	10	Move to adopt the 4x RS codewords interleaving for 200GbE and 400 GbE using 200G/lane AUIs or PMDs, as shown in slides 4-6 and 10 of he_3dj_02a_2307 along with deskew (alignment) to codeword boundaries for 100G/lane input lanes.	https://www.ieee802.org/3/dj/public/23 07/he 3dj 02a 2307.pdf	He	Ran	802.3: Passed by Unanimous Consent
07-2023	11	Move to adopt the FEC_I sublayer architecture with 200G throughput convolutional interleaver as shown in slides 6-11 of he_3dj_01_2307 for 200G/400G/800G/1.6TbE	https://www.ieee802.org/3/dj/public/23 07/he 3dj 01 2307.pdf	Не	Nicholl	802.3: Passed by Unanimous Consent
07-20-2023	1	Move to adopt the 200G/L Die/Device Model changes to Annex 93A (COM) proposed in lim_3dj_01a_2307 slides 6 and 7	https://www.ieee802.org/3/dj/public/23 0720/lim 3dj 01a 2307.pdf	Mike Li	Weaver	802.3: Passed by Unanimous Consent
07-20-2023	3	Move to adopt the 200G/L package model to Annex 93A (COM) proposed in https://www.ieee802.org/3/dj/public/23 07/benartsi 3dj 02 2307.pdf slide 5	https://www.ieee802.org/3/dj/public/23 07/benartsi 3dj 02 2307.pdf	Dudek	Ben-Artsi	802.3: 22 / 5 / 10
09-2023	3	Move to adopt the self-sync method for inner FEC as described in pages 7-11 of he_3dj_01a_2309.	https://www.ieee802.org/3/dj/public/23 09/he 3dj 01a 2309.pdf	Не	Gustlin	802.3: Passed by Unanimous Consent
09-2023	4	Move to adopt the Inner FEC Pad insertion changes of pad block from 384 bits to 1024 bits (8 Inner FEC CWs) and insertion period from 3264 CWs to 8704 CWs, including 8:1 Hamming interleaver protection for pad bits, as shown in rechtman_3dj_01a_2309 slides 5-7 and 10.	https://www.ieee802.org/3/dj/public/23 09/rechtman 3dj 01a 2309.pdf	Rechtman	He	802.3: Passed by Unanimous Consent
09-2023	5	Move to adopt the the CR host and cable assembly insertion loss budget proposed in diminico_3dj_01a_2309, slide 7 for the symmetrical CR use case.	https://www.ieee802.org/3/dj/public/23 09/diminico 3dj 01a 2309.pdf	Diminico	Tracy	802.3: Passed by Unanimous Consent

09-21-2023	1	Move to adopt C2C DER_0 = 0.67E-5 and C2M DER_0 = 2E-5 for the	https://www.ieee802.org/3/dj/public/23 0921/lusted 3dj 01a 230921.pdf	Brown	Li, Mike	802.3: Passed by
		case when the AUI DER_0 is split across the C2M and the C2C inside of				Unanimous Consent
09-21-2023	2	a Type 1 or Type 2 PHY per lusted_3dj_01a_230921, slide 7	https://www.ieee802.org/3/dj/public/23 0921/lusted 3dj 01a 230921.pdf	Proun	Ghiasi	802.3: 46 / 4 / 9
09-21-2023	2	Move to adopt C2M DER_0 = 2E-5 for the case when the AUI is only a C2M (no C2C) inside of a Type 1 or Type 2 PHY per choice A in	nttps://www.leee80z.org/3/dj/public/23 0921/lusted 3dj 01a 230921.pdi	Brown	Gillasi	802.3: 40 / 4 / 9
		lusted_3dj_01a_230921, slide 9				
11-2023	7	Move to adopt the proposal on slide 2 of lusted_3dj_07a_2311	https://www.ieee802.org/3/dj/public/23 11/lusted 3dj 07a 2311.pdf	Ofelt	Dudek	802.3: Passed by
11 2020	•	more to duopt the proposal on shae 2 of fasted_ouj_o/d_2511	meeps, // www.ceebse.org/o/a// passio/25 22/ lasted out o/d 2522.pdf	O.C.I.	Baack	Unanimous Consent
11-2023	8	Move to adopt gustlin_3dj_01_2311 to fill the 802.3dj logic baseline holes that	https://www.ieee802.org/3/dj/public/23 11/gustlin 3dj 01 2311.pdf	Gustlin	Nicholl, Shawn	802.3: Passed by
		were identified in brown_3dj_01_2309				Unanimous Consent
11-2023	9	Move to adopt the two package approach proposed in lusted_3dj_02_2311 slide	https://www.ieee802.org/3/dj/public/23 11/lusted 3dj 02 2311.pdf	Li, Mike	Ben-Artsi	802.3: Passed by
		#4				Unanimous Consent
11-2023	10	Move to adopt the proposed Class A and Class B package parameters in	https://www.ieee802.org/3/dj/public/23 11/lim 3dj 01a 2311.pdf	Li, Mike	Ben-Artsi	802.3: Passed by
		lim_3dj_01a_2311 slides 8-9 for 200G/lane backplane and copper cable PHYs as				Unanimous Consent
		a baseline proposal				
11-2023	11	Move to adopt the host and cable assembly insertion loss budgets proposed in	https://www.ieee802.org/3/dj/public/23 11/tracy 3dj 01a 2311.pdf	Weaver	Noujeim	802.3: Passed by
		the magenta box "proposed baseline content" in tracy_3dj_01a_2311, slide 12,				Unanimous Consent
		for the copper cable objectives. Specific host and cable assembly nomenclature is				
		a TBD.				
11-2023	12	Move to adopt DER_0 = 2e-4 for 200 Gb/s per lane backplane and copper cable		Healey	Heck	802.3: Passed by
		PMD link			_	Unanimous Consent
11-2023	13	Move to adopt the "TP1-TP4 IL" column in the table and MCB insertion loss (2.7	https://www.ieee802.org/3/dj/public/23 11/diminico 3dj 01 2311.pdf	Diminio	Tracy	802.3: Passed by
		dB) on slide 9 of diminico_3dj_01_2311 for 200GBASE-CR1, 400GBASE-CR2,				Unanimous Consent
11 2022	15	800GBASE-CR4 and 1.6TBASE-CR8 PHYs. Move to adopt the 800GBASE-LR4 PMD baseline as shown in	https://www.iccc0002.org/2/di/public/22_11/rodos_2di_01c_2211.pdf	Dadas	Lin	802.3: 78 / 1 / 14
11-2023	15	·	https://www.ieee802.org/3/dj/public/23 11/rodes 3dj 01a 2311.pdf	Rodes	Liu	802.3: 78 / 1 / 14
11-28-2023	1	rodes_3dj_01a_2311 pages 4-9 Move to adopt timeline for IEEE P802.3dj noted on slide #6 of	https://www.ieee802.org/3/dj/public/23 1128/dambrosia 3dj 01b 2311.p	Nowell	Ghiasi	802.3: Passed by
11-28-2023	1	https://www.ieee802.org/3/dj/public/23 1128/dambrosia 3dj 01b 2311.pdf	df	Nowell	Gillasi	Unanimous Consent
01-2024	2	Move to adopt lusted nowell 3dj 01 2401 page 3	https://www.ieee802.org/3/dj/public/24 01/lusted nowell 3dj 01 2401.pd	Lusted	Nowell	802.3: Passed by
01 202 .	_	more to duope dusted_nomen_ody_ot_E for page o	f	Lusteu		Unanimous Consent
01-2024	3	Move to adopt lusted_nowell_3dj_01_2401 page 2	https://www.ieee802.org/3/dj/public/24 01/lusted nowell 3dj 01 2401.pd	Nowell	Brown	802.3: 76 / 13 / 12
			f			, ,
01-2024	5	Move to adopt the 800GBASE-FR4-500 baseline as shown in	https://www.ieee802.org/3/dj/public/24 01/welch 3dj 01a 2401.pdf	Nowell	Lusted	802.3: 68 / 16 / 14
		welch_3dj_01a_2401 pages 10-16				
01-2024	6	Move to adopt the COM Die/Device model parameters in lim_3dj_01_2401 slide	https://www.ieee802.org/3/dj/public/24 01/lim 3dj 01 2401.pdf	Lusted	Nowell	802.3: Passed by
		8 for 200G/Lane KR, CR, AUI chip-to-chip and chip-to-module				Unanimous Consent
01-2024	7	Move to adopt lusted_nowell_3dj_01_2401 page 4	https://www.ieee802.org/3/dj/public/24 01/lusted nowell 3dj 01 2401.pd	Lusted	Nowell	802.3: 58 / 3/ 20
			<u>f</u>			
01-2024	9	Move to adopt lusted_nowell_3dj_01_2401 page 6	https://www.ieee802.org/3/dj/public/24 01/lusted nowell 3dj 01 2401.pd	Lusted	Nowell	802.3: 57 / 5 / 15
01-2024	10	Move to adopt lusted_nowell_3dj_01_2401 page 7	https://www.ieee802.org/3/dj/public/24_01/lusted_nowell_3dj_01_2401.pd	Lusted	Ran	802.3: Passed by
			<u>f</u>			Unanimous Consent
01-2024	11	Move to adopt the 800GBASE-LR1 state diagrams in bruckman_3dj_01a_2401,	https://www.ieee802.org/3/dj/public/24_01/bruckman_3dj_01a_2401.pdf	Bruckman	Maniloff	802.3: Passed by
		slides 4-6 (with values of N and M as TBD)				Unanimous Consent
01-2024	12	Move to adopt the IMDD inner FEC example test vectors in	https://www.ieee802.org/3/dj/public/24_01/levy_3dj_01b_2401.pdf	Brown	He	802.3: Passed by
02 2024		levy_3dj_02a_2401.7z, as described in levy_3dj_01b_2401.	https://www.ieee802.org/3/dj/public/24_01/levy_3dj_02a_2401.7z	14.00		Unanimous Consent
03-2024	2	Move to adopt the following as baselines for the 800GBASE-ER1-20 PHY	https://www.ieee802.org/3/dj/public/24_03/wang_3dj_01a_2403.pdf	Williams	Kareti	802.3: 58 / 9 / 13
		• optical: wang_3dj_01a_2403 pages 7-10	https://www.ieee802.org/3/dj/public/23_07/nicholl_3dj_02a_2307.pdf			
03-2024	2	• logic: nicholl_3dj_02a_2307 Move to amend the adopted 800GBASE-ER1 and 800GBASE-ER1-20	https://www.ieee802.org/3/dj/public/23 07/nicholl 3dj 02a 2307.pdf	Hubor	Shwebi	802 3. Passad by
03-2024	3	logic baselines (nicholl_3dj_02a_2307) based on slides 6-9 of	https://www.ieee802.org/3/di/public/24 03/huber 3di 01a 2403.pdf	Huber	Sluyski	802.3: Passed by Unanimous Consent
		huber 3dj 01a 2403.	inclps.//www.icecouz.org/s/uj/public/24_05/Hubel_5uj_01a_2403.pul_			Onaminous Consent
03-2024	4	Move to amend the 800GBASE-ER1 optical baseline (williams_3dj_01a_2305 pgs	https://www.ieee802.org/3/dj/public/23_05/williams_3dj_01a_2305.pdf	Williams	Kareti	802.3: Passed by
05 2027	-	7-10) per wang 3dj 01a 2403 pages 7-10	https://www.ieee802.org/3/dj/public/23_03/willains_3dj_01a_2303.pdf	***************************************	Nateti	Unanimous Consent
03-2024	5	Move to adopt malicoat 3dj 01a 2403 as the MDI baseline for 400GBASE-DR2	https://www.ieee802.org/3/dj/public/24_03/malicoat_3di_01a_2403.pdf	Malicoat	Stassar	802.3: Passed by
	J	and 400GBASE-DR2-2			2.2300.	Unanimous Consent
03-2024	8	Move to adopt the AUI C2C DER_0 per slide 6 of lusted_3dj_04_2403	https://www.ieee802.org/3/di/public/24 03/lusted 3dj 04 2403.pdf	Heck	Dudek	802.3: 51 / 1 / 27
03-2024	9	Move to adopt the CR MDI connector naming per diminico_3dj_01_2403, slide 4	https://www.ieee802.org/3/dj/public/24 03/diminico 3dj 01 2403.pdf	Diminico	Kocsis	802.3: 58 / 5 / 16
03-2024	11	Move to adopt the proposal for automatic polarity detection and correction in	https://www.ieee802.org/3/dj/public/24 03/ran 3dj 01a 2403.pdf	Ran	HEck	802.3: Passed by
		the start-up protocol, per ran_3dj_01a_2403				Unanimous Consent
03-2024	12	Move to adopt the proposal for training pattern changes in the start-up protocol,	https://www.ieee802.org/3/dj/public/24_03/ran_3dj_03a_2403.pdf	Ran	Brown	802.3: 60 / 1 / 22
		per ran_3dj_03a_2403				

03-2024	13	Move to adopt the start-up protocol to enable segment-by-segment training per ran_3dj_04_2403 slides 3-4,8-14 and ran_3dj_05a_2403 slides 2-9 as a modification to the PMD control function adopted by motion #10 in January 202-	https://www.ieee802.org/3/dj/public/24_03/ran_3dj_05a_2403.pdf	Ran	Dudek	802.3: Passed by Unanimous Consent
		(2nd item on slide 7 of	f			
		https://www.ieee802.org/3/dj/public/24_01/lusted_nowell_3dj_01_2401.pdf)				
03-2024	14	Move to adopt:	https://www.ieee802.org/3/dj/public/24 03/ghiasi 3dj 01a 2403.pdf	Ghiasi	Maniloff	802.3: 43 / 1 / 31
		CRU text per ghiasi_3dj_01a_2403 page 10 with 4 MHz CRU for 200GBASE-DR1,				
		400GBASE-DR2, 800GBASE-DR4, 1.6TBASE-DR8, 800GBASE-FR4-500				
		CRU text per ghiasi_3dj_01a_2403 page 11 with 4 MHz CRU for all backplane and				
		Cu cable PMDs				
		CRU text per ghiasi_3dj_01a_2403 page 13 with 4 MHz CRU for 200GBASE-FR1,				
		400GBASE-DR2-2, 800GBASE-DR4-2, 1.6TBASE-DR8-2, 800GBASE-FR4, 800GBASE	-			
		LD4				