

oFEC Codeword Error Marking

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FlexO-xe to OFEC adaptation

The fundamental block size of oFEC is 3552bits. At 800G there are actually 256 blocks that constitute 116×10280 b of FlexO-xe -like framed data. The payload of the FlexO-xe frame contains GMP mapped Ethernet (mapped as 257b blocks which are 128b interleaved to the FlexO-xe. A CRC32 is added to every 4 x 10280b rows. This CRC protects against false negative errors passing through the FEC decoder. If the FEC indicates a UCB the block is corrupted and the CRC would fail. If the FEC unknowingly passes a bad block the CRC32 is meant to catch that. The PCS block is responsible to generate the VE block errors to the host based on CRC32.

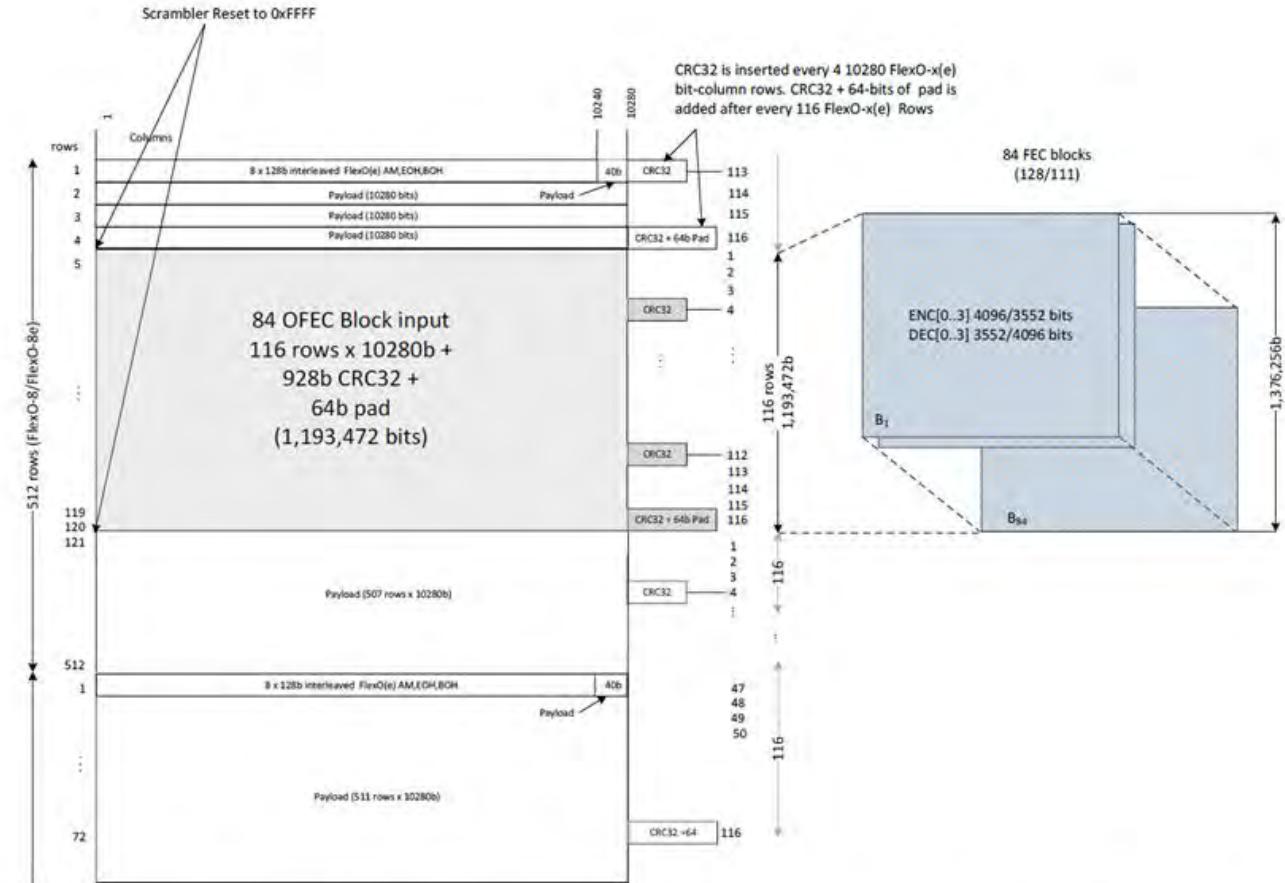


Figure 13: $116 \times 10,280$ bit-column row FlexO-8(e) adaptation to OFCBG84

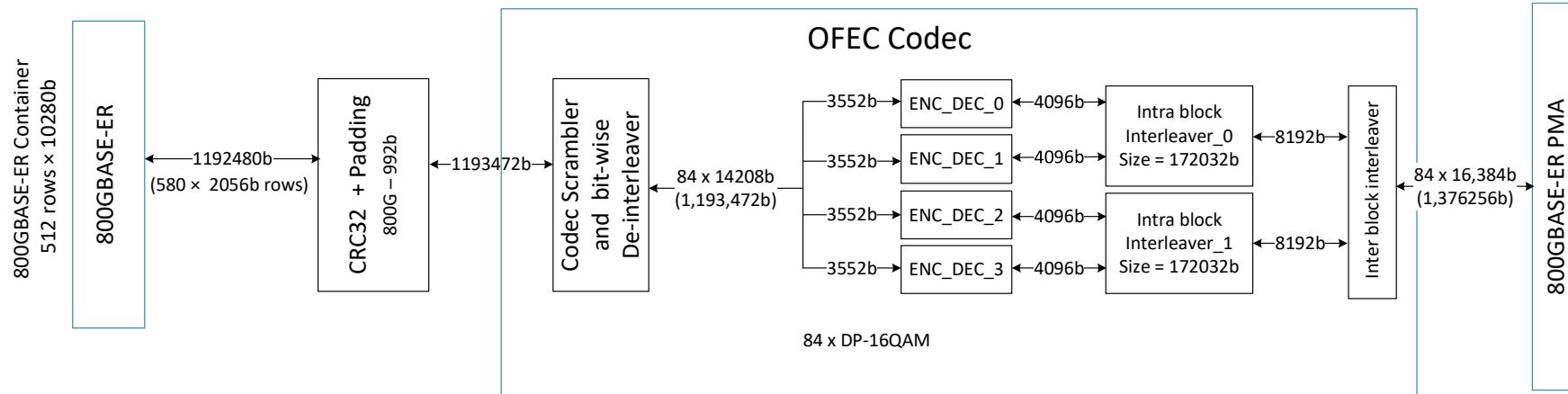
Summary

- CRC size is 41 120 bits.
- On average 40 832 bits are MAC data bits
- Target FLR is 6E-11.
- Based on numbers above CRC block error ratio is expected to be less than 5.903E-11.
- The CRC block is deinterleaved across 84 FEC codewords the oFEC codeword error ratio is 84x smaller or 7.027E-13.
- Conversion between FLR to block error ratio is:
- $\text{FLR} = \text{BlockErrorRatio} * (1 + \text{NumberOfBitsPerEthernetFrame}/\text{NumberofDataBitsPerBlock})$

Backup

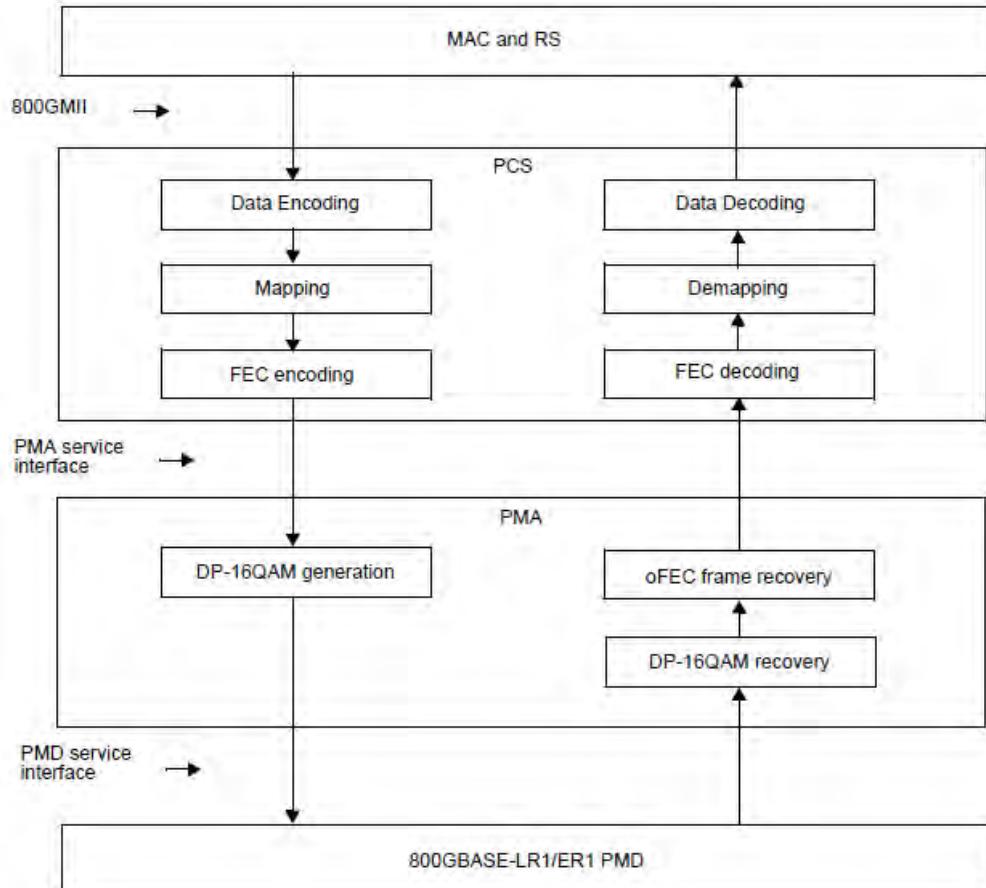
- From nicholl_3dj_01a_230630

PCS - oFEC encoder/interleaver/merge



- The oFEC block includes a scrambler which is reset at the beginning every 580 x 2056b rows of information bits.
- The oFEC block is organized as 4 oFEC encode/decoders (ENC_DEC_[0..3]) followed by two Intra block interleavers (Intra_block [0..1]) and an inter-block interleaver. These functions operate in parallel to produce an oFEC codeword.
- A codeword is a semi-infinite set of bits organized in a matrix with a semi-infinite number of rows and N columns (N=128).
- 84 oFEC codec blocks are ratio locked and aligned to the media-side DSP super frame.
- The interleaver structure is organized as an (84,8) array of 16b x 16b square blocks and contains two mechanisms:
- An intra-block interleaver (170,032b) reorders the bits in each 16b x 16b square block to ensure that the bits in each row and column of a square block at the encoder output are remapped uniformly in the square block for transmission.
- An inter-block interleaver ensures that nearby symbols on the link contain bits that are widely separated from the encoder output.
- The oFEC codec block consumes 1,193,472b and produces 1,376,256b of data and parity, (128/111) expansion ratio

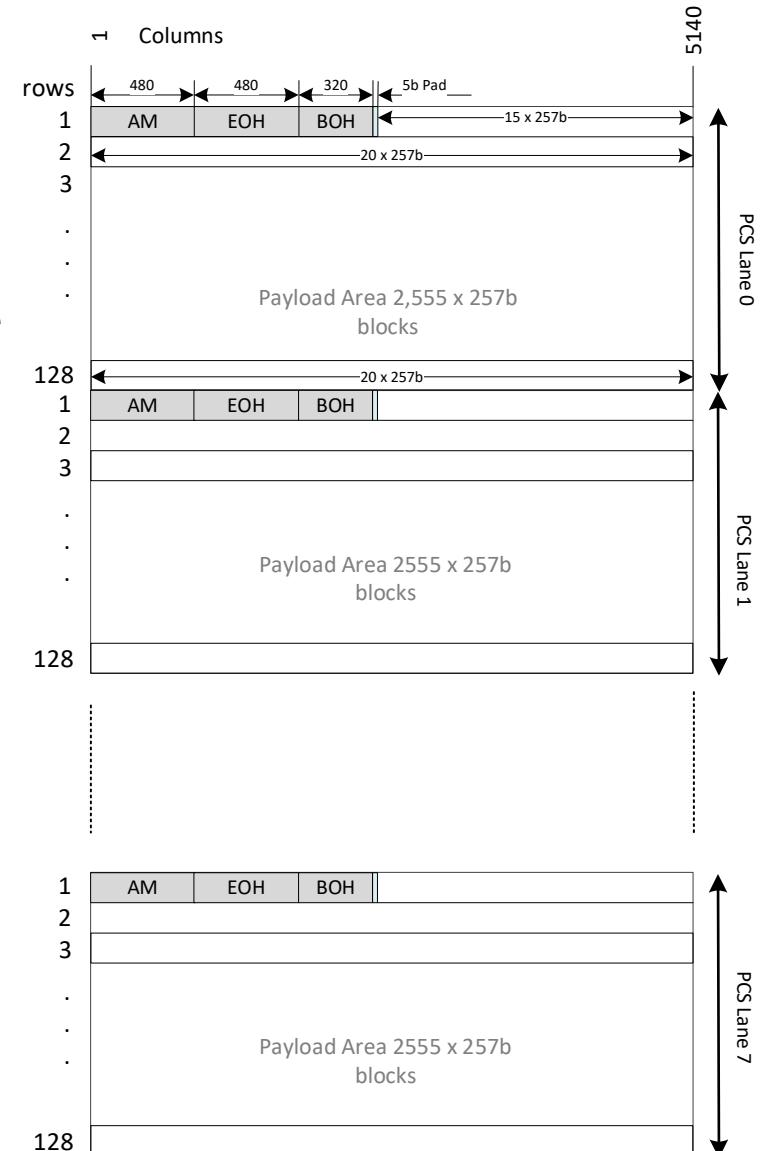
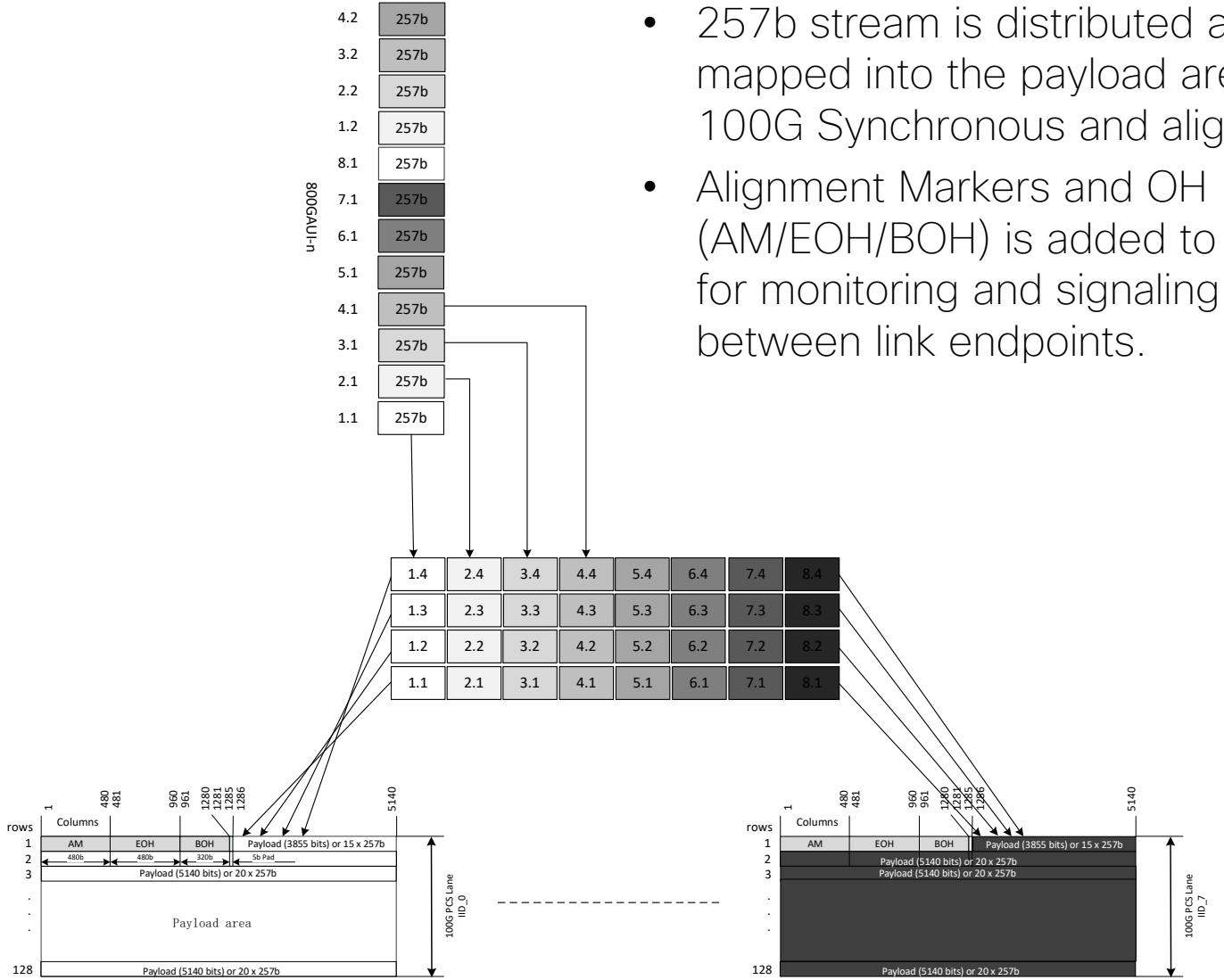
800GBASE-ER1 PHY Overview



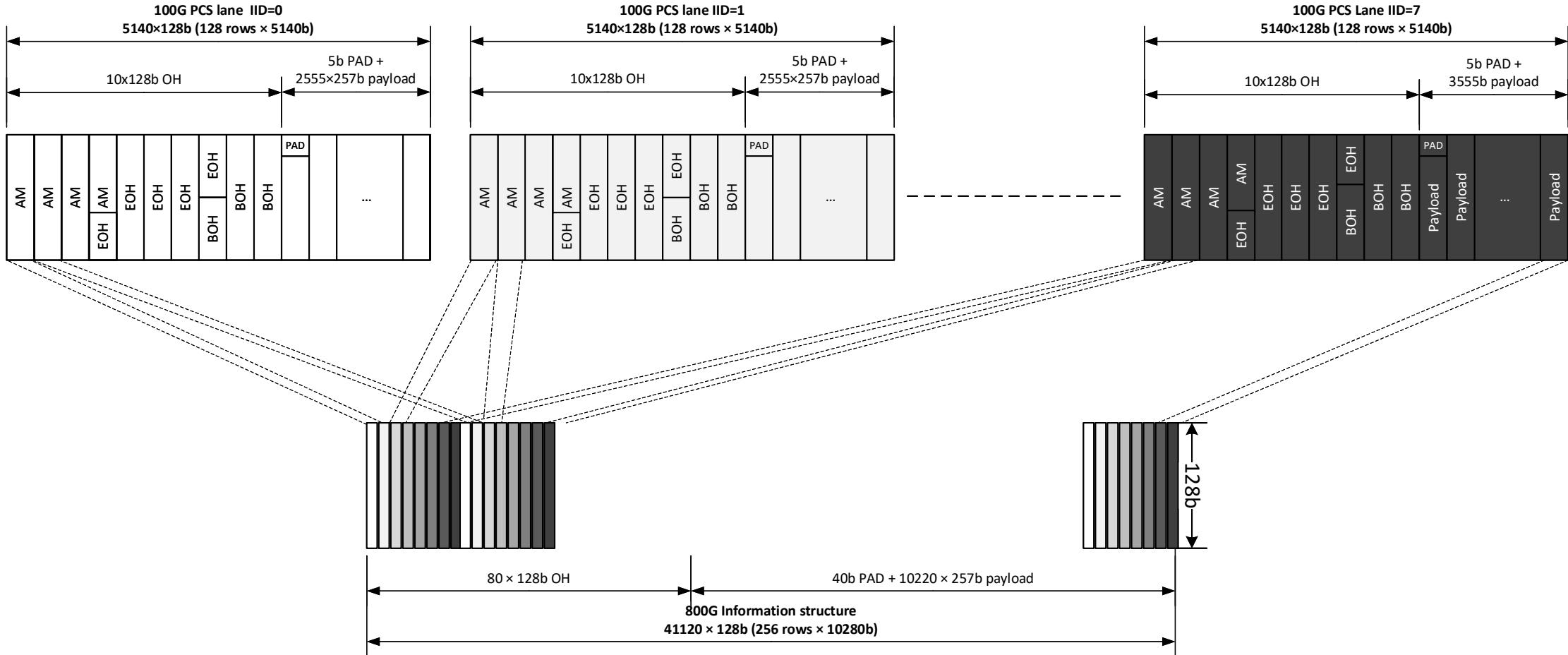
- Builds upon the efforts in 802.3cw to define an 802.3 PHY documentation structure to support a coherent optical interface
 - Split of functionality between PCS, PMA and PMD
 - Definition of PMA and PMD services interfaces
- PCS
 - 256/257b data encoding/decoding
 - GMP mapping/demapping
 - FEC encoding/decoding
 - based on oFEC defined for 800ZR/ZR+
- PMA
 - DP-16QAM generation/recovery

PCS - 257b distribution & GMP mapping

- 257b stream is distributed and GMP mapped into the payload area of 8 x 100G Synchronous and aligned lanes
- Alignment Markers and OH (AM/EOH/BOH) is added to each lane for monitoring and signaling purposes between link endpoints.

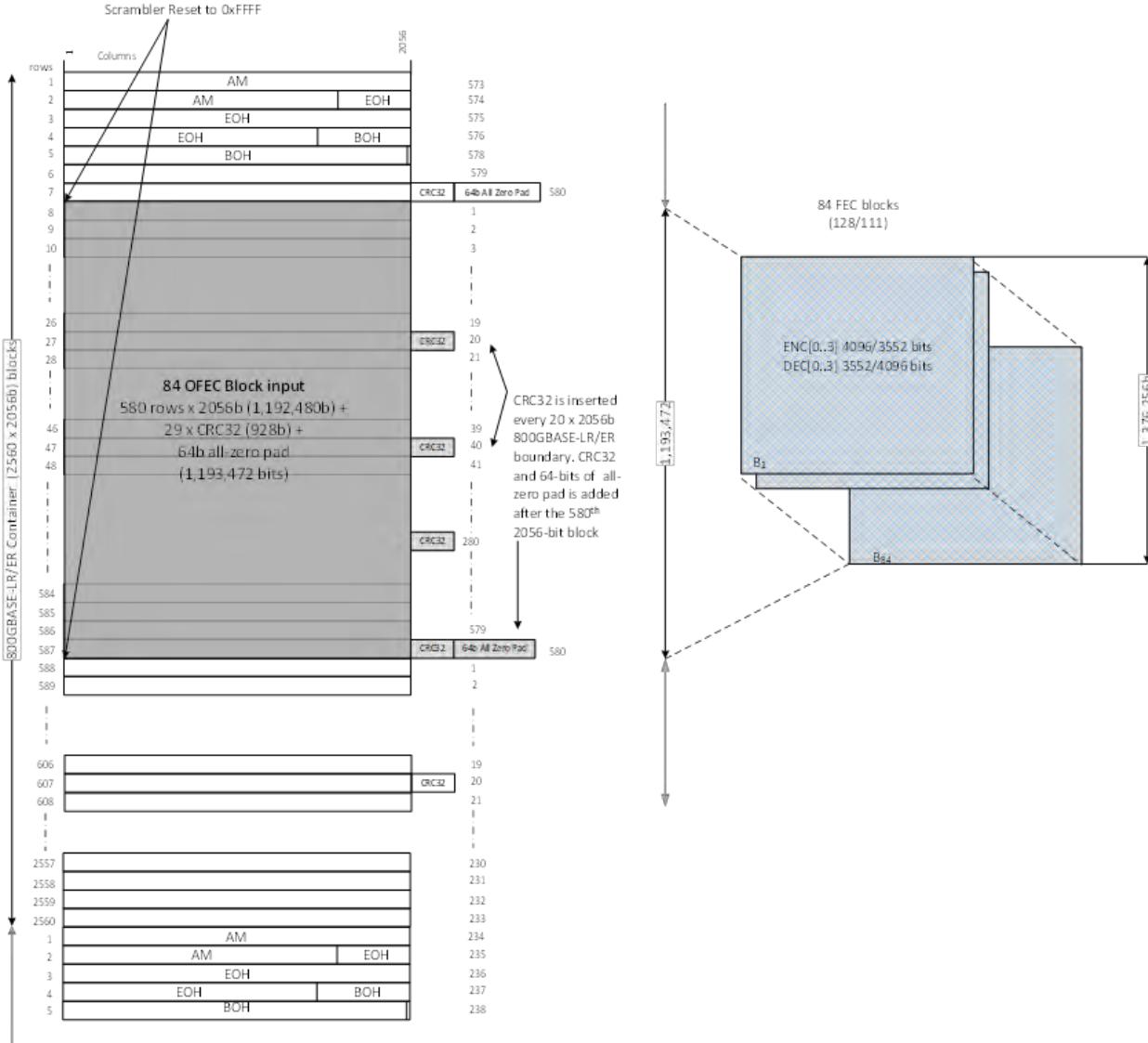


PCS - 128b Interleaving



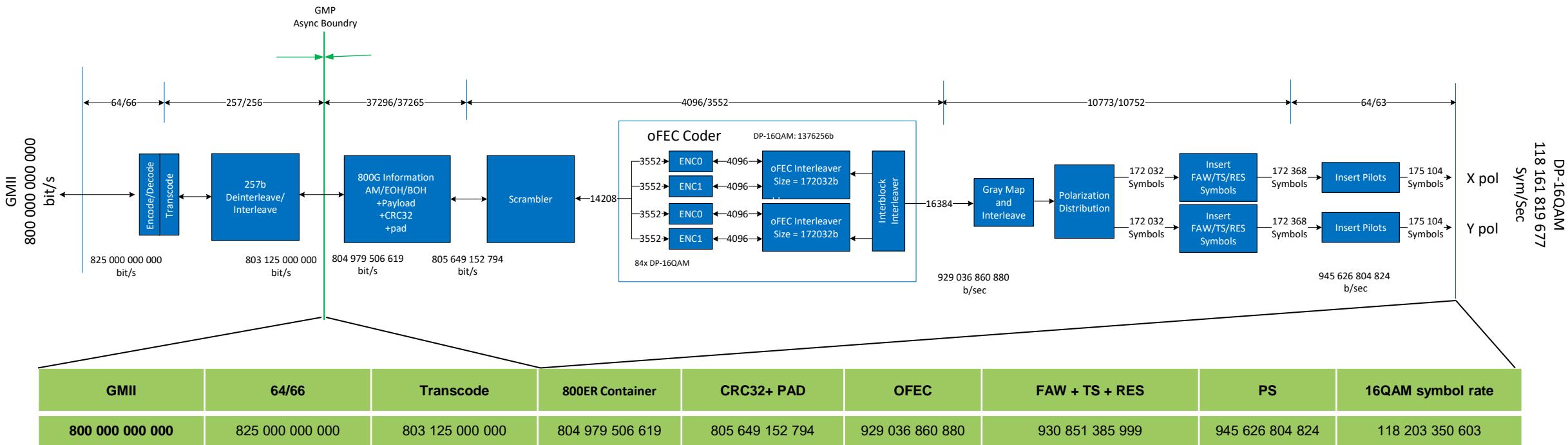
8 x 100G lanes are 128b interleaved to an 800G structure

PCS - 800G structure adapted to oFEC



- The 800G structure at the output of the 128b interleaver can be redrawn as 2560 rows x 2056b (5,263,360b) total.
- 580 x 2056b rows + 29 x CRC32 + 64-bits of pad align to 84 oFEC blocks (1,193,472b)
- A CRC32 is generated covering every 20 x 2056b rows to ensure MTTFPA.
- 84 oFEC blocks correspond to a symbol based optical frame (DSP Superframe).
- The oFEC block includes a scrambler which is reset at the beginning every 580 x 2056b rows of information bits.
- The oFEC blocks produce 1,376,256b of data + parity to the PMA.

Data rates overview



800GBASE-ER1 = DP-16QAM @ 118.203350603 GSym/Sec

OIF 800ZR and ITU-T FlexO-8e = DP-16QAM @ 118.203350603 GSym/Sec (Interoperable).