ACT/GMSLE Training Frame and Training Sequence

Contribution to 802.3dm Task Force

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Introduction

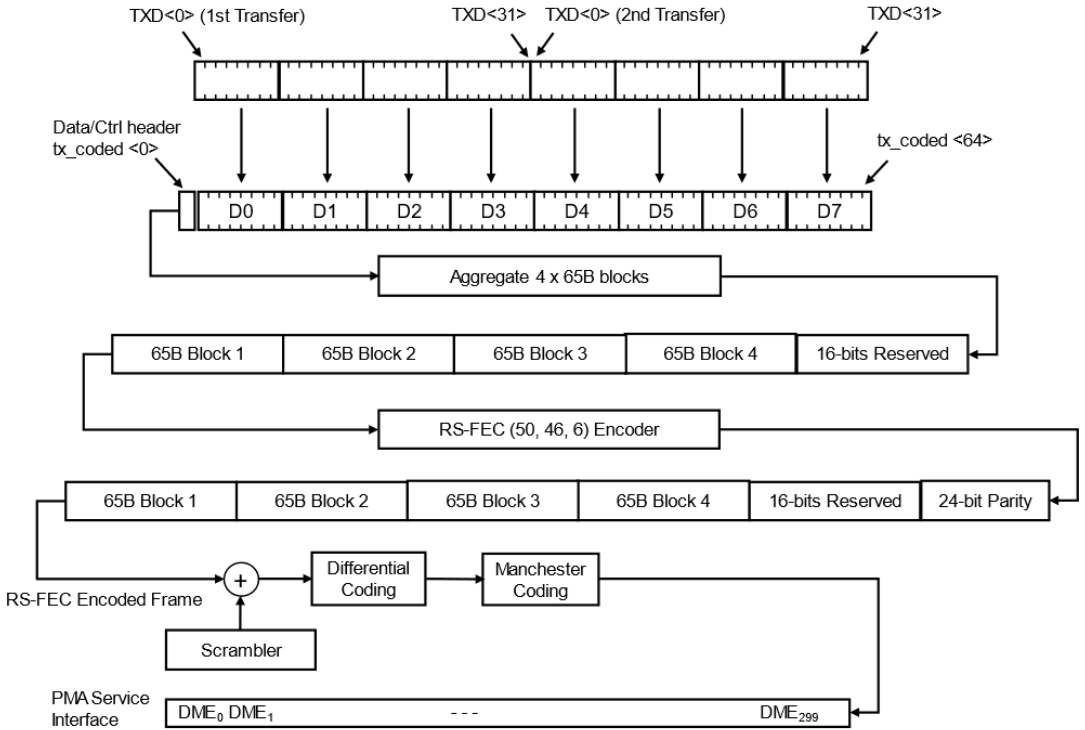
- This presentation proposes an updated frame structure for the 100M ACT/GMSLE training frame
- The new frame structure is based on the 100M ACT/GMSLE data mode FEC frame structure
- Main objectives:
  - Simplify the implementation of training frame, by reusing data mode functionality where possible
  - Simplify the training state machines, including transition from SEND_T to SEND_N

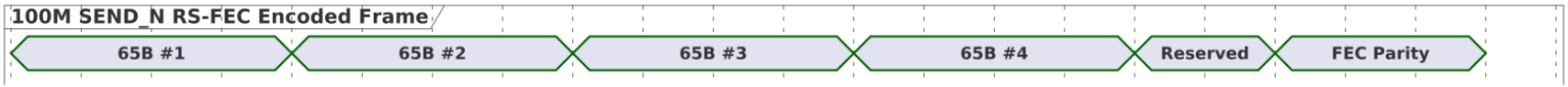
Background

The ACT/GMSLE compromise text proposal has 300-bit FEC frames with:

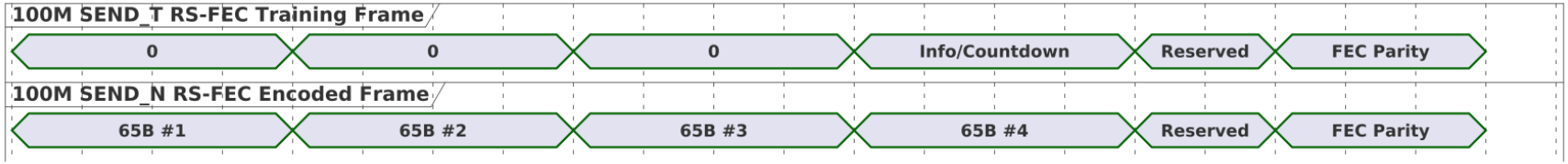
- RS-FEC(50,46,6) encoding
- 260-bits for 4 x 64B/65B blocks
- 16-bits reserved for OAM, etc.
- 24-bits for FEC parity

This presentation proposes to use the same structure as basis for the 100M training frame





100M Training Frame Proposal



The new SEND_T frame format proposal is to use the SEND_N frame structure for the SEND_T frame, with the following structure:

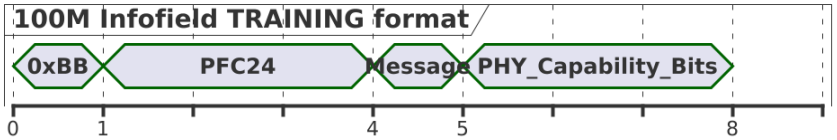
- The first three 64B/65B blocks hold all zero data blocks
- The fourth 64B/65B blocks holds new 64B/65B control block containing the Infofield

100M Infofield Proposal

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

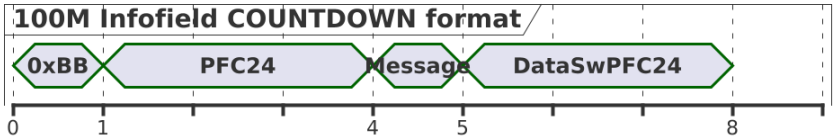
Figure 149–27—Infofield TRAINING format



PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 149–28—Infofield COUNTDOWN format



The 100M Infofield is the same as for 802.3ch, except that Octets 2, 3, 11, and 12 have been dropped.

The CRC16 can be eliminated because the frame has RS-FEC error correction.

NOTE: The PFC24 field may not be needed for the 100M direction

Infofield Message and PHY Capability

The message field can be the same as used in 802.3ch

The PHY capability field can be same as in 802.3ch, with the appropriate capability set

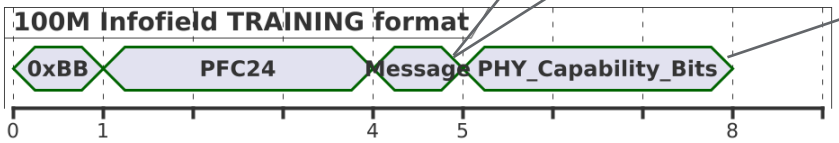


Table 149–10—Infofield message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 149–11—Infofield message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 149–12—PHY capability bits

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData																Reserved	InterleaverDepth		PrecodeSel		SlowWakeRequest	EEEen	OAMen

Infofield 64B/65B Block

The training frame Infofield is encoded as 64B/65B block, with distinct encoding (see yellow line at the bottom of the table on the right)

The Infofield encoding is

- PFC24: I0, I1, I2
- Message: I3
- PHY_Capability_Bits: I4, I5, I6

Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	
$I_0\ I_1\ I_2\ I_3\ I_4\ I_5\ I_6$	1	0xBB	I_0	I_1	I_2	I_3	I_4	I_5	I_6

NOTE: The PFC24 field may not be needed for the 100M direction

PHY Control State Diagram

For the Multi-Gig direction, the training sequence can follow 802.3ch Figure 149-32

For the 100M direction the training sequence can be simplified as shown in the state diagram on the right

Because the training frame has the same structure as the data mode frame, switching from training to data mode only requires changing the frame payload

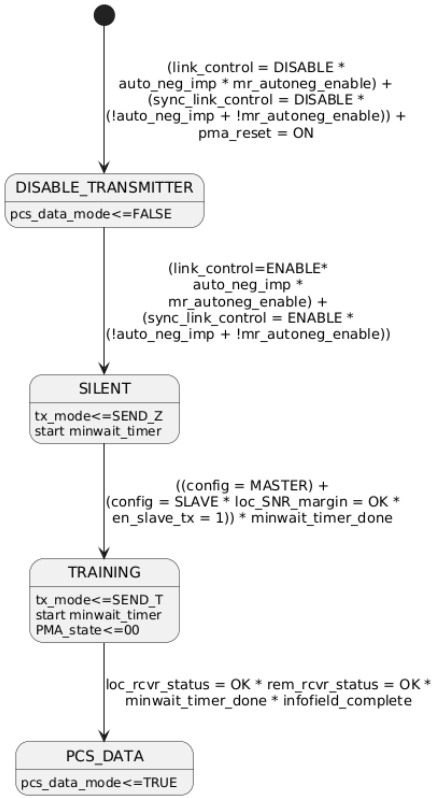


Figure: 100M PHY Control state diagram

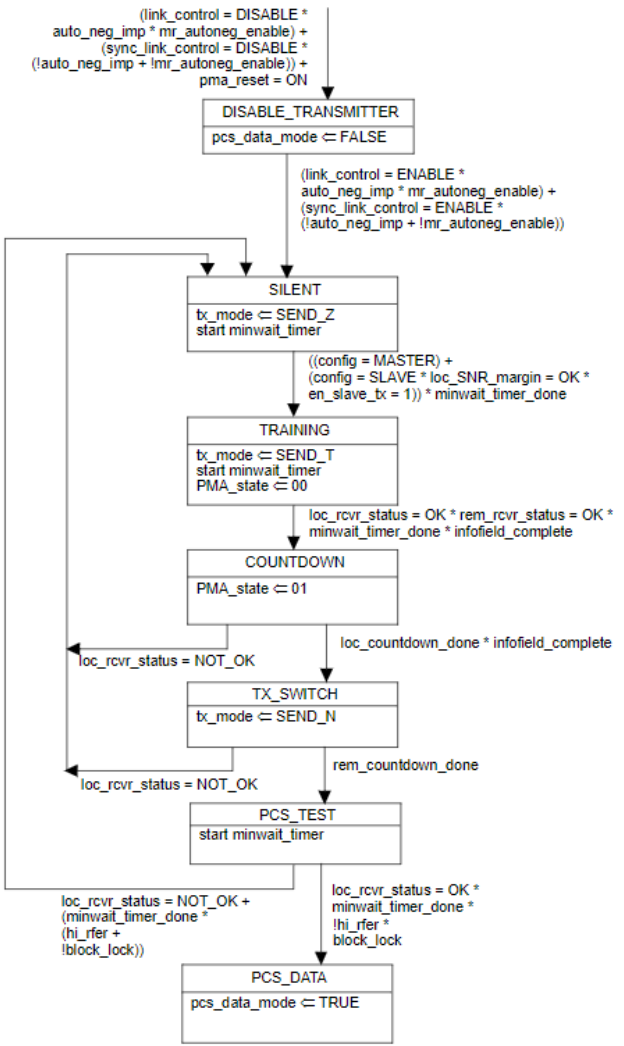


Figure 149–32—PHY Control state diagram

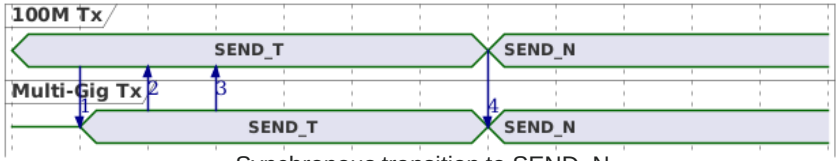
Status Bits

There are three status bits exchanged in the Infofield Message (two in each direction):

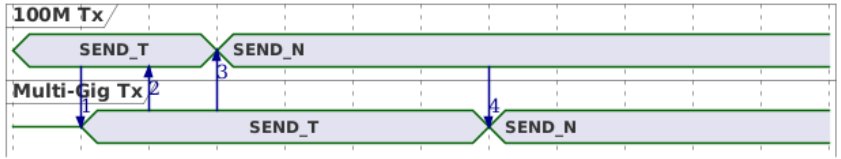
- loc_rcvr_status
- en_slave_tx
- timing_lock_OK

The status bits are used to control the state transitions in the training sequence (see figure on the right).

In 802.3ch the transition to SEND_N is synchronous, but it is also possible to use asynchronous transition to SEND_N, if it brings any benefit



Synchronous transition to SEND_N



Asynchronous transition to SEND_N

Typical signaling sequence:

1. en_slave_tx = 1
2. timing_lock_OK = 1
3. loc_rcvr_status = OK (for 100M)
4. loc_rcvr_status = OK (for Multi-Gig)

Conclusion

- This presentation proposes an updated frame structure for the 100M ACT/GMSLE training frame
- The new training frame structure simplifies the implementation of training frame, by reusing the data mode frame structure
- The new training frame structure simplifies the implementation of the transition from SEND_T to SEND_N
- The simplicity of the proposed training frame can both simplify camera PHY implementation and enhance interoperability

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