Baseline Text Proposal for TDD Based 802.3dm PHY

Wei Lou, Ahmad Chini, Mehmet Tazebay
Broadcom Corp.

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Contributors and Supporters

- Ching-Yen Lee -- RealTek
- Claude Gauthier -- NXP
- Frank Wang -- RealTek
- Kamal Dalmia -- Aviva Links
- Korhan Tanc -- NXP
- Ramanjit Ahuja -- OnSemi
- Sachin Goel -- Aviva Links
- Scott Muma -- Microchip
- Tiaq Ng -- Aviva Links
- Yao-Chun Chuang -- RealTek

Introduction

- This presentation provides a highlight of the initial draft proposal of texts and block diagrams to *802.3dm* Service Primitive/Interface, PCS and PMA clauses and subclauses, based on TDD operational mode presented in
  - January meeting **https://www.ieee802.org/3/dm/public/0125/Chini_3dm_01a_0125.pdf**
  - March meeting https://www.ieee802.org/3/dm/public/0325/Chini_3dm_01a_0325.pdf

- In the latest *IEEE P802.3dm/D0.4* draft text (https://www.ieee802.org/3/dm/private/drafts/P802dm_D0p4.pdf), the multiG+100MBASE-T1/V1 PHY and 100M+multiGBASE-T1/V1 have separate Clauses for Service Primitive/Interface, PCS and PMA. Due to the similarities between the two types of PHY in TDD operation, we combine their Service Primitive/Interface into *Clause 200.2*, their PCS into *Clause 200.4*, and their PMA into *Clause 200.6*. We still keep Clause number of *200.3*, *200.5* and *200.7*, to be consistent with Clause naming convention of D0.4 draft. Those Clauses could be removed in the final specification.

- We referenced heavily to *Clause 149* due to the many similarities between *802.3dm* and *802.3ch*, and we highlighted the major changes from *802.3ch*. For the Clauses/Subclauses yet to be finalized, we designate as TBD.

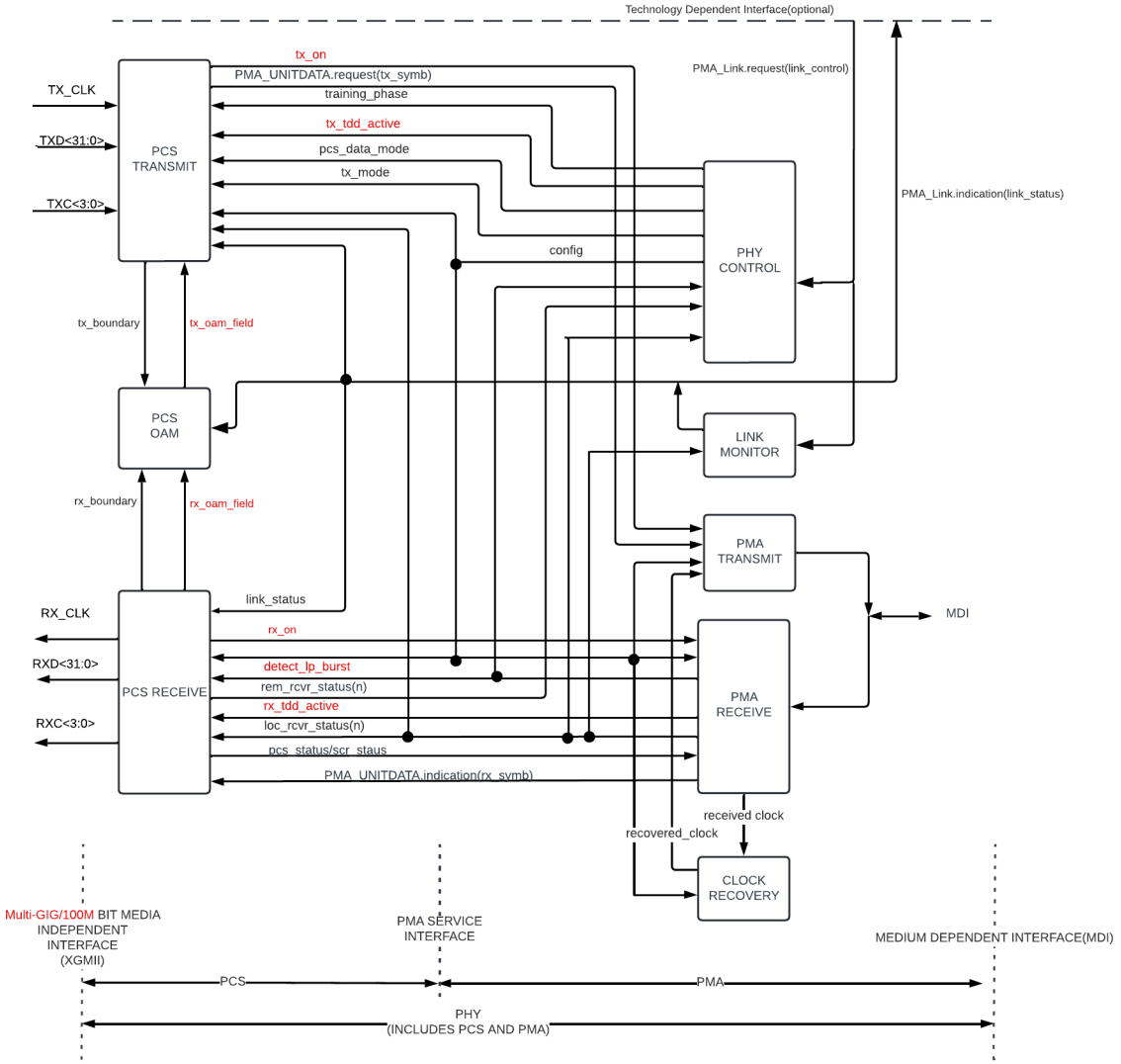
- In the asymmetric image sensor application, we assume the 100M+MultiGBASE-T1/V1 PHY is the MASTER, and MultiG+100MBASE-T1/V1 PHY is the SLAVE. To accommodate different applications, MASTER and SLAVE designation can be reversed. Some related parameters should be redefined in that case.

- The detailed draft proposal can be found in a separate document at: *Baseline_Text_for_TDD_PHY_V1_050925.pdf*

200.1 Overview (TBD)

- **200.1.1 Nomenclature (TBD)**
- **200.1.2 PHY/PMD types (TBD)**
- **200.1.3 Relationship of MultiG+100M/100M+MultiGBASE-T1/V1 to other standards (TBD)**
  - Figure 200-2 is modified from Figure 149-2, to support TDD duplex mode of operation
- **200.1.4 Operation of MultiG+100M/100M+MultiGBASE-T1/V1 (TBD)**
  - **200.1.4.1 Physical Coding Sublayer(PCS), MultiG+100MBASE-T1/V1**
  - **200.1.4.2 Physical Coding Sublayer(PCS), 100M+MultiGBASE-T1/V1**
  - **200.1.4.3 Physical Medium Attachment(PMA) sublayer, MultiG+100MBASE-T1/V1**
  - **200.1.4.4 Physical Medium Attachment(PMA) sublayer, 100M+MultiGBASE-T1/V1**
- **200.1.5 Signaling, ~~MultiG+100MBASE-T1/V1~~**
- **200.1.6 ~~Signalling, 100M+MultiGBASE-T1/V1~~**
- **200.1.7 Interfaces (TBD)**
- **200.1.8 Conventions in this clause (TBD)**

Figure 200-2 Functional Block Diagram



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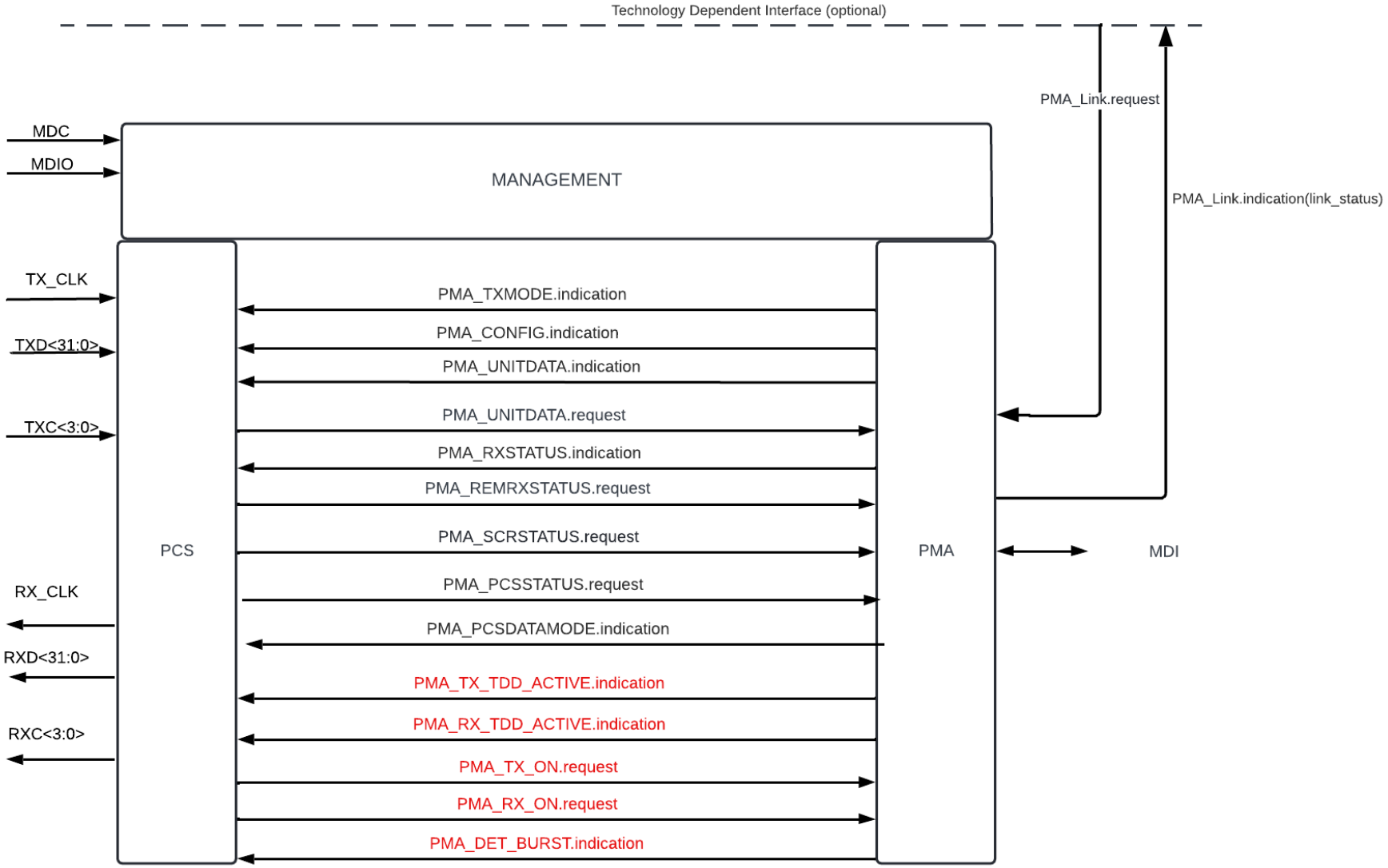
200.2 (MultiG+100M/100M+MultiGBASE-T1/V1) Service Primitives and Interfaces

- **200.2.1 Technology Dependent Interface**
  - 200.2.1.1 PMA_LINK.request (link_control)
  - 200.2.1.2 PMA_LINK.indication(link_status)
- **200.2.2 PMA service interface**

  Five new service primitives are added to support TDD operation. EEE related service primitives are removed. Some other service primitive definitions have been changed from Clause 149.2.2. Figure 200-3 is modified from Figure 149-3.

  - 200.2.2.1 PMA_TXMODE.indication (tx_mode)
  - 200.2.2.2 PMA_CONFIG.indication (config)
  - 200.2.2.3 PMA_UNITDATA.request (tx_symb)
  - 200.2.2.4 PMA_UNITDATA.indication (rx_symb)
  - 200.2.2.5 PMA_SCRSTATUS.request(scr_status)
  - 200.2.2.6 PMA_PCS_STATUS.request (pcs_status)
  - 200.2.2.7 PMA_RXSTATUS.indication (loc_rcvr_status)
  - 200.2.2.8 PMA_REMRXSTATUS.request (rem_rcvr_status)
  - 200.2.2.9 PMA_PCSDATAMODE.indication (pcs_data_mode)
  - 200.2.2.10 PMA_TX_TDD_ACTIVE.indication (tx_tdd_active) (Added)
  - 200.2.2.11 PMA_RX_TDD_ACTIVE.indication (rx_tdd_active) (Added)
  - 200.2.2.12 PMA_TX_ON.request (tx_on) (Added)
  - 200.2.2.13 PMA_RX_ON.request (rx_on) (Added)
  - 200.2.2.14 PMA_DET_BURST.indication(detect_lp_burst) (Added)

Figure 200-3 MultiG+100M/100M+MultiGBASE-T1/V1 service interface



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PMA service interface (PMA_TXMODE)

- **200.2.2.1 PMA_TXMODE.indication**

  The transmitter in an 802.3 dm link normally sends over the MDI symbols that represent XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

  – **Semantics of the primitive**

    PMA_TXMODE.indication(tx_mode)

    PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values of the form:

    – SEND_N: This value is continuously asserted during transmission of sequences of symbols representing a (XGMII?) data stream in the data mode.
    – SEND_TS: This value is continuously asserted in case transmission of sequences of symbols representing the TDD symmetric training mode is to take place. MASTER and SLAVE send 3Gsps baud rate with PAM2 TDD training frames.
    – SEND_TA: This value is continuously asserted in case transmission of sequences of symbols representing the TDD asymmetric training mode is to take place. Master send 3Gsps baud rate with PAM2 TDD training frames. SLAVE send target baud rate of 3Gsps or 6Gsps with PAM2 TDD training frames
    – SEND_TA_EXT: This value is continuously asserted in case transmission of sequences of symbols representing the TDD asymmetric extended training mode is to take place for SLAVE baud rate of 6Gsps and PAM2/PAM4 modulation. MASTER baud rate is 3Gsps and PAM2 Modulation.
    – SEND_Z: This value is continuously asserted in case transmission of zero symbols is required

200.3 (100M+MULTIGBASE-T1/V1) Service Primitives and Interfaces, low speed channel

- **As specified in clause 200.2 (could be removed in the final specification)**

200.4 Physical Coding Sublayer(PCS) functions

- **200.4.1 PCS service interface(XGMII)**

  Modified from Clause 149.3.1

- **200.4.2 PCS functions**

  Modified from Clause 149.3.2. Figure 200-4 is modified from Figure 149-4, to support TDD operation.

  - **200.4.2.1 PCS Reset Function**

    Modified from Clause 149.3.2.1

  - **200.4.2.2 PCS Transmit Function**

    Modified from Clause 149.3.2.2. Figure 200-5 is modified from Figure 194-5, to support newly proposed TDD training frame generation in PAM2 and PAM4

    - **200.4.2.2.1** Modified from Clause 149.3.2.2.1
    - **200.4.2.2.2** Figure 200-6-1, 200-6-2 are modified from Figure 194-6, for MASTER and SLAVE transmit bit ordering. Figure 200-7-1, 200-7-2 are modified from Figure 194-7 for MASTER and SLACE receive bit ordering.
    - **200.4.2.2.3- 200.4.2.2.4** As specified for MulitGBASE-T1 PHY is 149.3.2.2.3 – 149.3.2.2.4
    - **200.4.2.2.5** Modified from 149.3.2.2.5 to remove EEE/LPI related control codes. Table 200-2 is modified from Table 149-2, to remove LPI control codes
    - **200.4.2.2.6-200.4.2.2.7** As specified for MulitGBASE-T1 PHY in 149.3.2.2.6-149.3.2.2.7
    - ~~**200.4.2.2.8**~~ REMOVED, as no EEE mode is defined
    - **200.4.2.2.9- 200.4.2.2.12** As specified for MultiGBASE-T1 PHY in 149.3.2.2.9-149.3.2.2.12
    - **200.4.2.2.13** Modified from 149.3.2.2.13
    - **200.4.2.2.14 – 200. 4.2.2.18** Modified from 149.3.2.2.14-149.3.2.2.18
    - **200.4.2.2.19** As specified for MultiGBASE-T1 PHY in 149.3.2.2.19
    - **200.4.2.2.20** Precoder(TBD)
    - **200.4.2.2.21** As specified for MultiGBASE-T1 PHY in 149.3.2.2.21
    - **200.4.2.2.22** Removed EEE section. Replaced with subclause for PAM2 mapping

  - **200.4.2.3 PCS Receive Function**

    Modified from Clause 149.3.2.3

    - **200.4.2.3.1** Modified from 149.3.2.3.1
    - **200.4.2.3.2 – 200.4.2.3.3** As specified for MultiGBASE-T1 PHY in 149.3.2.3.2-149.3.2.3.3

200.4 Physical Coding Sublayer(PCS) functions

- **200.4.3 Test-pattern generators**

  Modified from Clause 149.3.3

- **200.4.4 Side-stream scrambler polynomials**

  Modified from Clause 149.3.4, to support TDD operation

- **200.4.5 PMA training frame**

  Modified from Clause 149.3.5 to support TDD operation

- **200.4.6 PCS TDD signaling**

  Replaced 149.3.6 LPI signaling with 200.4.6 TDD Signaling

- **200.4.7 PCS Detailed functions and state diagrams**

  Modified from Clause 149.3.7

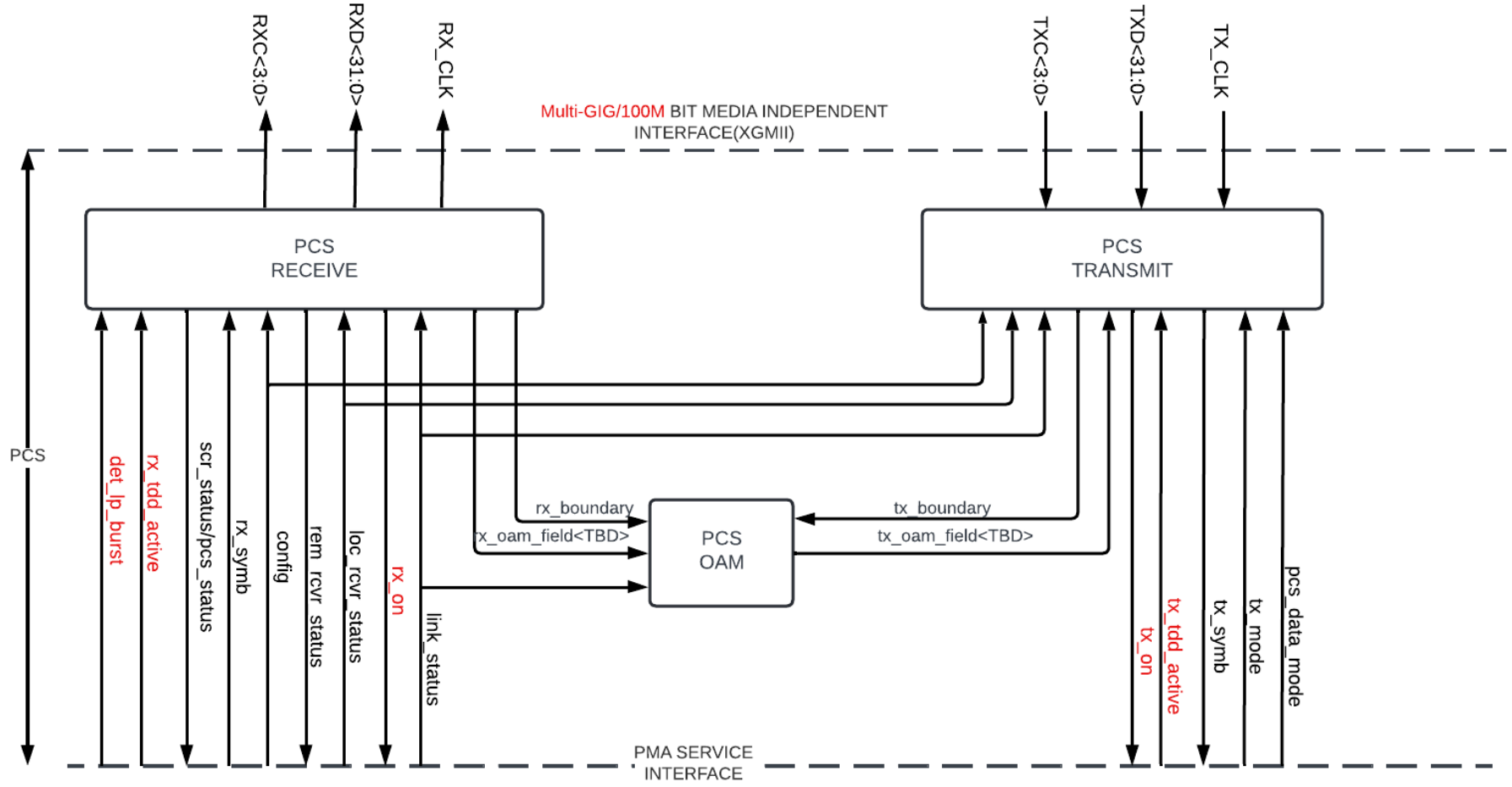
- **200.4.8 PCS management**

  Modified from Clause 149.3.8

- **200.4.9 Operations, Administration, and Maintenance(OAM) --TBD**

200.4.2 PCS Functions

- **Figure 200-4 PCS reference diagram**



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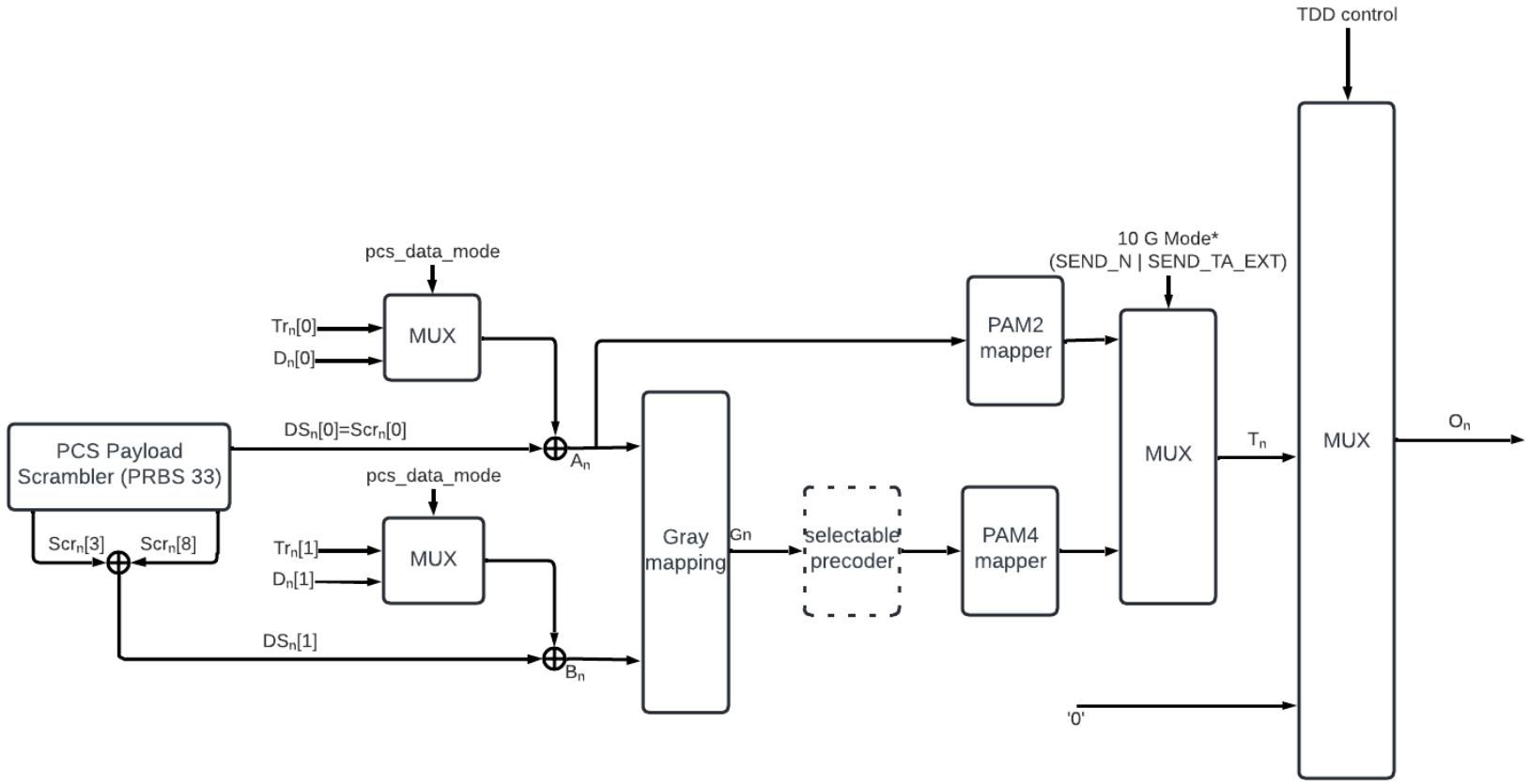
200.4.2.2 PCS Transmit Function

- **Figure 200-5 PCS Transmit Function block diagram**



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200.4.2.2 PCS Transmit Function

- The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 200-16, and to the PCS Transmit bit ordering in Figure 200-6-1 and Figure 200-6-2

- Dashed rectangles in Figure 200-6-2 and Figure 200-7-1 are used to indicate data path of PAM2 or PAM4 signals. Only one of them shall be chosen for a particular operational speed mode. Dashed rectangles in Figure 200-16 should be removed from final standard as it is related to EEE operation.

- For 100M+MultiGBASE-T1/V1 PHY (MASTER), after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take 1 group of 15 65B blocks and append a 17-bit OAM field to it, shown in Figure 200-6-1. This forms the input to an (130,124) RS-FEC which adds 48 parity bits. The resulting 1040 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. Transmit data-units are sent to the PMA service interface via the PMA UNITDATA.request primitive.

- For MultiG+100MBASE-T1/V1 PHY(SLAVE), after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take L groups of 15 65B blocks and append a 1-bit OAM field to each group. This forms the input to an L-interleaved (130,122) RS-FEC superframe which adds L × 64 parity bits, shown in Figure 200-6-2. 25 such superframes are formed for one data payload. L=1 for 2.5Gbps and L=2 for 5Gbps. For 2.5Gbps and 5Gbps PAM2 transmission, the resulting L × 1040 x 25 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. L=4 for 10Gbps PAM4 transmission. The resulting L × 1040 x 25 bits are then scrambled. These bits are then mapped, two at a time, into a PAM4 symbol. the transmit data-units are sent to the PMA service interface via the PMA UNITDATA.request primitive.

- In each symbol period, when communicating with the PMA, the PCS Transmit generates a PAM2 or PAM4 symbol that is transferred to the PMA via the PMA UNITDATA request primitive.

- The operation of the PCS Transmit function is controlled by the PMA TXMODE indication message received from the PMA PHY Control function.

  - If a PMA TXMODE.indication message has the value SEND_TS, SEND_TA, or SEND_TA_EXT, PCS Transmit shall generate a sequence (O_n,) defined in 200.4.5.4 to the PMA via the PMA UNITDATA.request primitive.

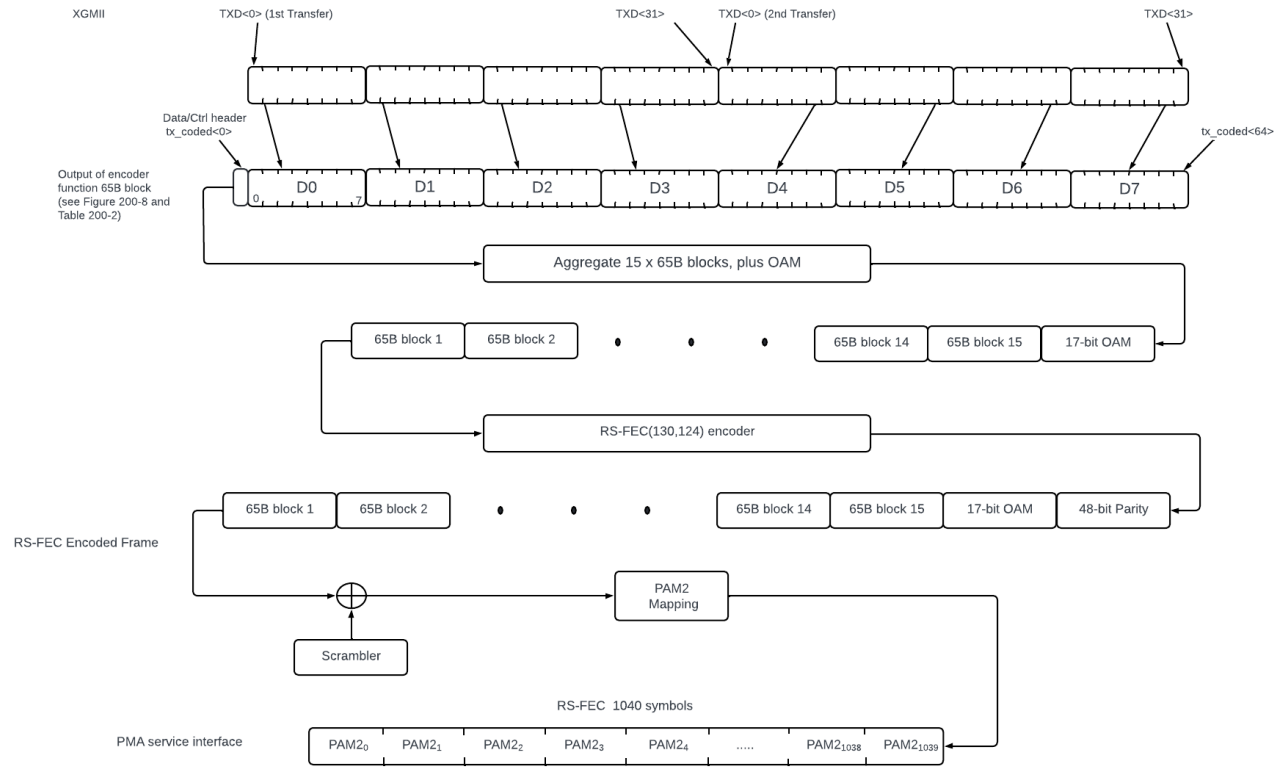
  - During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes request for remote transmitter settings. (200.6.2.4).

  - If a PMA_TXMODE indication message has the value SEND N. the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control.

  - L interleaving and Superframe structure is similar to MultiGBASE-T1.

Figure 200-6-1 MASTER PCS Transmit bit ordering

- **200.4.2.2 PCS Transmit Function**
  - **200.4.2.2.2 65B RS-FEC transmission code – MASTER (100M+MultiGBASE-T1/V1)**



Note 1 -- This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters

Figure 200-6-1 MASTER PCS Transmit bit ordering

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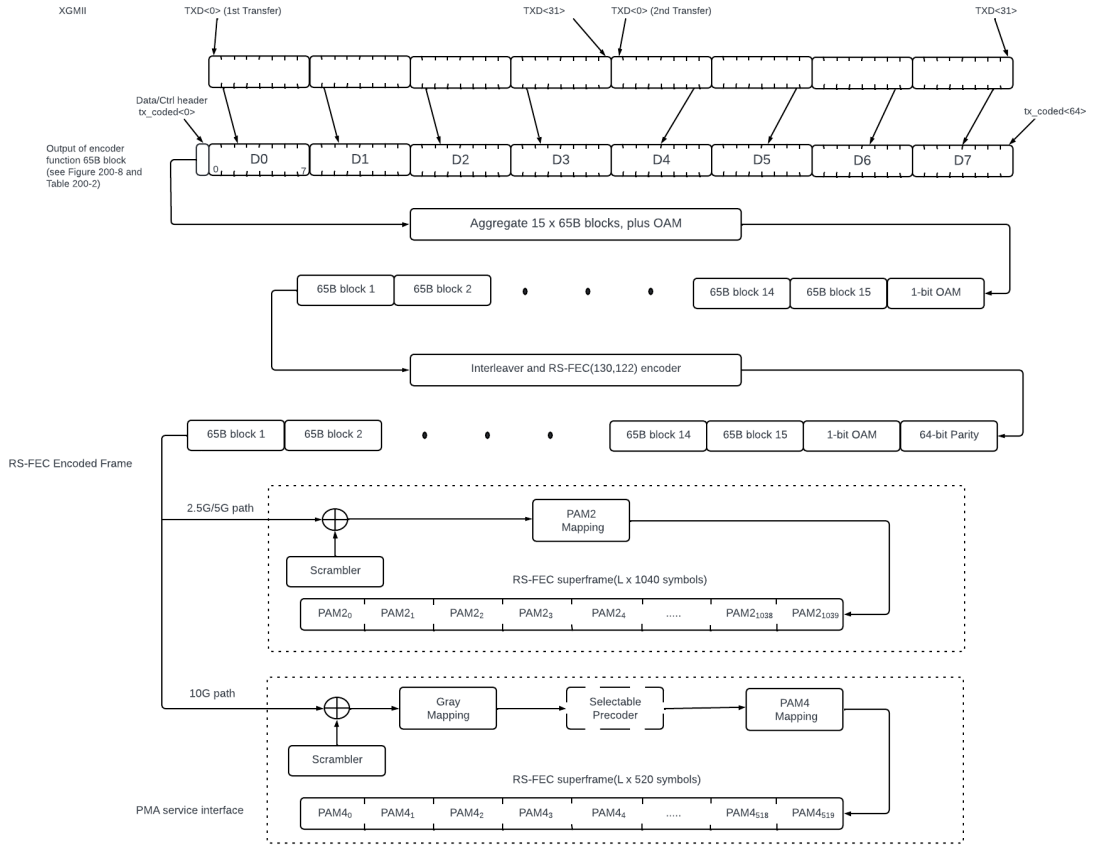
Figure 200-6-2 SLAVE PCS Transmit Bit ordering

- **200.4.2.2 PCS Transmit Function**
  - **200.4.2.2.2 65B RS-FEC transmission code -- SLAVE(MultiG+100MBASE-T1/V1)**



Note 1 -- This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters
Note 2-- Figure shown for L=1
Note 3-- Either the PAM2 or the PAM4 path is choosen

Figure 200-6-2 SLAVE PCS Transmit bit ordering

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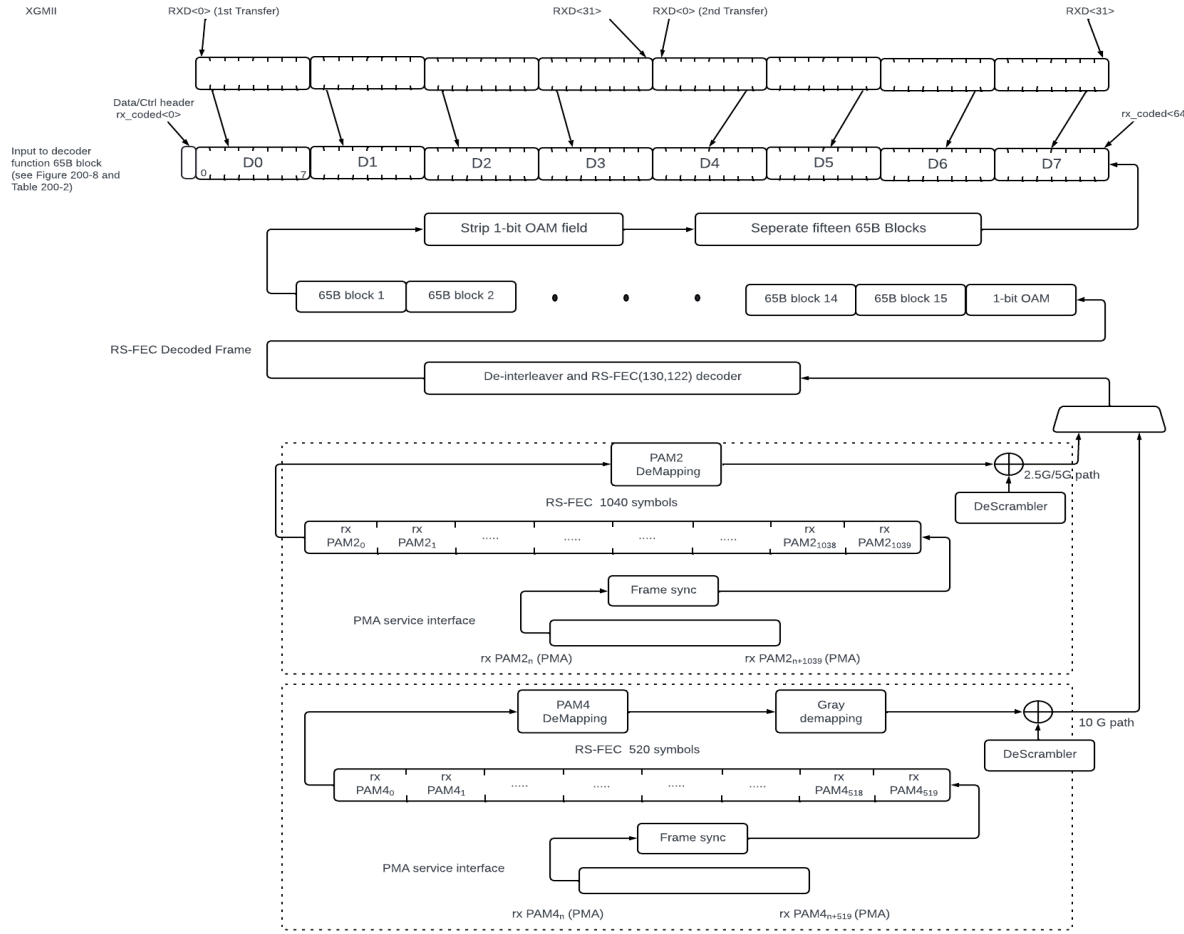
Figure 200-7-1 MASTER Receive bit ordering

- **200.4.2.2 PCS Transmit Function**
  - **200.4.2.2.2 65B RS-FEC transmission code MASTER(100M+MultiGBASE-T1/V1) RX**



Note 1 -- This figure shows the mapping from the a 64B/65B block to a block containing eight data characters to the XGMII
Note 2 -- FIgure shown for L=1

Figure 200-7-1 MASTER PCS Receive bit ordering

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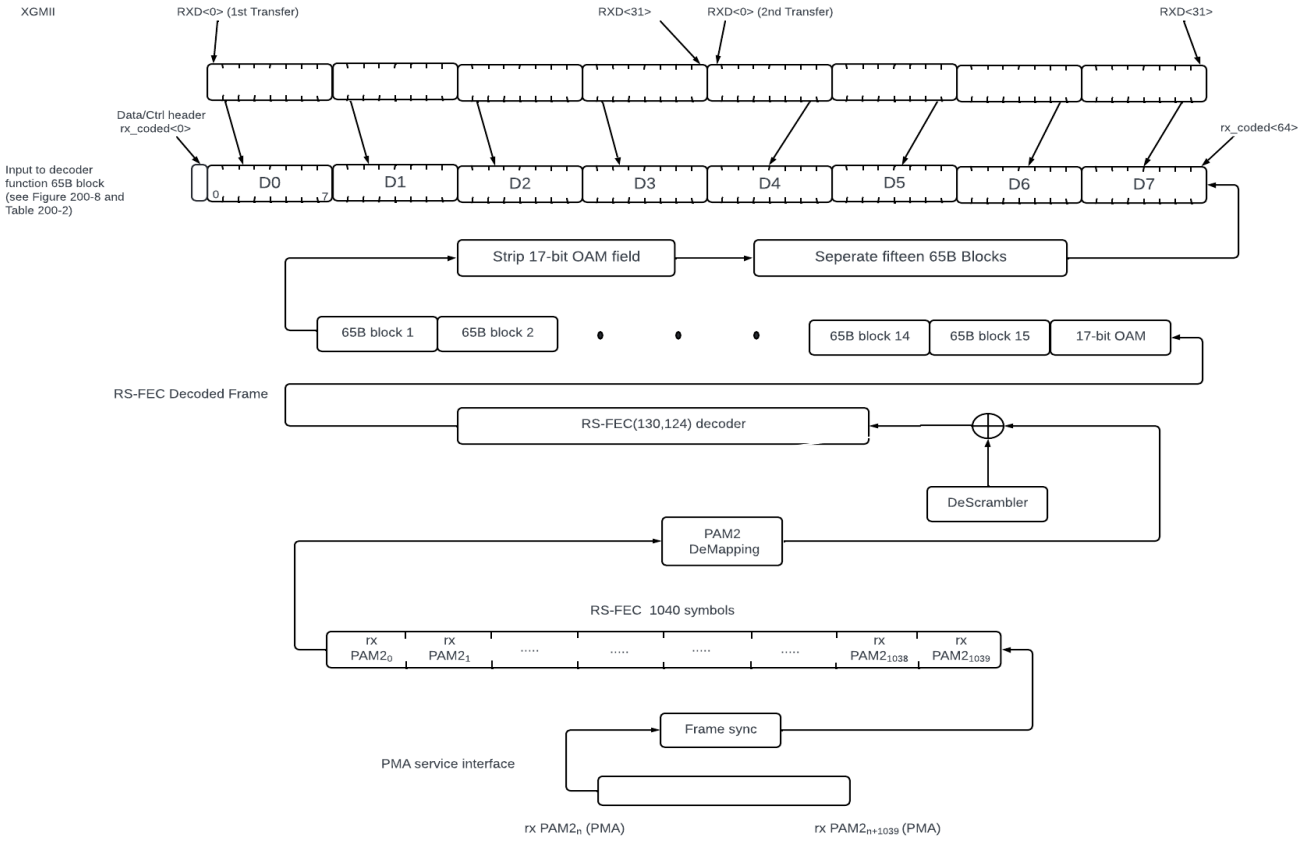
Figure 200-7-2 Slave Receive bit ordering

- **200.4.2.2 PCS Transmit Function**
  - **200.4.2.2.2 65B RS-FEC transmission code – SLAVE(MultiG+100MBASE-T1/V1) RX**



Note 1 -- This figure shows the mapping from the a 64B/65B block to a block containing eight data characters to the XGMII

Figure 200-7-2 SLAVE PCS Receive bit ordering

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PCS (200.4.2.2.3-8)

- **200.4.2.2.3 Notation conventions**

  As specified for MultiGBASE-T1 in 149.3.2.2.3

- **200.4.2.2.4 Block structure**

  As specified for MultiGBASE-T1 in 149.3.2.2.4

- **200.4.2.2.5 Control Codes**

~~The same set of control characters are supported by the XGMII and the 2.5G/5G/10GBASE-T1 PCS.~~ All control characters except LPI are supported by both the XGMII and the DM's PCS, as DM does not support EEE. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The ~~2.5G/5G/10GBASE-T1~~ PCS encodes the start and terminate control characters implicitly by the block type field. The ~~2.5G/5G/10GBASE-T1~~ PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The ~~2.5G/5G/10GBASE-T1~~ PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to ~~2.5G/5G/10GBASE-T1~~ control codes and XGMII control codes are specified in Table ~~149–2~~. All XGMII control code

Table ~~149–2~~—Control codes for ~~MultiGBASE-T1~~

Control character	Notation	XGMII control code	~~2.5G/5G/10G BASE-T1~~ control code	~~2.5G/5G/10G BASE-T1~~ O code
idle	/I/	0x07	0x00	
~~LPI~~	~~/LI/~~	~~0x06~~	~~0x06~~	
start	/S/	0xFB	Encoded by block type field	
terminate	/T/	0xFD	Encoded by block type field	
error	/E/	0xFE	0x1E	
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0		0x1C	0x2D	reserved0
reserved1		0x3C	0x33	reserved1
reserved2		0x7C	0x4B	reserved2
reserved3		0xBC	0x55	reserved3
reserved4		0xDC	0x66	reserved4
reserved5		0xF7	0x78	reserved5
Signal ordered set[1]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

[1]Reserved for INCITS T11 Fibre Channel use.

- **200.4.2.2.6 Ordered sets**

  As specified for MultiGBASE-T1 in 149.3.2.2.6

- **200.4.2.2.7 Idle (*/I/*)**

  As specified for MultiGBASE-T1 in 149.3.2.2.7

- **200.4.2.2.8 ~~LPI (*/LI/*)~~**

~~**149.3.2.2.8 LPI (/LI/)**~~

~~Low Power Idle (LPI) control characters (/LI/) on the XGMII indicate that the LPI client is requesting operation in the LPI transmit mode. A continuous stream of LPI control characters (/LI/) is used to maintain a link in the LPI transmit mode. Idle control characters (/I/) are used to transition from the LPI transmit mode to the normal mode. PHYs that support EEE respond to the LPI XGMII control characters using the procedure outlined in 149.1.3.3. LPI characters may be added or deleted by the PCS to adapt between clock rates. /LI/ insertion and deletion shall occur in groups of four. /LI/s may be added following Low Power Idle characters. They shall not be added while data is being received.~~

~~If EEE is not supported, then /LI/ is not a valid control character.~~

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PCS (200.4.2.2.9-13)

- **200.4.2.2 PCS Transmit Function**
  - **200.4.2.2.9 as specified in 802.3 .ch 149.3.2.2.9**
  - **200.4.2.2.10 as specified in 802.3 .ch 149.3.2.2.10**
  - **200.4.2.2.11 as specified in 802.3 .ch 149.3.2.2.11**
  - **200.4.2.2.12 as specified in 802.3 .ch 149.3.2.2.12 with following modification**
  - **200.4.2.2.13 Transmit process (TBD)**

The 100M+MultiGBASE-T1/V1 PHY transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 30 XGMII data transfers are encoded into an RS-FEC frame. It takes 1040 PMA_UNITDATA transfers to send an RS-FEC frame of data.

The MultiG+100MBASE-T1/V1 PHY transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 30 XGMII data transfers are encoded into an RS-FEC frame. For 2.5Gbps and 5Gbps mode, it takes 1040 PMA_UNITDATA PAM2 transfers to send an RS-FEC frame of data. For 10Gbps mode, it takes 520 PMA_UNITDATA PAM4 transfers to send an RS-FEC frame of data.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 200-16). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and scrambler. Tx_coded<0> contains the data/ctrl header and the remainder of bits contain the block payload

PCS (200.4.2.2.14-15)

- **200.4.2.2 PCS Transmit Function**
  - **200.4.2.2.14 RS-FEC framing and RS-FEC encoder**

For 100M+MultiGBASE-T1/V1 PHY(MASTER) transmission, the resulting RS-FEC frame of 15 65B blocks, followed by the 17-bit OAM/Reserved field and 48 parity bits is 1040 bits. See Figure 200-6-1 and 200.4.2.2.17 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 992-bit vector, consisting of tx_group15x65B, and the 17-bit OAM/Reserved field, and shall generate the 6 8-bit parity symbols(48 bits total).

For MultiG+100MBASE-T1/V1 PHY(SLAVE) transmission, the resulting RS-FEC frame of 15 65B blocks, followed by the 1-bit OAM/Reserved field and 64 parity bits is 1040 bits. See Figure 200-6-2 and 200.4.2.2.17 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 976-bit vector, consisting of tx_group15x65B, and the 1-bit OAM/Reserved field, and shall generate the 8 8-bit parity symbols(64 bits total).

  - **200.4.2.2.15 RS-FEC framing and RS-FEC encoder**

The interleaver depth L of the transmitter shall be predefined for each speed.

When the defined interleaving depth L=1, there is no interleaving, and the RS-FEC superframe is the same as the RS-FEC frame.

When the defined interleaving depth L>1, the round-robin interleaving scheme as shown in Figure 200-9 shall be applied

100M+MultiGBASE-T1/V1 PHY (MASTER) transmission only supports L=1 (no interleaving)

For MultiG+100MBASE-T1/V1 PHY(SLAVE) transmission, 2.5G+ 100M BASE-T1/V1 only supports L=1, 5G+ 100M BASE-T1/V1 only supports L=2, 10G+ 100M BASE-T1/V1 only supports L=4

The MultiG+100MBASE-T1/V1 PHY PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe. There are 976 x L bits, or 122 x L Reed-Solomon message symbols in total in the input superframe. The corresponding message symbols are $m_{122xL-1}$, $m_{122*L-2}$, …m_1,m_0. These message symbols are distributed to L RS-FEC encoders. When L>1, each RS-FEC encoder receives one out of every L message symbols from the superframe; otherwise, the RS-FEC encoder operates exactly the same as specified in 200.4.2.2.17

PCS(200.4.2.2.15-17)

- 200.4.2.2.15-17

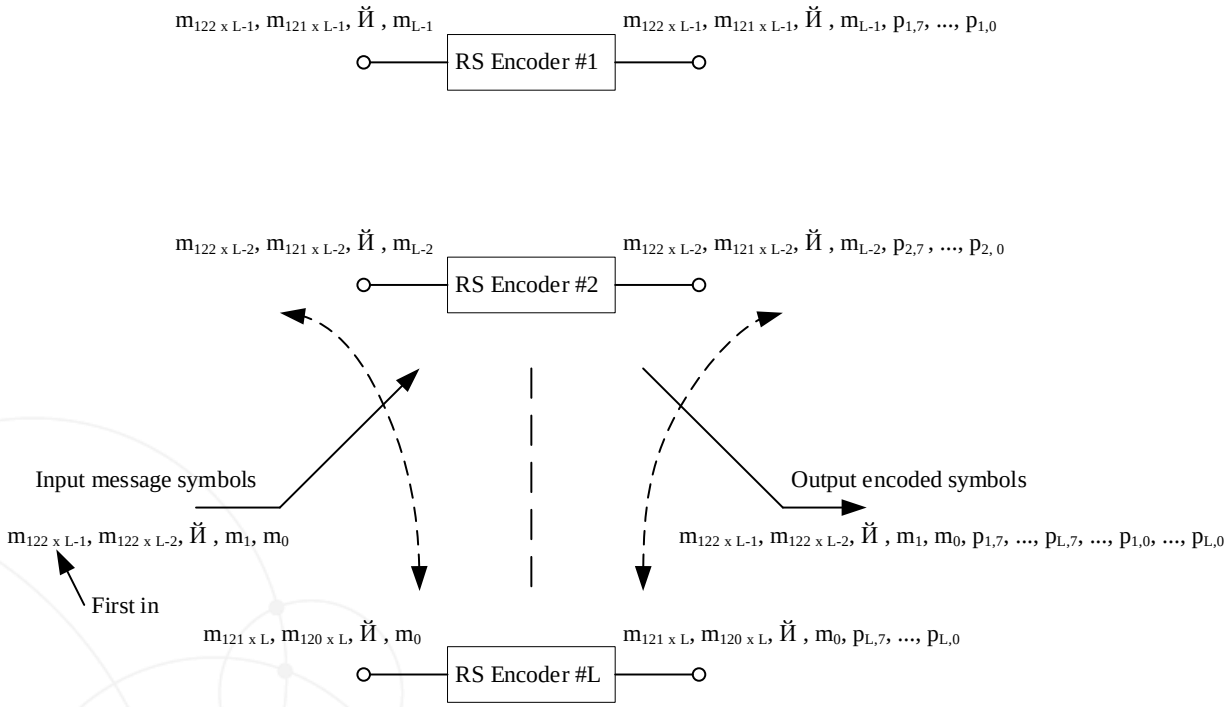
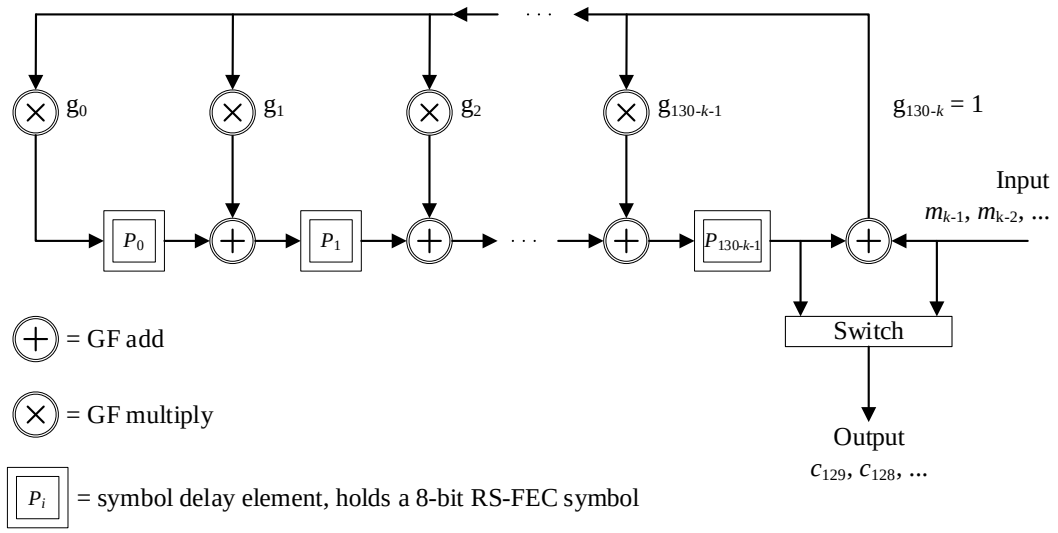


Figure 200–9 —Interleaving block diagram with interleaving depth L

Figure 200–10—Reed-Solomon encoder functional model



The coefficients of the generator polynomial for the code are presented in Table 200–3.

Table 200–3—Coefficients of the generator polynomial g_i (decimal)

i	MASTER RS-FEC(130,124)	SLAVE RS-FEC(130,122)
0	38	24
1	227	200
2	32	173
3	218	239
4	1	54
5	63	81
6	1	11
7	—	255
8	—	1

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PCS (200.4.2.2.18-22)

- **200.4.2.2.18 PCS scrambler – as specified in 149.3.2.2.18 w/ modification of equation 149-4 to following**

$$A_n = \begin{cases} DS_n[0] \oplus Tr_n[0] & pcs\_data\_mode = FALSE \\ DS_n[0] \oplus D_n[0] & pcs\_data\_mode = TRUE \end{cases}$$

$$B_n = \begin{cases} DS_n[1] \oplus Tr_n[1] & pcs\_data\_mode = FALSE \\ DS_n[1] \oplus D_n[1] & pcs\_data\_mode = TRUE \end{cases}$$

Equation: 200-4

- **200.4.2.2.19 Gray mapping for PAM4 encoding – as specified in 149.3.2.2.19**
- **200.4.2.2.20 Selectable precoder —as specified in 149.3.2.2.20 (TBD???)**
- **200.4.2.2.21 PAM4 encoding – as specified in 149.3.2.2.21**
- **200.4.2.2.22 PAM2 mapping**
  - Input bit S_n is mapped to the transmit symbol T_n as follows: if S_n=0 then T_n=+1, if S_n=1 then T_n=-1

PCS (200.4.2.3)

- **200.4.2.3 PCS Receive Function**
  - **As specified in clause 149.3.2.3 with modifications**
    - The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 200-17, and the PCS Receive bit ordering in Figure 200-7-1 and Figure 200-7-2 including compliance with the associated state variable as specified in 200.4.7.2.2
    - Following descrambling, the L-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. For MASTER, the RS-FEC decoded frame is then separated into a 1-bit OAM field and 15 64B/65B blocks. In each burst, the 25 superframes can form 25-bit, 50-bit and 100-bit OAM field, for 2.5Gbps, 5Gbps, and 10Gbps mode, respectively. For SLAVE, the RS-FEC decoded frame is then separated into a 17-bit OAM field and 15 64B/65B blocks.
    - This process generates the 64B/65B block vector rx coded <64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 200-17). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.
    - During PMA training mode, PCS Receive checks the received PAM2 or PAM4 framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_ SCRSTATUS.request primitive to OK.
    - When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 (TBD, MASTER and SLAVE difference?) consecutive RS-FEC frame errors are detected, the block lock flag is de-asserted. The block lock flag is re-asserted upon detection of a valid RS-FEC frame. When block lock is asserted and hi _rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD 31:0> and RXC <3:0> on the XGMII.
    - When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMARXSTATUS.indication(loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process when PHY control is in PCS_DATA state. The PCS Synchronization process sets the block lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes a refresh header. It also includes training payload which has an Infofield, inserted in the *N_inf* th bit of the training payload(specified in clause 200.4.5.3). When the PCS Synchronization process is synchronized to this pattern, block lock is asserted.
    - TDD related description(TBD)

PCS (200.4.4)

- **200.4.4 Side-stream scrambler polynomials**

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ Equation ~~(149–5)~~ as transmitter side-stream scrambler generator polynomial.

$$g_M(x) = 1 + x^{13} + x^{33} \qquad \text{~~(149–5)~~}$$

If the PMA_CONFIG.indication message assumes the value of SLAVE, PCS Transmit shall employ Equation ~~(149–6)~~ as transmitter side-stream scrambler generator polynomial.

$$g_S(x) = 1 + x^{20} + x^{33} \qquad \text{~~(149–6)~~}$$

An implementation of MASTER and SLAVE PHY side-stream scramblers by linear-feedback shift registers is shown in Figure ~~149–~~11. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

This scrambler, once started during PMA training, shall continue to run uninterrupted ~~during the transition from PAM2 to PAM4.~~ during PMA training frames and data mode frames(including refresh header and payload), and shall stop during QUIET

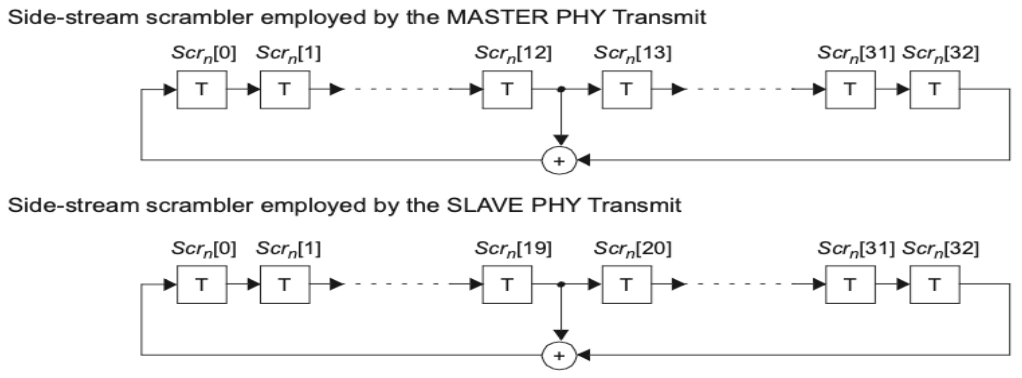

Figure ~~149–~~11—Realization of side-stream scramblers by linear feedback shift registers

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PCS (200.4.5)

- **200.4.5 PMA training frame**
  - Each PMA training frame includes a refresh header followed by a training payload.
  - Refresh header (refresh_hdr) is a sequence of PAM2 symbols with length of *N_r* symbols. Depending on which training phase and speed mode, training payload is a sequence of either PAM2 or PAM4 symbols with length of *N_p* symbols.
  - The 33 bit side-stream scrambler(Clause 200.4.4) is used to generate both refresh header and training payload. Once started at the beginning of 1st burst, this scrambler shall continue to run uninterrupted for each symbol during refresh headers and the training payloads and shall stop during the Quiet.
  - The refresh header and training payload data sequence bits are all 0s, with the exception that a 96 bits infofield is started at *N_inf* th symbol of the training payload. This data sequence *S_t(n)* is scrambled by the 33 bit side-stream scrambler, and it is defined in Equation 200-9.
  - The infoField is used to exchange messages between link partners during the startup training.
  - During the 10Gbps extended training mode (Training phase 2), the training payload transmitted by SLAVE shall map to PAM4 symbols. In all other cases, the training payload shall map to PAM2 symbols.
  - Refresh_hdr's and training payload's lengths are described in the 200.4.5.1, in Table 200-1, Table 200-2 and Table 200-3.

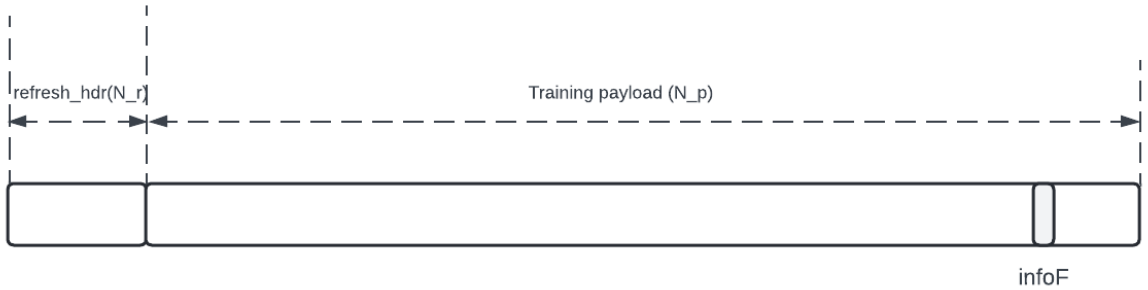

Figure 200-12 PMA Training frame

PCS (200.4.5.1)

- **200.4.5 PMA training frame (Continue)**
  - 200.4.5.1 Refresh Header and Training payload length

tx_mode	refresh_header N_r(symb)	training_payload N_p(symb)
SEND_TS	560	13200
SEND_TA	640	1040
SEND_TA_EXT	640	1040
SEND_N	640	1040

Table 200-4 N_r and N_p value for 100M+MultiGBASE-T1/V1 (Master) TX

tx_mode	refresh_header N_r(symb)	training_payload N_p(symb)
SEND_TS	560	13200
SEND_TA	480	26000
SEND_TA_EXT	N/A	N/A
SEND_N	480	26000

Table 200-5 N_r and N_p value for 2.5G+100MBASE-T1/V1 (Slave) TX

tx_mode	refresh_header N_r (symb)	training_payload N_p(symb)
SEND_TS	560	13200
SEND_TA	960	52000
SEND_TA_EXT	960(10G only)	52000(10G only)
SEND_N	960	52000

Table 200-6 N_r and N_p value for 5/10G+100MBASE-T1/V1 (Slave) TX

PCS (200.4.5.2)

- **200.4.5 PMA training frame (Continue)**
  - 200.4.5.2 Refresh header and training payload data bits generation

$$N\_b = \begin{cases} N\_p & \sim(tx\_speed=10Gbps * tx\_mode=SEND\_TA\_EXT) \\ 2* N\_p & tx\_speed=10Gbps * tx\_mode=SEND\_TA\_EXT \end{cases}$$

Equation: 200-7

$$N\_inf = \begin{cases} N\_b - 256 & \sim(tx\_speed=10Gbps * tx\_mode=SEND\_TA\_EXT) \\ N\_b - 512 & tx\_speed=10Gbps * tx\_mode=SEND\_TA\_EXT \end{cases}$$

Equation: 200-8

$$S\_t_k = \begin{cases} 0 & 0<= k <= N\_r+ N\_inf-1 \\ InfoField\ (k \bmod N\_r+N\_inf) & N\_r+N\_inf<= k <= N\_r+N\_inf + 95 \\ 0 & N\_r+N\_inf+96<= k <= N\_r+ N\_b-1 \end{cases}$$

Equation: 200-9

$$Tr_n[0] = \begin{cases} S\_t_{(n)} & \sim(tx\_speed=10Gbps * tx\_mode= SEND\_TA\_EXT) + (0<= n <=N\_r-1) \\ S\_t_{(2n-N\_r)} & tx\_speed=10Gbps * (tx\_mode= SEND\_TA\_EXT) * (N\_r <= n<=N\_r + N\_p -1) \end{cases}$$

$$Tr_n[1] = S\_t_{(2n-N\_r+1)} \qquad tx\_speed=10Gbps * (tx\_mode= SEND\_TA\_EXT) * (N\_r <= n<=N\_r + N\_p -1)$$

Equation: 200-10

- *N_b* is the number of bits in the training payload. *N_inf* is the bit position where infoField starts. The first bit start at bit 0.
- S_t_k is the PMA training frame bit sequence. It has all 0s, except at the infoField position. $0 <= k <= N\_r + N\_b - 1$
- For refresh header, or PAM2 training payload, $Tr_n[0]$ is the same as S_t_n and it is used as scrambler input.
- For PAM4 training payload, two bits are grouped into pairs, $Tr_n[0]$ and $Tr_n[1]$, where *n* is an index indicating the symbol number. The pair $\{Tr_n[0], Tr_n[1]\}$ will be used as scrambler input

PCS (200.4.5.3-4)

- 200.4.5.3 PMA training symbol generation

$$G_n = \text{Gray mapping } (\{A_n, B_n\})$$

Equation: 200-11

$$T_{(n)} = \begin{cases} PAM2\_Mapper(A_n) & \sim(tx\_speed=10Gbps * (tx\_mode=SEND\_N + tx\_mode=SEND\_TA\_EXT)) + \ (0<= n <= N\_r-1) \\ PAM4\_Mapper(G_n) & tx\_speed=10Gbps * (tx\_mode=SEND\_N + tx\_mode=SEND\_TA\_EXT) * (N\_r <= n <= N\_r+N\_p-1) \end{cases}$$

Equation: 200-12

$$O_n = \begin{cases} T_{(n)} & 0<= n <= N\_r + N\_p - 1 \\ 0 & N\_r + N\_p <= n <= N\_tdd-1 \end{cases}$$

Equation: 200-13

  - For PAM2 training frame, $Tr_n[0]$ shall be scrambled with the $DS_n[0]$ which is equal to $Scr_n[0]$ defined by clause 149.3.4. The output scrambled bit A_n shall be input to PAM2 mapper.
  - For PAM4 training payload, the pair of $Tr_n[0]$ and $Tr_n[1]$ shall be scrambled with two scrambler bits $DS_n[0]$ and $DS_n[1]$, defined by clause 149.3.4 and 149.3.2.2.18
  - The generation of scrambled bits $\{A_n,B_n\}$ can be found at Figure 200-5, with equation 200-4. The $\{A_n,B_n\}$ shall be input to the Gray mapping for PAM4 encoding specified by 149.3.2.2.19. The output G_n can be input to precoder(TBD) and then to the PAM4 mapper defined by 149.3.2.2.21
  - The inclusion of precoder defined in 802.3 ch is TBD

- 200.4.5.4 Generation of output symbol O_n
  - The transmit symbol O_n is selected by TDD control logic. For each TDD cycle (specified in Clause 200.4.6), the transmitter will send out T_n and 0, based on symbol time index n.
  - n will be continuous symbol count modulo *N_tdd.* The 33 bit scrambler shall be stopped during QUIET.
  - PAM2_Mapper is specified in 200.4.2.2.22
  - PAM4_Mapper is specified in 200.4.2.2.21
  - Gray mapping is specified in 200.4.2.2.19
  - *N_tdd* is the number of symbols equivalent to 9.6 us of TDD cycle time.

PCS (200.4.6)

- **200.4.6 PCS TDD signaling**

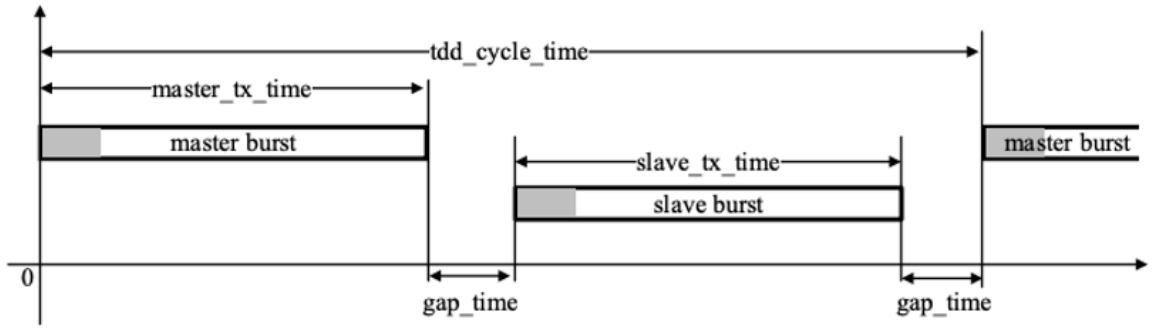

Figure 200-13 Master/Slave TDD cycle illustration

tx_mode	Master_tx_time (ns)	Slave_tx_time (ns)	tdd_cycle_time (ns)
SEND_TS	4586.67	4586.67	9600
SEND_TA	560	8826.67	
SEND_TA_EXT			
SEND_N			

Table 200-7 master_tx_time and slave_tx_time

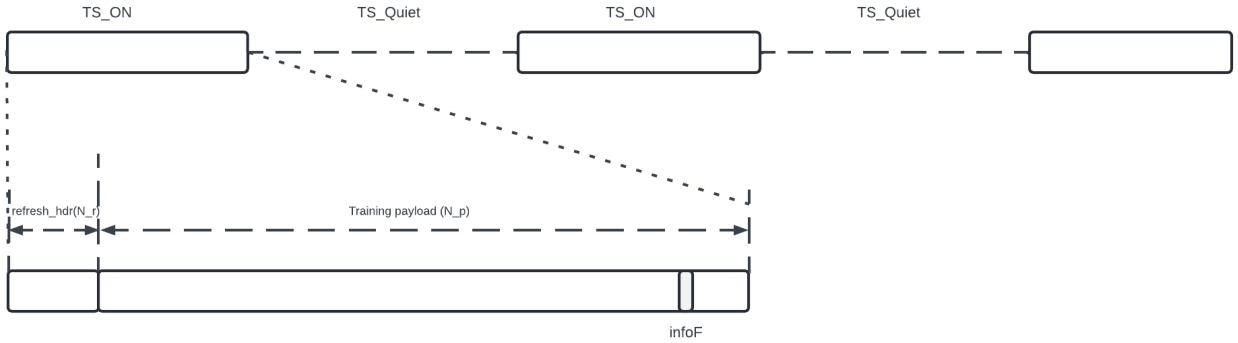

Figure 200-14-1 Symmetric training timing and frame structure

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Figure 200-14-2/3 Asymmetric Training/Data Mode- Timing and Frame Structure

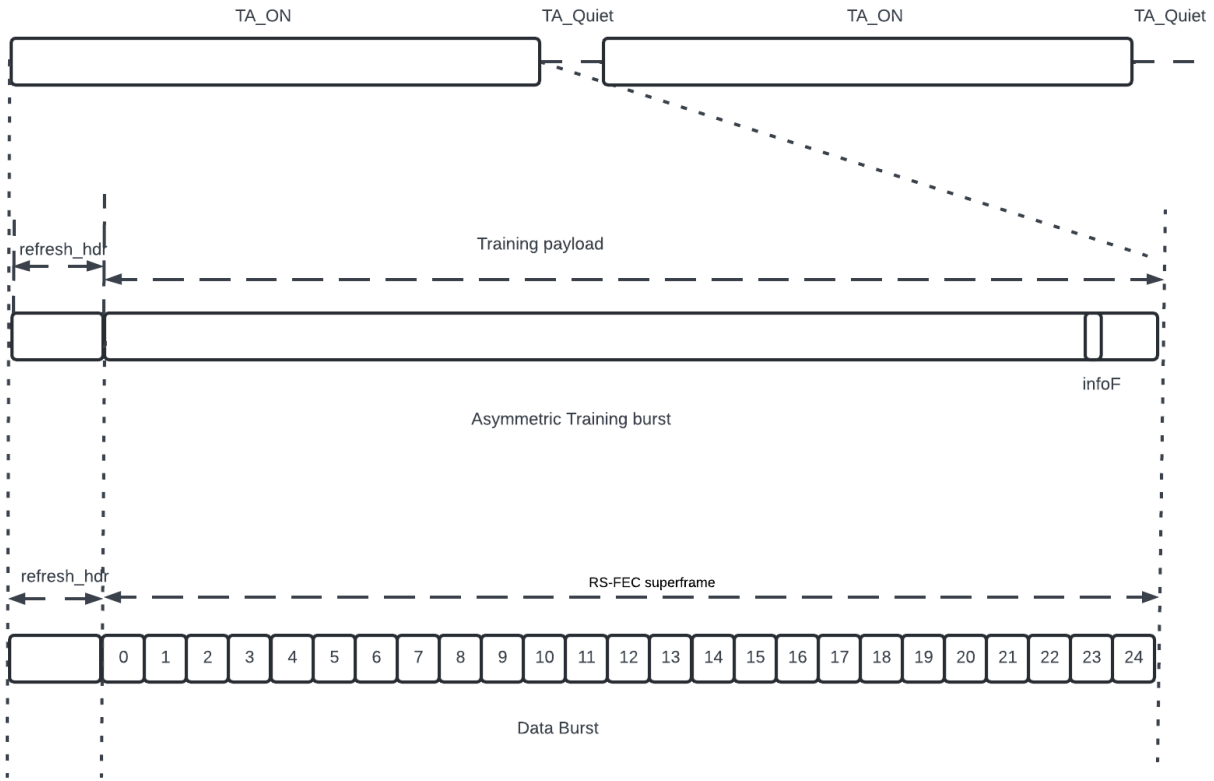

Figure 200-14-2 Asymmetric training/Data Mode timing and frame structure—MultiG+100MBASE-T1/V1 TX

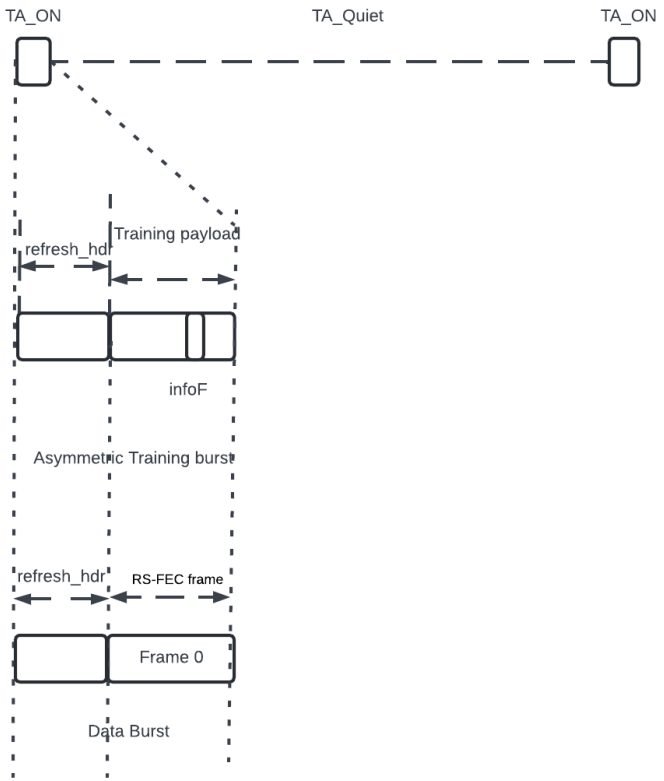

Figure 200-14-3 Asymmetric training/Data Mode timing and frame structure—100M+MultiGBASE-T1/V1 TX

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PCS (200.4.7)

- **200.4.7 PCS Detailed functions and state diagrams**
  - **200.4.7.1 State diagram conventions**

    As specified in 149.3.7.1
  - **200.4.7.2 State diagram parameters**
    - **200.4.7.2.1 Constants**

      As specified in 149.3.7.2.1, removed LPBLOCK_T and LPBLOCK_R for LPI mode.
    - **200.4.7.2.2 Variables**

      Removed 149.3.7.2.2 EEE/LPI related variables. Added variables to support TDD operation
    - **200.4.7.2.3 Timers**

      Removed 149.3.7.2.3 EEE/LPI related Timers. Added timers to support TDD operation
    - **200.4.7.2.4 Functions**

      Modified from 149.3.7.2.4, removed LPI related types in R_BLOCK_TYPE and T_BLOCK_TYPE
      - **DECODE()**
      - **ENCODE()**
    - **200.4.7.2.5 Counters**

      Modified from 149.3.7.2.5, removed LPI related counters
    - **200.4.7.2.6 Messages**
  - **200.4.7.3 State diagrams**

    Modified Figure 200-15 RFER monitor state diagram from 149-15, removed LPI related signals
    - **PCS Transmit state diagram**

      Modified Figure 200-16 from Figure 149-16, remove LPI related signal/paths. Removed original Figure 149-17
    - **PCS Receive state diagram**

      Modified Figure 200-17 from Figure 149-18, remove LPI related signal/paths. Removed original Figure 149-19

Figure 200-15 RFER Monitor Block Diagram

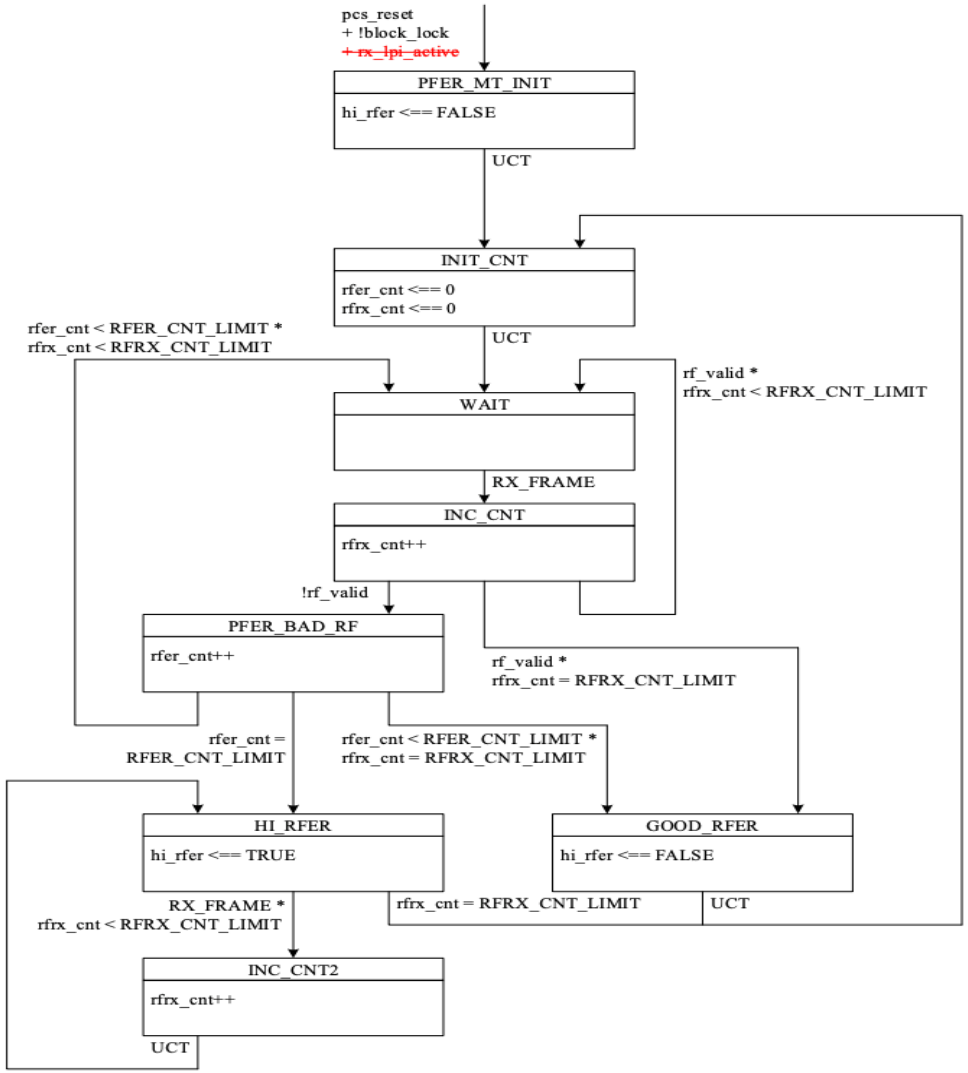

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Figure 200-16/17 PCS 64B/65B Transmit/Receive State Diagram

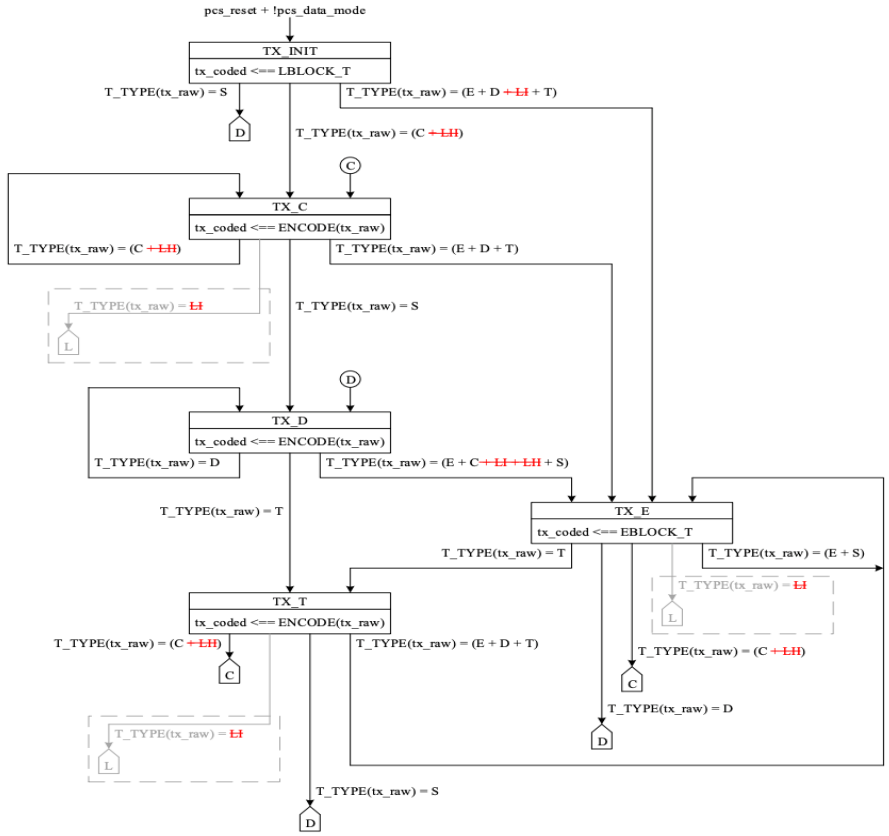

Figure 200-16 PCS 64B/65B Transmit State Diagram

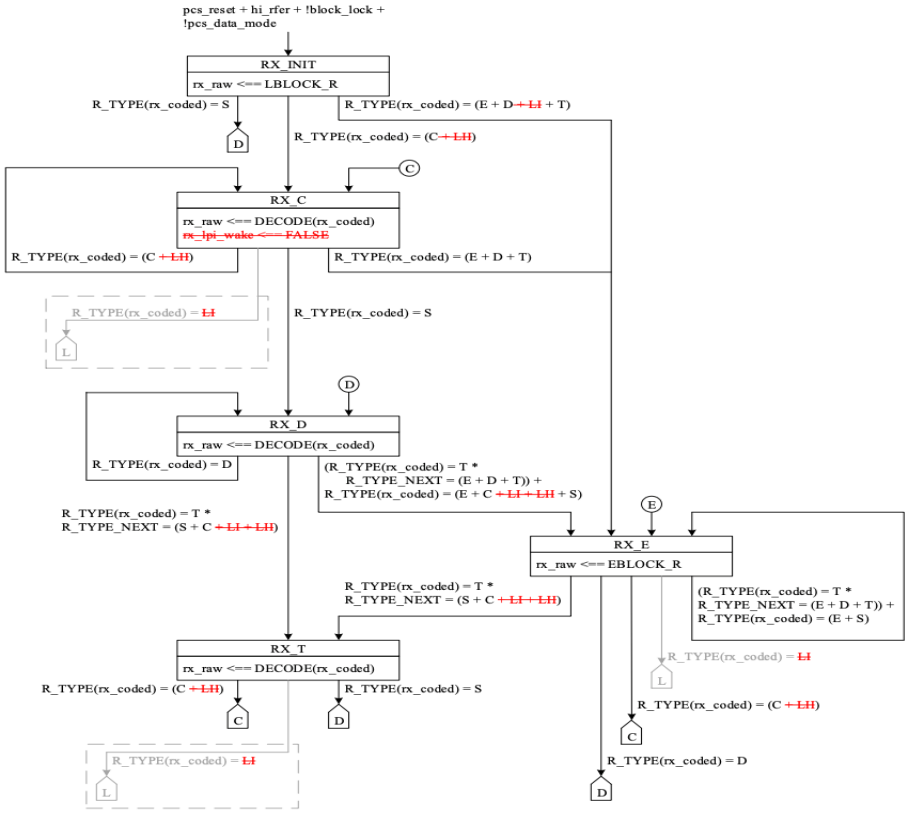

Figure 200-17 PCS 64B/65B Receive State Diagram

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200.6 Physical Medium Attachment(PMA) sublayer

- **200.6.1 PMA functional specifications**

  Modified from 149.4.1, with updated Figure 200-26 PMA reference diagram, to support TDD operation.

- **200.6.2 PMA functions**
  - **200.6.2.1 PMA Reset function**

    Modified from 149.4.2.1, with updated link up time proposal
  - **200.6.2.2 PMA Transmit function**

    Modified from 149.4.2.2, with updated text to support TDD operation
  - **200.6.2.3 PMA Receive function**

    Modified from 149.4.2.3, with updated text to support TDD operation
  - **200.6.2.4 PHY Control function**

    Modified from 149.4.2.4, with updated text to support TDD operation
  - **200.6.2.5 Link Monitor function**

    As specified in 149.4.2.5
  - **200.6.2.6 TDD Monitor function(TBD)**
  - **200.6.2.7 Clock Recovery function(TBD)**
- **200.6.3 MDI**
- **200.6.4 State variables**
  - **200.6.4.1 State diagram variables**
  - **200.6.4.2 Timers**
- **200.6.5 State diagrams**

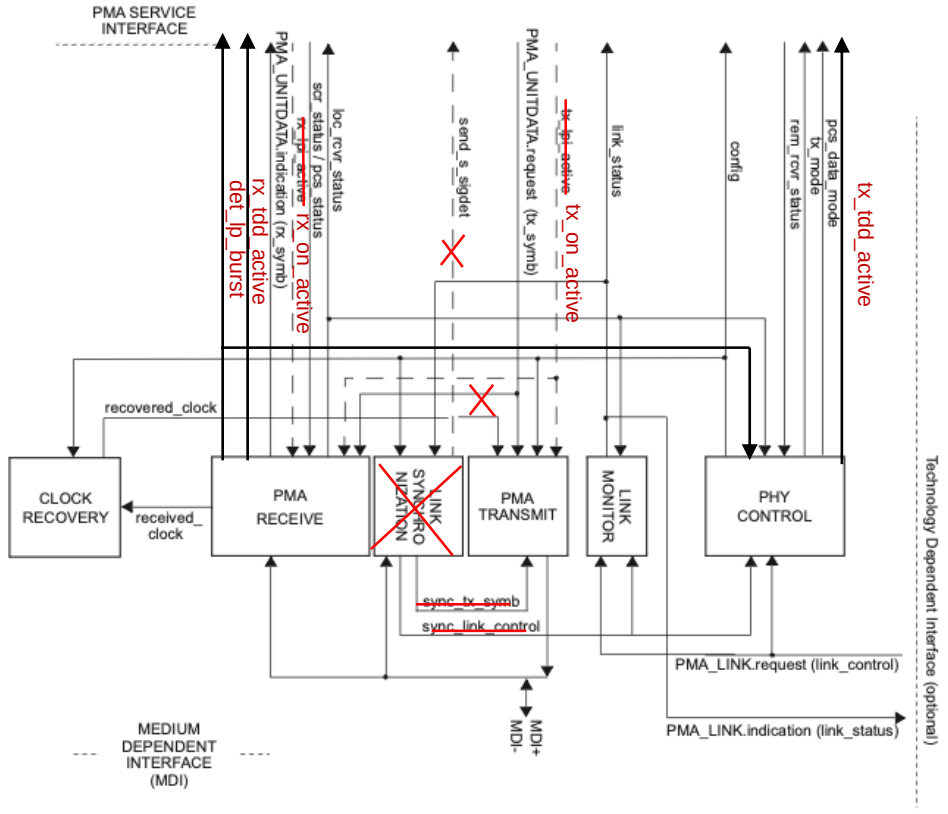
200.6 PMA functional specifications

- **200.6.1 PMA functional specifications**

149.4.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in ~~149~~.2.2 to the MultiGBASE-T1 baseband medium, specified in ~~149~~.7.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in ~~149~~.8.



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure ~~149~~–26—PMA reference diagram

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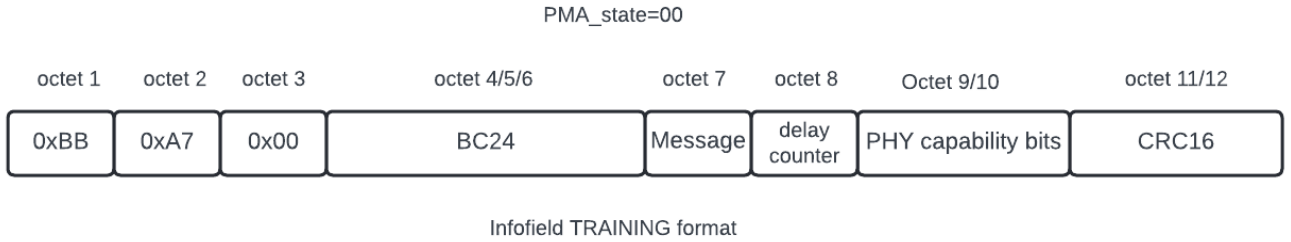
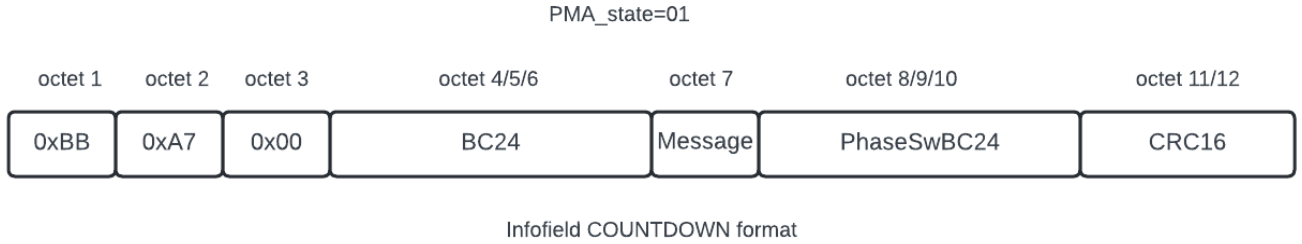
200.6.2.4 PHY Control function

- **200.6.2.4 PHY Control function**
  - PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 200-32.
  - During PMA training (TRAINING and COUNTDOWN states in Figure 200-32), PHY Control information is exchanged between link partners with a 12-octet Infofield, which is XORed with the 96 bits starting after the *N_inf* bit of the training payload specified in 200.4.5.3. The Infofield is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the training phase transition.
  - The 12-octet Infofield shall include the fields in 200.6.2.4.2 through 200.6.2.4.8, also shown in Figure 200-27 and Figure 200-28. Infofield shall be transmitted at least 16 (TBD) times with each change to octets 7 to 10.



Infofield TRAINING format

Figure 200-27



Infofield COUNTDOWN format

Figure 200-28

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200.6.2.4.4 Message Field

- **200.6.2.4.4 Message Field**
  - The Message Field is one octat. For both MASTER and SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, training_phase<4:3>, reserved<2:0>}.
  - The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6>=00 indicates TRAINING, and PMA_state<7:6>=01 indicates COUNTDOWN.
  - The two training_phase-indicator bits Training_phase<4:3> shall communicate the training phase of the transmitting transceiver to the link partner. Training_phase<4:3> =00 indicate SYMMETRIC TRAINING, Training_phase<4:3>=01 indicates ASYMMETRIC TRAINING, and Training_phase<4:3>=10 indicates extended ASYMMETRIC TRAINING in 10Gbps mode.
  - All possible Message Field settings are listed in Table 1 for MASTER or SLAVE. Any other values shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA burst shall be the first row of Table 1 for MASTER, and the first or second row of Table1 for SLAVE. Moreover, for a given Message Fields setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

PMA_state<7:6>	loc_rcvr_status	Training phase<4:3>	reserved	reserved	reserved
00	0	0	0	0	0
00	1	0	0	0	0
01	1	0	0	0	0
00*	0	1	0	0	0
00	1	1	0	0	0
01	1	1	0	0	0
00*	0	2	0	0	0
00*	1	2	0	0	0
01*	1	2	0	0	0

Table 1 -- Infofield message field valid MASTER or SLAVE settings

* Means this row could be skipped if not applicable

200.6.2.4.5 PHY capability bits

- **200.6.2.4.5 PHY capability bits**
  - When PMA_state<7:6>= 00, then [Oct9<7:0>,Oct10<7:0>] contains the PHY capability bits. Each octet is sent LSB first.
  - The format of PHY capability bits is Oct10<1:0>= PrecoderSel, Oct10<2>= OAMEn, Oct10<4:3>=Negotiated(operation) High speed, Oct10<7:5>=Speed Capability. Oct9<7:0>=VendorSpecificData[7:0]. Other bits are reserved.
  - Speed Capability (MultiG+100MBASE-T1/V1 PHY set its TX capability, 100M+MultiGBASE-T1/V1 PHY set its RX capability): Oct10<5> 2.5G capable, Oct10<6> 5G capable, Oct10<7> 10G capable.
  - Negotiated High speed: 00 -- 2.5G, 01– 5G, 10 – 10G
  - OAMEn: The optional BASE-T1/V1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen=1
  - PrecodeSel indicates the requested precoder.
  - The capability bit values shall be considered as valid only when loc_rcvr_status bit is 1.
  - The criteria to set Negotiated Speed is TBD

Table 200-11 – PHY capability bits

Oct 9								Oct 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData								PrecodeSel		OAMEn		Negotiated speed	Speed Capability 2.5G	Speed Capability 5G	Speed Capability 10G

200.6.2.4.6 TDD delay counter

- **200.6.2.4.6 TDD delay counter**
  - When PMA_state<7:6>=00, then Oct8<7:0> contains TDD delay counter sent LSB first. The format of TDD delay counter is Oct<1:0>= Reserved. Oct<2>= delay_count_valid. Oct<7:3>= delay _count<4:0>.
  - TDD delay counter is only defined during the symmetric training phase, when PMA_state<7:6>=00. The initial value shall be set to 0.
  - After MASTER PHY detects SLAVE TDD burst position, it should estimate the channel delay, then set its delay_count in the TDD delay counter to a value between 0 to 31(TBD), as well as set delay_count_valid bit to 1. Each LSB unit represents 5.333 ns delay (16 symbols in 3G symbol rate).
  - SLAVE shall accept the received remote delay_count only when received remote delay_count_valid bit is set to 1. SLAVE shall store this delay_count number.
  - As acknowledgement of the reception of this delay_count, SLAVE shall send back its received delay count in its own delay_count field and set its delay_count_valid to 1, so MASTER can confirm the exchange of this information is completed. When MASTER or SLAVE finishes the exchange of delay count, the negotiated speed, and the PrecodeSel, it shall set Negotiation_done signal to 1. The PHY control can then move to COUNTDOWN0 state, if loc_rcvr_status and rem_rcvr_status are both OK.
  - Starting from Asymmetric training and to the data mode, SLAVE shall adjust its transmit burst position according to the stored delay_count. It should move its transmit starting time (relative to the last MASTER payload bit at the SLAVE MDI input) earlier by 26.666ns + delay_count *5.333ns, compared with symmetric training case (200.6.2.4.11).

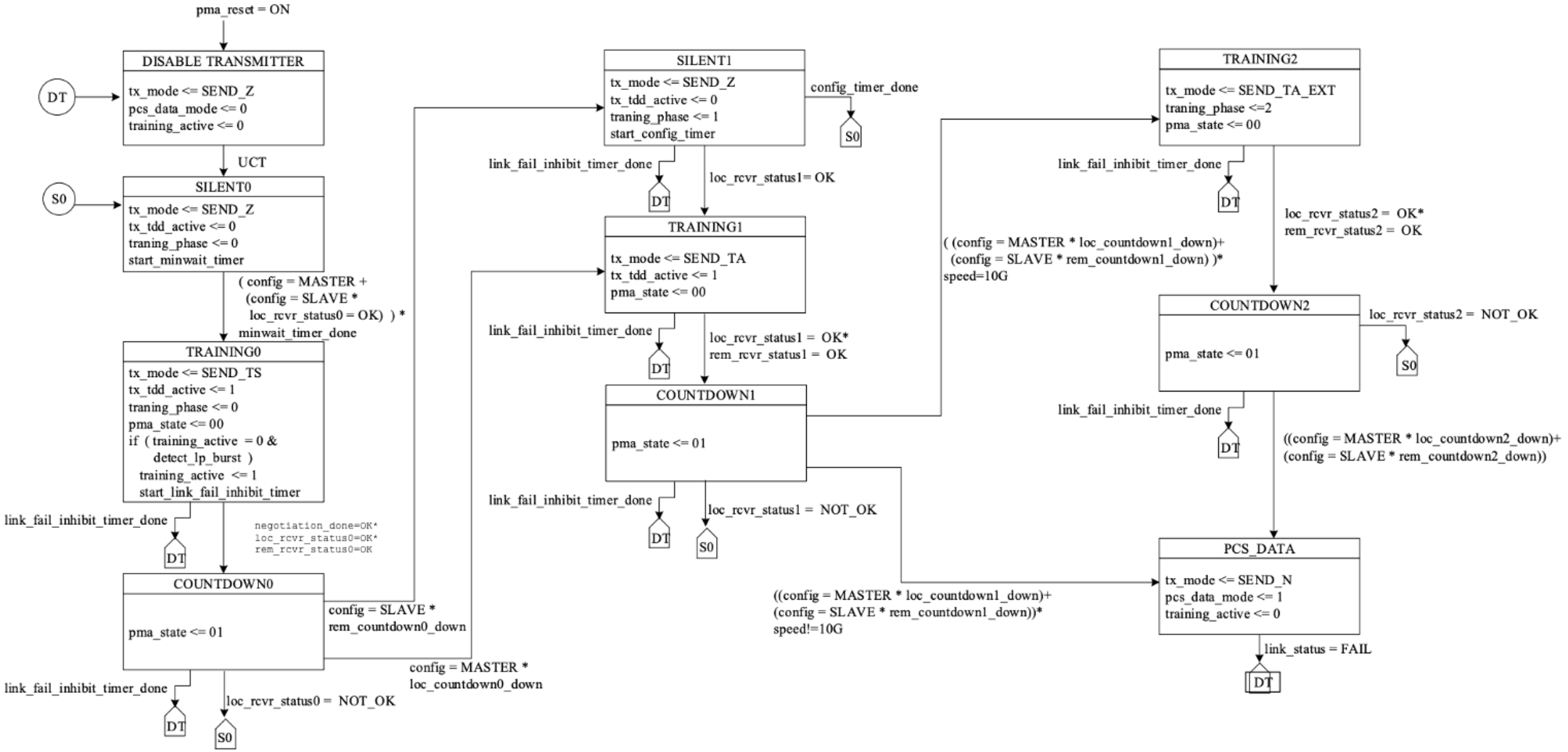
Table 200-12 – TDD delay counter

Oct 8							
0	1	2	3	4	5	6	7
Reserved		Delay_count_valid					Delay_count

200.6.2.4.10 Startup Sequence

- **200.6.2.4.10 Startup sequence**
  - The startup sequence shall comply with the state diagram description given in Figure 200-32. PMA_CONFIG is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.
  - During startup, prior to entering the TRAINING0 state, the SLAVE shall align its transmit PMA training frame to be 133.33 ns after the last PMA training payload bit from MASTER appears on the SLAVE input MDI. The SLAVE Infofield Burst count shall match the MASTER Infofield burst count from this previous PMA training frame.
    In the TRAINING0 state, PAM 2 transmission is used and PHY capabilities, PrecoderSel and delay_count are exchanged with Infofields as specified in 200.6.2.4.5. The final negotiated speed mode will be determined (TBD)
  - At any COUNTDOWN state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control returns to the SILENT0 state and attempts a retrain.
  - After starting TRAINING1/COUNTDOWN1 or TRANING2/COUNTDOWN2 or DATA MODE, the SLAVE shall use its stored MASTER transmitted delay_count to align its transmit PMA training frame to be 106.66ns – delay_count * 5.33ns (TBD), after the last PMA training payload bit from the MASTER appears on the SLAVE input MDI.
  - MASTER link_fail_inhibit_timer is started when it detects 1st SLAVE transmitted PMA training frame. SLAVE link_fail_inhibit_timer is started when it sends first PMA training frame to the MASTER. The link_fail_inhibit_timer value is defined to be 50 ms (TBD), it is used to force a restart if the link up cannot be achieved within maximum allowed time.
  - MASTER and SLAVE will move from TRAINING state to COUNTDOWN state, if local_rcvr_status and rem_rcvr_status are both asserted, and negotiation_done bit is OK.

Figure 200-32 PHYC Control State Diagram



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