Receiver Design Targets for an Asymmetric Camera PHY Link

May 14, 2025 New Orleans, Louisiana

Ahmad Chini, Mehmet Tazebay Broadcom Corporation

Foreword

- Receiver design for an asymmetric PHY is not unique even if all aspects of standard are specified and finalized. Implementers may take different approaches depending on target priorities of the design.
- At least two categories of design can be distinguished:
 - Performance optimized design
 - Complexity minimized design
- In this document, two design approaches are shown for a TDD-based 2.5Gbps/100Mbps link.

Performance Optimized Receiver Design

- For performance optimized receiver design, the following steps are suggested:
 - 1. Use Salz-SNR to identify frequencies with worst ingress noise performance.
 - Design receiver with a decision point SNR of about 10dB above the target BER requirement (e.g. for PAM2 with BER of 1e-12, design for dp-SNR > 27dB). With 10dB noise margin, the ingress noise may occupy up to 2/3 of the eye at decision point without affecting the BER.
 - 3. Simulate performance with ingress noise at worst frequencies to estimate ingress noise tolerance of a particular design.
- The above steps can be used with mixed mode equalization techniques (CTLE+DFE) to avoid more costly ADC based receiver design.

Example Salz-SNR analysis for ingress noise tolerance



https://www.ieee802.org/3/dm/public/0125/Chini_3dm_02a_0125.pdf

- The plot shown in the left are for a receiver that use CTLE+DFE for equalization (no ADC).
- Eye height referred to the receiver input shows how much noise is tolerated at each frequency without noise cancellation.
- For the particular implementation shown, the referred to input eye height is shaped by a CTLE (high + low pass filters).
- Ingress noise tolerance is lowest at about 500MHz for a 2.5Gbps/100Mbps TDD link.

Equalizer simulation for a typical Coaxial cable



https://www.ieee802.org/3/dm/public/0325/Chini_3dm_02b_0325.pdf

- Without ingress noise, decision point SNR is measured to be 32.8dB.
- With 100mVpp, 427MHz Ingress noise, the signal level drops by about 2/3 or 10dB.
- 10dB drop in signal due peak limited CW noise, brings SNR down to 22.8dB for this example and BER requirement of 1e-12 is met even with this additional ingress noise.

Next is a cost minimized receiver design at the camera side

Example of a cost minimized TDD receiver



- A cost minimized SerDes implementation use a CTLE to keep the eye.
- A single bit slicer converts signal into streams of bits for data and clock recovery.
- FIFO area is 0.001mm² in 16nm technology and is scaled for other technology sizes.
- Optimizing dp-SNR is not the target for such a design, eye opening is assumed to be sufficient.
- Eye diagram for a receiver with a fixed, 6dB passive¹ CTLE simulated for a 10.2m coaxial cable with 4 inline connectors and is shown next.

1- CTLE with higher gains and adaptive forms exist but was not used in this simulation

Eye at the Transmitter



Transmitter output **before** PoC distortion



Transmitter output after PoC distortion

Eye at the Receiver





Receiver input **before** CTLE

Receiver input after CTLE (6dB boost)

Eye with added Ingress Noise



100mVpp Ingress noise at 427MHz

100mVpp Ingress noise at 27MHz

• Eye is open at sampling point even with 100mVpp CW noise.

Conclusions

- When comparing relative receiver cost, it is important to note the target design goals.
- The receiver design may be done with performance in mind where some added area and complexity is absorbed in return for a good dp-SNR performance and with added system margin.
- The receiver can also be designed for the lowest area and complexity for a certain portion of the PHY down to a small fraction of a mm².
- When the image sensor die size is about 100mm^{2 (*)}, focusing on items taking a small fraction of mm² is not going to make a meaningful difference for the total relative cost.

https://www.ieee802.org/3/ISAAC/public/091423/2023-09-18_Automotive%20camera%20PHY%20requirements%20study_V2.3.pdf