Complexity and Performance Comparison of 802.3dm Architecture Proposals

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Foreword

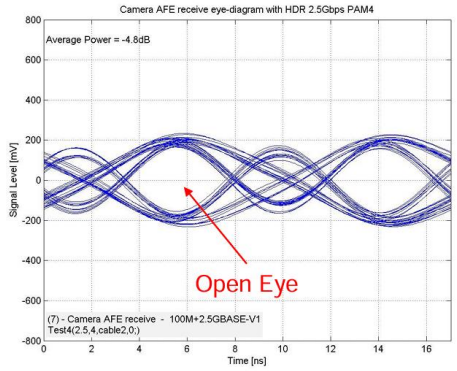
- While performance has always been a main discussion topic in Ethernet PHY protocol development, the automotive networking is in particular demanding for stringent emission and immunity requirements.
- In addition to performance, the complexity and power consumption have been cited for optimization in 802.3dm PHY.
- There has been a number of presentations so far discussing the performance and complexity of certain proposed implementations for TDD and ACT.
- In this presentation, the receiver complexity and performance are reviewed and compared for the 2.5Gbps/100Mbps link.

1- https://www.ieee802.org/3/dm/public/0125/Chini_3dm_01a_0125.pdf

ACT Analysis Platform - simDM[1]

- The simulation platform or ACT-simDM code is shared with the task force.
- ACT-simDM, uses **30 taps of fractional FFE and 10 taps of DFE** for downstream receiver and **1-tap FFE** with **1-tap DFE** for upstream receiver. The **ADC** digitization effect is not modeled (i.e. assumed negligible).
- **Fourth-order Butterworth** is used in both directions for both transmitter & receiver (4 filters).
- The upstream performance analysis is based on eye opening.
- The presentation[1] shows performance of a 2.5Gbps link with PAM2 modulation and 30mV of in-band CW noise as well as some other noise scenarios.

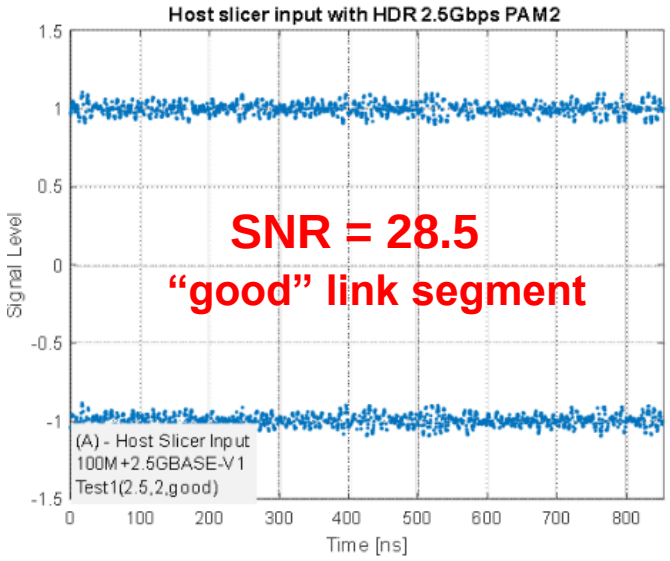
```
%%% Emulate LDR Tx and Rx analog filters as 4th order Butterworth filters %%%
[b,a] = butter(4,2.5/act.ldr_oversampling);  % 293MHz cut-off frequency
act.lkp.afe.tx_filter.a = a;
act.lkp.afe.tx_filter.b = b;
act.dut.afe.rx_filter.a = a;
act.dut.afe.rx_filter.b = b;

%%% Emulate HDR Tx and Rx analog filters as 4th order Butterworth filters %%%
[b,a] = butter(4,1/act.hdr_oversampling);
act.lkp.afe.rx_filter.a = a;
act.lkp.afe.rx_filter.b = b;
act.dut.afe.tx_filter.a = a;
act.dut.afe.tx_filter.b = b;

%%% Configure equalizer lengths %%%
eq_config.dut.ffe_length = 1; % Set DUT FFE length
eq_config.dut.dfe_length = 1; % Set DUT DFE length
eq_config.lkp.ffe_length = 30; % Set LKP FFE length
eq_config.lkp.dfe_length = 10; % Set LKP DFE length
```

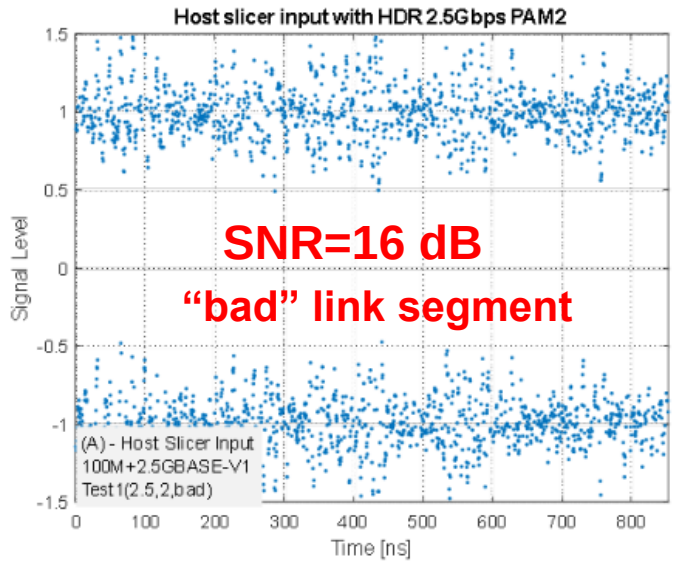


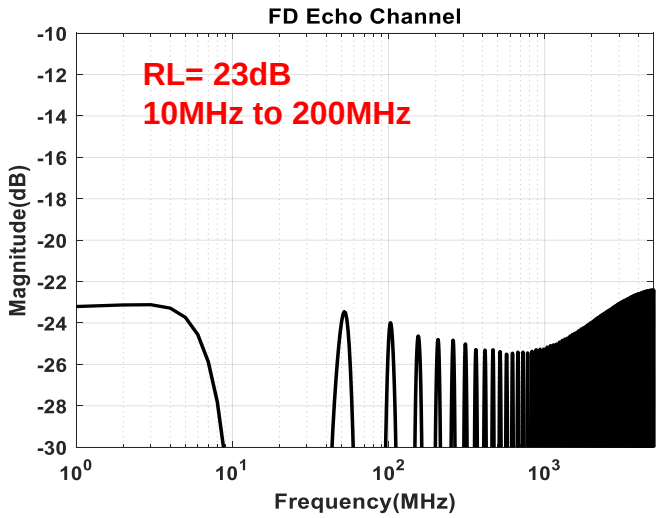
Low speed receiver Eye diagram

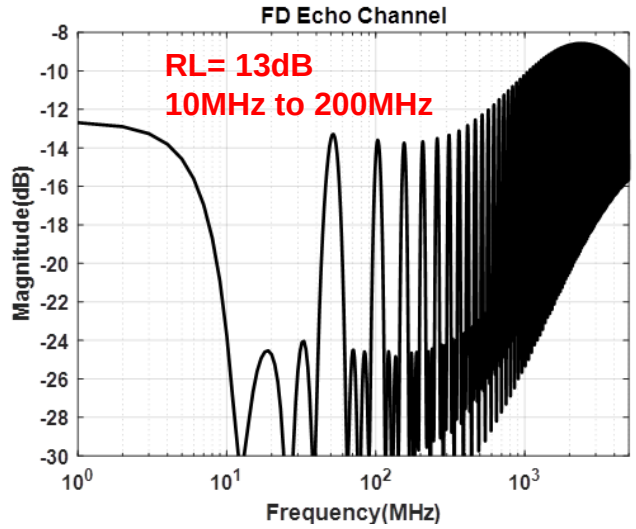
1. https://www.ieee802.org/3/dm/public/0325/jonsson_3dm_02_03_10_25.pdf

ACT-simDM[1], High Speed Receiver, “Good” versus “Bad” Cable



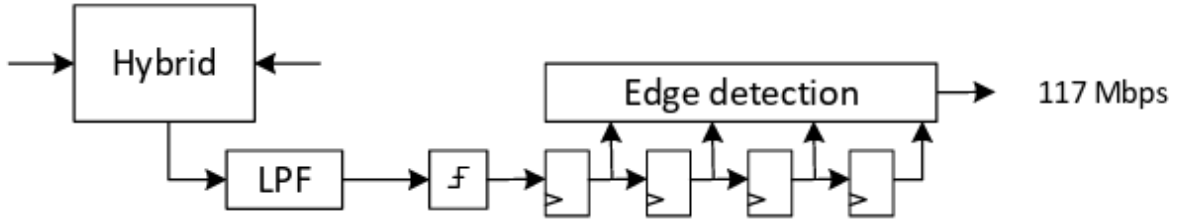






- SNR is calculated measuring the slicer input values.
- RL plots are shown for “good” and “bad” link segments used in the simulation.
- For the “bad” channel, when echo path is forced to zero, SNR seen to be 21dB. Therefore, an SNR of 16dB is dominated by low frequency echo.

ACT Low Speed Receiver, Alternative Implementation[2] (cntd.)



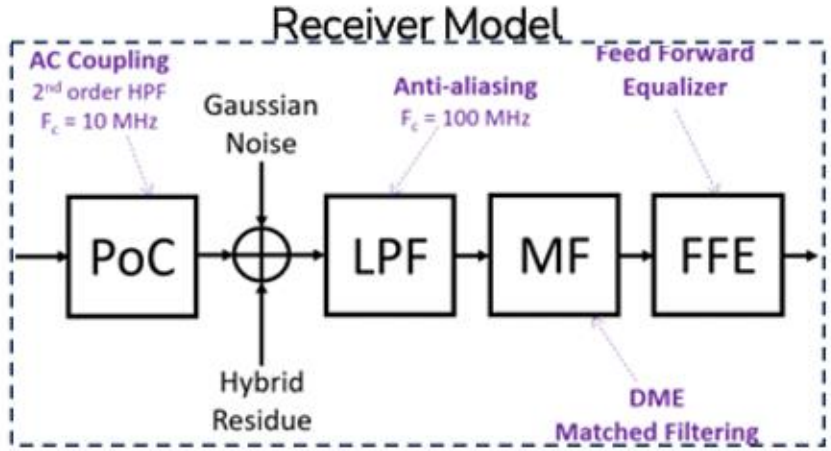
2. https://www.ieee802.org/3/dm/public/0125/Lo_3dm_02a_0125.pdf

- A cost minimized design is proposed in the cited contribution[2] for ACT receiver at the camera side.
- The received signal after Hybrid circuit is sampled and processed at a rate of 117MHz x 4 = 468Msps
- The low frequency echo from PoC circuit is not analyzed, no HPF is designed/considered in the receiver.
- Also, the ingress noise and the corresponding jitter effect (on the recovered clock) is not analyzed, in particular, for crystal-less solutions where recovered clock is used for camera transmitter (high speed TX).

ACT Low Speed receiver, Alternative Implementation[3] (cntd.)

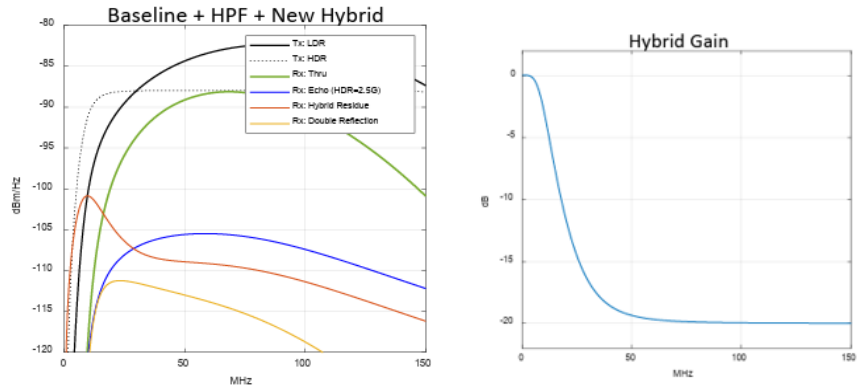
- A 30MHz HPF in the receiver is suggested to counter the echo from PoC circuit and weaker echo cancellation at low frequencies[3].
- The SNR is calculated to be **20dB** by frequency domain analysis for BW of 117MHz. The peak PSD of signal is seen in the plot -83dBm/Hz[1].
- The detailed architecture of DME match-filtering and FFE is not provided for complexity and performance analysis. A match-filter has to be implemented with a good resolution to avoid nonlinear behavior before FFE.
- LPF is designated as antialiasing filter but ADC and sampling rate is not specified for complexity and performance analysis.

1- Compare this with -94dBm/Hz for TDD (11dB higher)

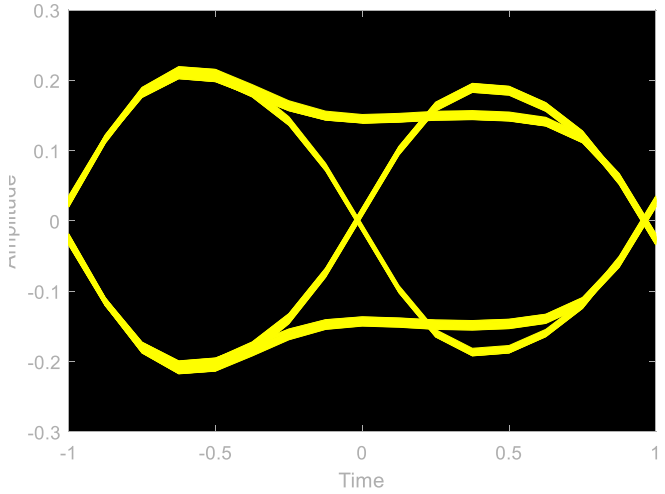


3. https://www.ieee802.org/3/dm/public/0325/sedarat_3dm_02_202503.pdf

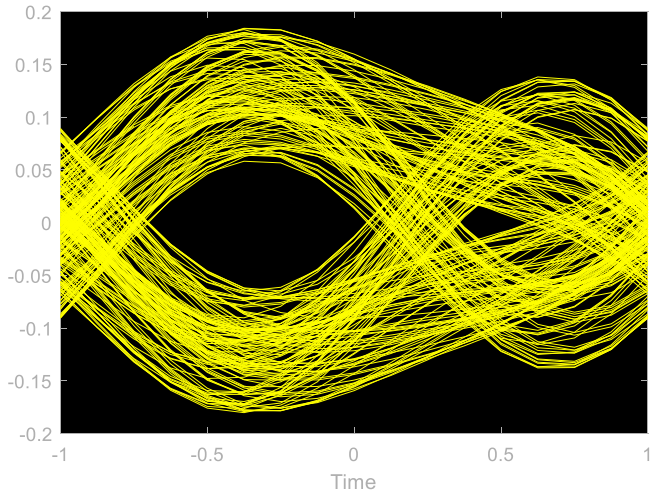
- Bandwidth: 117 MHz
- SNR: 20 dB (1 dB higher than baseline)



ACT Low Data Rate Receiver Simulation



Transmitter output (after TX LPF, 4th order and 6MHz PoC HPF)



Receiver after 30MHz HPF + LPF and 100mVpp noise at 70MHz

The channel echo (not considered in this simulation) results in additional distortion.

The time index is normalized to the baud rate.

- A simulation is performed to verify the eye opening and noise performance of the receiver with in-band ingress noise.
- DME encoding produces two types of pulses. Transmit signal eye diagram shows the two pulse types, one twice as wider than other one.
- When going through 30MHz HPF and the LPF in the receiver, the two pulse types encounter different delays, resulting in additional zero crossings jitter.
- In-band ingress noise further distorts the clock jitter and it complicates clock recovery and the effect on the bidirectional performance which should be analyzed.

TDD Low and High Data Rate Receiver Implementations

- Two different receiver implementation has been presented for the TDD 2.5Gbps/100Mbps link.
- The receiver design for optimized performance includes a CTLE, HPF and a DFE[1] with analog implementation. The same equalizer design may be used on both sides of a link for 2.5Gbps/100Mbps.
- Such a equalizer is several times less complex than the one suggested for ACT downstream receiver (see pages 4 and 5 of this presentation). The big portion of savings is in the elimination of ADC, but also in eliminating FFE and reduced DFE.
- The other obvious difference is in the performance, when dp-SNR is compared. For TDD, dp-SNR is 32dB with a typical[1] cable but dp-SNR may drop to 26.7dB due to secondary reflections[2] for cables with marginal RL. For ACT, dp-SNR is 16dB to 28.5dB depending on the channel return loss (see page 5 of this presentation).
- For upstream direction, a high performance receiver for TDD uses a DFE with total of 6 add/subtract taps where as ACT needs an ADC, full size DME and FFE (multipliers not adders). The calculated SNR for ACT is 20dB while for TDD, it is 26.7dB to 32dB depending on return loss effect on the secondary reflections[1,2]. TDD processes 1680bits in 9.6us (175Msps) where as ACT processes 234Msps continuously.

1. https://www.ieee802.org/3/dm/public/0325/Chini_3dm_02b_0325.pdf
2. https://www.ieee802.org/3/dm/public/0325/zimmerman_ILD_3dm_01_03052025.pdf

FEC Complexity and Performance

- TDD uses an 8-bit RS (130, 122) code while ACT uses a 10-bit RS (360, 326) code as in 802.3ch.
- The 10-bit RS (360, 326) is a stronger code and it helps with the reduced dp-SNR of ACT but the relative implementation cost is multiple of the shorter 8-bit code proposed for TDD. The code length is 3600 bits for ACT vs 1040bits for TDD.
- FEC decoding is optional for TDD given dp-SNR with a good margin at 2.5Gbps. If a decoder is implemented, a single error correcting decoder is more likely to be used for its lower complexity.

TDD and ACT receivers performance and complexity 2.5Gbps/100Mbps

	Complexity	dp-SNR	Jitter (Loop Timing)
Slave- Lowest cost receiver implementation	Negligible compared to Image Sensor for both TDD and ACT	Decision point SNR is not specified.	Received symbol Jitter is > 10 times higher for ACT as compared to TDD (baud rate difference)
Slave- High performance Receiver Implementation	TDD receiver is less complex than ACT high performance receiver	• ~27dB to 32dB for TDD • Up to 20dB for ACT depending on RL	Received symbol Jitter is >> 10 times higher for ACT as compared to TDD (baud rate and SNR difference)
Master- High performance Receiver Implementation	ACT receiver is several times more complex than TDD	• ~27dB to 32dB for TDD • 16dB to 28.5dB for ACT depending on RL	Good for both TDD and ACT (crystal based, free running)

Slave: Camera Receiver (low speed)
Master: ECU Receiver (high speed)

Summary and Conclusions

- The performance and complexity of various receiver implementations for TDD and ACT are reviewed with comments on the extent of the analysis and simulation.
- For TDD, the proposed equalizer design apply to both sides of the link (camera and ECU side) for 2.5Gbps/100Mbps.
- TDD outperforms ACT on both sides of the link when dp-SNR is compared.
- The complexity of the proposed architecture for ACT is several times higher than one proposed for TDD on the downstream (high speed direction).
- The camera transmit clock has to use its receiver's recovered clock. The excessive jitter on the receive path affects high speed direction performance and it requires further analysis for ACT-based PHY.
- Even with a better performance and lower link complexity, TDD peak PSD is less by about 10dB than ACT and therefore, it is less likely to cause emission issues.

Thank you for your attention

Questions?